### **Freescale Semiconductor**

Advance Information

# **High Speed CAN Transceiver**

The MC33901/34901 are high speed CAN transceivers providing the physical interface between the CAN protocol controller of an MCU and the physical dual wires CAN bus. They are packaged in an 8 pin SOIC with market standard pin out, and offer excellent EMC and ESD performance without the need for external filter components.

- Four devices variations are available:
- Versions with and without CAN bus wake-up.
- Versions with and without TXD dominant protection.

#### Features

- · Very low current consumption in standby mode
- Automatic adaptation to 3.3 or 5.0 V MCU communication
- Standby mode with remote CAN wake-up on some versions.
- Pin and function compatible with market standard

Cost efficient robustness:

- · High system level ESD performance
- Very high electromagnetic Immunity and low electromagnetic emission without common mode choke or other external components.

Fail-safe behaviors:

- TXD Dominant timeout, on the MC33901 version.
- Ideal passive when unpowered, CAN bus leakage current  ${<}10~\mu\text{A}.$
- VDD and VIO monitoring

Document number: MC33901 Rev. 1.0, 12/2013



### HIGH SPEED CAN TRANSCEIVER



EF SUFFIX (PB-FREE) 98ASB42564B 8-PIN SOICN

#### Industrial Applications (MC34901)

- Transportation
- Backplanes
- · Lift/elevators
- · Factory automation
- Industrial process control

#### Automotive Applications (MC33901)

- · Supports automotive CAN high-speed applications
- Body electronics
- · Power train
- · Chassis and safety
- Infotainment
- · Diagnostic equipment
- Accessories

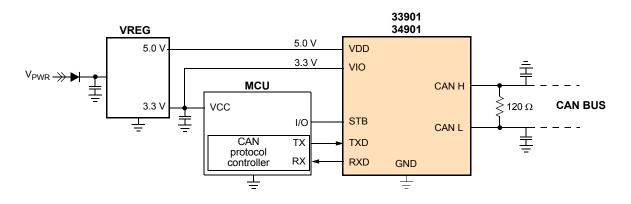


Figure 1. Simplified Application Diagram

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# 1 Orderable Parts

This section describes the part numbers available to be purchased along with their differences.

Part Number <sup>(1)</sup>	Temperature (T <sub>A</sub> )	Package	Wake-up Function	TXD dominant protection
MC33901WEF		SOIC 8 pins	Available	Available
MC33901SEF	40.4- 405.%O		Not Available	Available
MC34901WEF	-40 to 125 °C		Available	
MC34901SEF			Not Available	Not Available

Notes

1. To Order parts in Tape & Reel, add the R2 suffix to the part number.

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http:// www.freescale.com and perform a part number search.

# 2 Internal Block Diagram

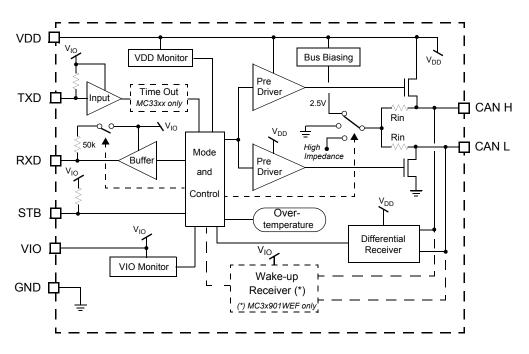
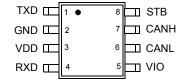


Figure 2. Internal Block Diagram

# 3 Pin Connections

## 3.1 Pinout





## 3.2 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 8.

### Table 2. 33901 Pin Definitions

Pin Number	Pin Name	Pin Function	Definition
1	TXD	Input	CAN bus transmit data input pin
2	GND	Ground	Ground
3	VDD	Input	5.0 V input supply for CAN driver and receiver
4	RXD	Output	CAN bus receive data output pin
5	VIO	Input	Input supply for the digital input output pins
6	CAN L	Input/Output	CAN bus low pin
7	CAN H	Input/Output	CAN bus high pin
8	STB	Input	Standby input for device mode selection

## 3.3 Maximum Ratings

### Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
ELECTRICAL	RATINGS				_
V <sub>DD</sub>	V <sub>DD</sub> Logic Supply Voltage	-0.3	7.0	V	
V <sub>IO</sub>	Input/Output Logic Voltage	-0.3	7.0	V	
V <sub>STB</sub>	Standby pin Input Voltage	-0.3	7.0	V	
V <sub>TXD</sub>	TXD maximum voltage range	-0.3	7.0	V	
V <sub>RXD</sub>	RXD maximum voltage range	-0.3	7.0	V	
V <sub>CANH</sub>	CANH Bus pin maximum range	-27	40	V	
V <sub>CANL</sub>	CANL Bus pin maximum range	-27	40	V	
V <sub>ESD</sub>	ESD Voltage			V	(2)
	Human Body Model (HBM) (all pins except CANH and CANL pins)		±2000		
	<ul> <li>Human Body Model (HBM) (CANH, CANL pins)</li> </ul>		±8000		
	Machine Model (MM)		±200		
	Charge Device Model (CDM)(/corners pins)		±500(/±750)		
	System level ESD			kV	
	<ul> <li>330 Ω / 150 pF Unpowered According to IEC61000-4-2:</li> </ul>		8.0	ĸv	
	• 330 $\Omega$ / 150 pF Unpowered According to OEM LIN, CAN, FLexray Conformance		6.0		
	<ul> <li>2.0 kΩ / 150 pF Unpowered According to ISO10605.2008</li> </ul>		8.0		
	+ 2.0 k $\Omega$ / 330 pF Powered According to ISO10605.2008		6.0		

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) ( $C_{ZAP}$  = 100 pF,  $R_{ZAP}$  = 1500  $\Omega$ ), the Machine Model (MM) ( $C_{ZAP}$  = 200 pF,  $R_{ZAP}$  = 0  $\Omega$ ), and the Charge Device Model.

## 3.4 Thermal Characteristics

#### Table 4. Thermal Ratings

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
HERMAL RA	TINGS	1		1	
	Operating Temperature			°C	
T <sub>A</sub>	Ambient	-40	125		
TJ	Junction	-40	150		
T <sub>STG</sub>	Storage Temperature	-55	150	°C	
T <sub>PPRT</sub>	Peak Package Reflow Temperature During Reflow	-	_	°C	
HERMAL RE	SISTANCE AND PACKAGE DISSIPATION RATINGS				
$R_{\ThetaJA}$	Junction-to-Ambient, Natural Convection, Single-Layer Board	-	140	°C/W	
T <sub>SD</sub>	Thermal Shutdown	150	_	°C	
T <sub>SDH</sub>	Thermal Shutdown Hysteresis	-	15	°C	

## 3.5 Operating Conditions

This section describes the operating conditions of the device. Conditions apply to all the following data, unless otherwise noted.

#### Table 5. Operating Conditions

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min	Max	Unit	Notes
V <sub>DD_F</sub>	Functional operating V <sub>DD</sub> voltage	V <sub>DD_UV</sub>	7.0	V	
V <sub>DD_OP</sub>	Parametric operating V <sub>DD</sub> voltage	4.5	5.5	V	
V <sub>IO_F</sub>	Functional operating V <sub>IO</sub> voltage	V <sub>IO_UV</sub>	7.0	V	
V <sub>IO_OP</sub>	Parametric operating V <sub>IO</sub> voltage	2.8	5.5	V	

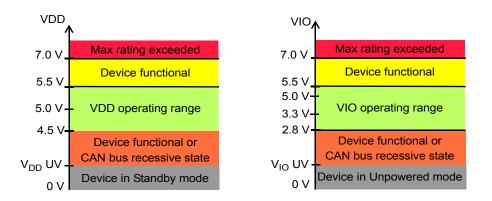


Figure 3. Supply Voltage Operating Range

## 4 General IC Functional Description and Application Information

## 4.1 Introduction

The 33901/34901 are high speed CAN transceivers providing the physical interface between the CAN protocol controller of an MCU and the physical dual wires CAN bus. They are packaged in an 8 pin SOIC with market standard pin out, and offer excellent EMC and ESD performance without the need for external filter components. They meet the ISO 11898-2 and ISO11898-5 standards, and have low leakage on CAN bus while unpowered.

The devices are supplied from VDD and VIO, to allow automatic operation with 5.0 and 3.3 V microcontrollers. They are offered in four versions: with and without CAN bus wake-up, and with and without TXD dominant time out.

## 4.2 Pin Function and Description

## 4.2.1 VDD Power Supply

This is the supply for the CANH and CANL bus drivers, the bus differential receiver and the bus biasing voltage circuitry. VDD is monitored for under voltage conditions. See Fail-safe Mechanisms.

When the device is in standby mode, the consumption on VDD is extremely low (Refer to IVDD).

## 4.2.2 VIO Digital I/O Power Supply

This is the supply for the TXD, RXD, and STB digital input outputs pins. VIO also supplies the low power differential wake-up receivers and filter circuitry. This allows detecting and reporting bus wake-up events with device supplied only from VIO. VIO is monitored for undervoltage conditions. See Fail-safe Mechanisms.

When the device is in Standby mode, the consumption on VIO is extremely low (Refer to IVIO).

### 4.2.3 STB

STB is the input pin to control the device mode. When STB is high or floating, the device is in Standby mode. When STB is low, the device is set in Normal mode. STB has an internal pull-up to VIO, so if STB is left open, the device is set to a predetermined Standby mode.

## 4.2.4 TXD

TXD is the device input pin to control the CAN bus level. In the application, this pin is connected to the microcontroller transmit terminal.

In Normal mode, when TXD is high or floating, the CANH and CANL drivers are OFF, setting the bus in a recessive state.

When TXD is low, the CANH and CANL drivers are activated and the bus is set to a dominant state. TXD has a built-in timing protection that disables the bus when TXD is dominant for more than  $tX_{DOM}$ .

In Standby mode, TXD has no effect on the device.

The TXD dominant protection is available on 33901, but not available on 34901.

## 4.2.5 RXD

RXD is the bus output level report pin. In the application, this pin is connected to the microcontroller receive terminal. In Normal mode, RXD is a push-pull structure. When the bus is in a recessive state, RXD is high. When the bus is dominant, RXD is low.

In Standby mode, the push-pull structure is disabled, RXD is pulled up to VIO via a resistor ( $R_{PU-RXD}$ ), and is in a high level. When the bus wake-up is detected, the push-pull structure resumes and TXD reports a wake-up via a toggling mechanism (refer to Figure 7). The toggling mechanism for bus wake-up reports is available on the MC33901WEF. This mechanism is not available on the MC33901SEF.

### 4.2.6 CANH and CANL

These are the CAN bus terminals.

CANL is a low side driver to GND, and CANH is a high side driver to VDD. In Normal mode and TXD high, the CANH and CANL drivers are OFF, and the voltage at CANH and CANL is approx. 2.5 V, provided by the internal bus biasing circuitry.

When TXD is low, CANL is pulled to GND and CANH to VDD, creating a differential voltage on the CAN bus.

In Standby mode, CANH and CANL drivers are OFF, and these pins are pulled down to GND via the device R<sub>IN</sub> resistor for the MC3x901WEF versions (ref to parameter Input resistance). In device unpowered mode, CANH and CANL are high-impedance with extremely low leakage to GND, making the device ideally passive when unpowered.

CANH and CANL have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. These pins have current limitation and thermal protection.

## 4.3 Operating Modes

The device has two operating modes: Standby and Normal.

### 4.3.1 Normal Mode

This mode is selected when the STB pin is low. In this mode, the device is able to transmit information from TXD to the bus and report the bus level to the RXD pin.

When TXD is high, CANH and CANL drivers are off and the bus is in the recessive state (unless it is in an application where another device drives the bus to the dominant state).

When TXD is low, CANH and CANL drivers are ON and the bus is in the dominant state.

### 4.3.2 Standby Mode

This mode is selected when the STB pin is high or floating. In this mode, the device is not able to transmit information from TXD to the bus, and it cannot report accurate bus information. The Device can only report bus wake up events via the RXD toggling mechanism.

The bus wake-up report is available on the MC3x901WEF. This feature is not available on the MC3x901SEF.

In Standby mode, the consumption from VDD and VIO is extremely low. In this mode, the CANH and CANL pins are pulled down to GND via the internal R<sub>IN</sub> resistor, for device versions MC33901WEF and MC34901WEF.

### 4.3.2.1 Wake-up Mechanism

The device versions MC3x901WEF include bus monitoring circuitry to detect and report bus wake-ups. To activate a wake-up report, three events must occur on the CAN bus:

- event 1: a dominant level for a time longer than t<sub>WU FLT1</sub> followed by

- event 2: a recessive level (event 2) longer than t<sub>WU FLT2</sub> followed by

- event 3: a dominant level (event 3) longer than t<sub>WU FLT2</sub>.

The RXD terminal will then report the bus state (bus dominant => RXD low, bus recessive => RXD high). The delay between bus dominant and RXD low, and bus recessive and RXD high is longer than in Normal mode (refer to  $t_{TGLT}$ ).

The three events must occur within the  $t_{WU}$  TO timeout.

Figure 7 "Wake-up Pattern Timing Illustration" illustrates the wake-up detection and reporting (toggling) mechanism.

If the three events do not occur within the  $T_{WU_TO}$  timeout, the wake-up and toggling mechanism are not active. This is illustrated in <u>Figure 8</u>.

The three events and the timeout function avoid a permanent dominant state on the bus that would generate a permanent wakeup situation, which would prevent the system from entering low power mode.

### 4.3.3 Unpowered Mode

When VIO is below VIO UV, the device is in unpowered mode. The CAN bus will be in high-impedance and the device is not able to transmit, receive, or report bus wake-up events.

## 4.4 Fail-safe Mechanisms

The device implements various protection, detection, and predictable fail-safe mechanisms.

### 4.4.1 STB and TXD Input Pins

The STB input pin has an internal integrated pull-up structure to the VIO supply pin. If STB is open, the device is set to Standby mode to ensure predictable behavior and minimize system current consumption.

The TXD input pin also has an internal integrated pull-up structure to the VIO supply pin. If TXD is open, the CAN driver is set to the recessive state to minimize current consumption and ensure that no false dominant bit is transmitted on the bus.

## 4.4.2 TXD Dominant Time Out Detection

If TXD is set low for a time longer than the  $tx_{DOM}$  parameter, the CAN drivers are disabled and the CAN bus will return to recessive state. This prevents the bus from being set to the dominant state permanently in case a fault sets the TXD input to low level permanently.

The device will recover from this when a high level is detected on TXD.

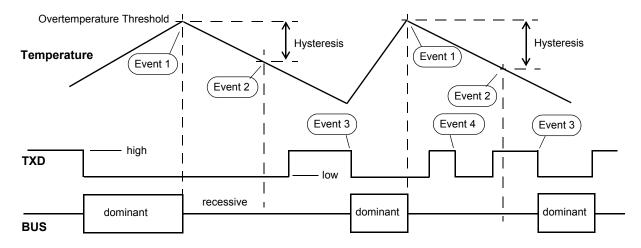
### Refer to Figures 9.

### 4.4.3 CAN Current Limitation

The current flowing in and out of the CANH and CANL driver is limited to a maximum of 100 mA, in case of a short-circuit (parameter for I<sub>LIM</sub>).

### 4.4.4 CAN Overtemperature

If the driver temperature exceeds TSD, the driver will be turned off to protect the device. A hysteresis is implemented in this protection feature. The device overtemperature and recovery conditions are shown in Overtemperature behavior. The driver remains disabled until the temperature has fallen below the OT threshold minus the hysteresis and a TXD high to low transition is detected.



Event 1: overtemperature detection. CAN driver disable.

Event 2: temperature falls below "overtemp. threshold minus hysteresis" => CAN driver remains disable.

Event 3: temperature below "overtemp. threshold minus hysteresis" and TxD high to low transition => CAN driver enable.

Event 4: temperature above "overtemp. threshold minus hysteresis" and TxD high to low transition => CAN driver remains disable.

#### Figure 4. Overtemperature behavior

## 4.4.5 VDD and VIO Supply Voltage Monitoring

The device monitors the VDD and VIO supply inputs.

If VDD falls below VDD UV (VDD\_UV), the device is set in Standby mode. This ensures a predictable behavior due to the loss of VDD. CAN driver, receiver, or bus biasing cannot operate any longer. In this case, the bus wake-up is available as VIO remains active.

If VIO falls below VIO UV (VIO\_UV), the device is set to an unpowered condition. This ensures a predictable behavior due to the loss of VIO, CAN driver, receiver, or bus biasing can not operate any longer. This sets the bus in high-impedance and in ideal passive behavior.

### 4.4.6 Bus Dominant State Behavior in Standby Mode

In device Standby mode, a bus dominant condition due, for instance to a short-circuit or a fault in one of the other CAN nodes, will not generate a permanent wake-up event, by virtue of the multiple events (dominant, recessive, dominant) and timeout required to detect and report bus wake-ups.

## 4.5 Device operation summary

The following table summarizes the device operation and the state of the input output pins, depending on the operating mode and power supply conditions.

#### STANDBY and NORMAL MODES

MODE	Description	VDD range	VIO range	STB	ТХД	RXD	CAN	Wake-up
Normal	Nominal supply and normal mode	from 4.5 to 5.5 V	from 2.8 to 5.5 V	Low	TXD High => bus recessive TXD Low => bus dominant	Report CAN state (bus recessive => RXD high, bus dominant => RXD low).	CANH and CANL drivers controlled by TXD input. Differential receiver report bus state on RXD pins. Biasing circuitry provides approx 2.5 in recessive state.	Disabled
Standby	Nominal supply and standby mode	from 0 to 5.5 V	from 2.8 to 5.5 V	High or floating	No effect. on CAN bus.	Report bus wake up via toggling mechanism for MC3x901WEF. RXD High level for MC3x901SEF	CAN driver and differential receiver disabled. Bus biased to GND via internal R <sub>IN</sub> resistors for MC3x901WEF. Bus high-impedance for MC3x901SEF.	Enabled on MC33901WEF Not available on MC33901SEF

#### UNDERVOLTAGE and LOSS OF POWER CONDITIONS

MODE	Description	VDD range	VIO range	STB	тхр	RXD	CAN	Wake up
Standby due to VDD loss	Device in standby mode due to loss of VDD (VDD fall below VDD UV)		from 2.8 to 5.5 V (5)	X (3)	x	Report bus wake up via toggling mechanism for MC3x901WEF. RXD High level for MC3x901SEF	CAN driver and differential receiver disabled. Bus biased to GND via internal R <sub>IN</sub> resistors for MC3x901WEF. Bus high-impedance for MC3x901SEF.	Enabled on MC33901WEF Not available on MC33901SEF.
Unpowered due to VIO loss	Device in unpowered state due to low VIO. CAN bus high- impedance.	(4)	from 0 to VIO_UV	X	Х	Pulled up to VIO down to VIO approx 1.5 V.	CAN driver and differential receiver disabled. High-impedance, with ideal passive behavior.	Not available.

Notes

3. STB pin has no effect. Device enters in standby mode.

4. VDD consumption < 10 uA down to VDD approx 1.5 V.

5. VIO consumption < 10 uA down to VIO approx 1.5 V. If STB is high or floating.

## 4.6 Electrical Chatacteristics

#### Table 6. Static Electrical Characteristics

Characteristics noted under conditions 4.5 V  $\leq$  V<sub>DD</sub>  $\leq$  5.5 V, 2.8 V  $\leq$  V<sub>IO</sub>  $\leq$  5.5 V, -40 °C  $\leq$  T<sub>A</sub>  $\leq$  125 °C, GND = 0 V, R on CAN bus (R<sub>L</sub>) = 60  $\Omega$ , unless otherwise noted. Typical values noted reflect the approximate parameter at T<sub>A</sub> = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Тур	Max	Unit	Notes
	UT VDD	I				
V <sub>DD</sub>	VDD Supply Voltage Range				V	
22	Nominal Operation	4.5	-	5.5		
V <sub>DD_UV</sub>	VDD Under voltage threshold	3.0	_	4.5	V	
I <sub>VDD</sub>	VDD supply current					
100	Normal mode, TXD High	_	_	5.0	mA	
	Normal mode, TX Low	_	40	65	mA	
	Standby mode	-	-	5.0	μA	
	JT VIO					
V <sub>IO</sub>	Vio Supply Voltage Range				V	
10	Nominal Operation	2.8	_	5.5		
V <sub>IO_UV</sub>	V <sub>IO</sub> Under voltage threshold	_	-	2.8	V	1
I <sub>VIO</sub>	VIO supply current					
	Normal mode, TXD high	_	_	200	μA	
	<ul> <li>Normal mode, TXD low or CAN bus in dominant state</li> </ul>	-	_	1.0	mA	
	<ul> <li>Standby mode, CAN bus in recessive state</li> </ul>	-	5	10	μA	
	Standby mode, wake-up filter and wake-up time out running	-	_	150	μA	
STB INPUT	•	Į		Į	_	
V <sub>STB</sub>	Input voltages					
	High level Input Voltage	0.7	_	-	VIO	
	Low level input voltage	-	-	0.3	V	
	Input threshold hysteresis	200	-	-	mV	
R <sub>PU-STB</sub>	Pull-up resistor to V <sub>IO</sub>	-	100	-	kΩ	
XD INPUT		•			1	
V <sub>TXD</sub>	Input voltages					
	High level Input Voltage	0.7	_	_	VIO	
	Low level input voltage	_	_	0.3	V	
	Input threshold hysteresis	200	300	-	mV	
R <sub>PU-TXD</sub>	Pull-up resistor to V <sub>IO</sub>	5.0	_	50	kΩ	
RXD OUTPU	T			1		
I <sub>RXD</sub>	Output current				mA	
	• RXD high, VRXD high = VIO - 0.4 V	-5.0	-2.5	-1.0		
	• RXD low, VRXD high = 0.4 V	1.0	2.5	5.0		
R <sub>PU-RXD</sub>	Pull-up resistor to $V_{IO}$ (in standby mode, without toggling - no wake-up report)	25	50	90	kΩ	

#### Table 6. Static Electrical Characteristics

Characteristics noted under conditions 4.5 V  $\leq$  V<sub>DD</sub>  $\leq$  5.5 V, 2.8 V  $\leq$  V<sub>IO</sub>  $\leq$  5.5 V, -40 °C  $\leq$  T<sub>A</sub>  $\leq$  125 °C, GND = 0 V, R on CAN bus (R<sub>L</sub>) = 60  $\Omega$ , unless otherwise noted. Typical values noted reflect the approximate parameter at T<sub>A</sub> = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Тур	Max	Unit	Notes
CANL and CA	NH TERMINALS	I				
V <sub>REC</sub>	Recessive voltage, TXD high, no load				V	Τ
	CANL recessive voltage	2.0	2.5	3.0		
	CANH recessive voltage	2.0	2.5	3.0		
V <sub>DIFF_REC</sub>	CANH - CANL differential recessive voltage, TXD high, no load	-50	_	50	mV	
V <sub>DOM</sub>	Dominant voltage, TXD low (t < TX <sub>DOM</sub> ), R <sub>L</sub> = 45 to 65 $\Omega$				V	
	CANL dominant voltage	0.5	-	2.25		
	CANH dominant voltage	2.75	-	4.5		
$V_{DIFF_DOM}$	CANH - CANL differential dominant voltage, R <sub>L</sub> = 45 to 65 $\Omega$ , TxD <sub>LOW</sub>	1.5	2.0	3.0	V	
I <sub>LIM</sub>	Current limitation, TXD low (t < TX <sub>DOM</sub> )				mA	
	<ul> <li>CANL current limitation, CANL 5V to 28V</li> </ul>	40	-	100		
	<ul> <li>CANH current limitation, CANH = 0V</li> </ul>	-100	-	-40		
V <sub>DIFF_THR</sub>	CANH - CANL Differential input threshold	0.5	-	0.9	V	
V <sub>DIFF_HYS</sub>	CANH - CANL Differential input voltage hysteresis	50	_	400	mV	
V <sub>DIFF_THR_S</sub>	CANH - CANL Differential input threshold, in standby mode	0.4	_	1.15	V	
V <sub>CM</sub>	Common Mode Voltage	-12	-	12	V	
R <sub>IN</sub>	Input resistance				k	
	CANL input resistance	5	-	50		
	CANH input resistance	5	-	50		
R <sub>IN_DIFF</sub>	CANH, CANL differential input resistance	10	_	100	kΩ	
R <sub>IN_MATCH</sub>	Input resistance matching	-3.0	-	3.0	%	
I <sub>IN_UPWR</sub>	CANL or CANH input current, device unpowered, VDD = VIO = 0 V, VCANL and VCANH 0.0 to 5.0 V range	-10	_	10	μA	
R <sub>IN_UPWR</sub>	CANL, CANH input resistance, VCANL = VCANH = $\pm$ 12 V	10	_	_	kΩ	
C <sub>CAN_CAP</sub>	CANL, CANH input capacitance (guaranteed by design and characterization)	_	20	-	pF	
C <sub>DIF_CAP</sub>	CANL, CANH differential input capacitance (guaranteed by design and characterization)	-	10	-	pF	
TSD	Temperature shutdown	150	185	-	°C	

### Table 7. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V  $\leq$  V<sub>DD</sub>  $\leq$  5.5 V, 2.8 V  $\leq$  V<sub>IO</sub>  $\leq$  5.5 V, -40 °C  $\leq$  T<sub>A</sub>  $\leq$  125 °C, GND = 0 V, R on CAN bus (R<sub>L</sub>) = 60  $\Omega$ , unless otherwise noted. Typical values noted reflect the approximate parameter at T<sub>A</sub> = 25 °C under nominal conditions, unless otherwise noted.

#### TIMING PARAMETERS

tX <sub>DOM</sub>	TXD DOM	2.5	-	16	ms	(6)
t <sub>LOOP</sub>	Т Іоор	-	-	255	ns	
t <sub>WU_FLT1</sub>	TWU filter1	0.5	_	5	μs	(7)
t <sub>WU_FLT2</sub>	TWU filter2	0.08	-	1	μs	(7)
t <sub>TGLT</sub>	Tdelay during toggling	-	-	1.3	μs	(7)
t <sub>wu_то</sub>	Twake up time out	1.5	_	7.0	ms	(7)
t <sub>DELAY_PWR</sub>	Delay between power up and device ready	_	120	300	μs	
t <sub>DELAY_SN</sub>	Transition time from standby to normal mode (STB high to low)			40	us	

Notes

6. MC33901 versions only

7. MC33901WEF and MC34901WEF versions only

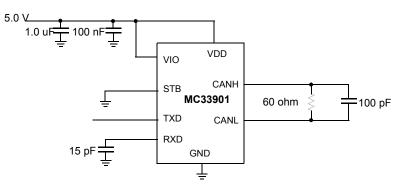


Figure 5. Timing Test Circuit

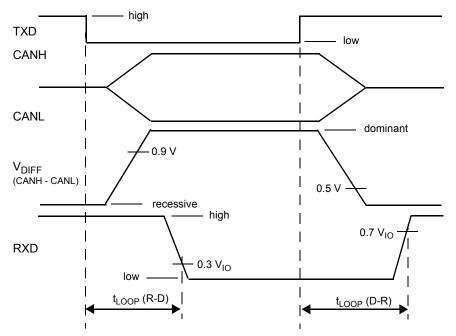


Figure 6. CAN Timing Diagram

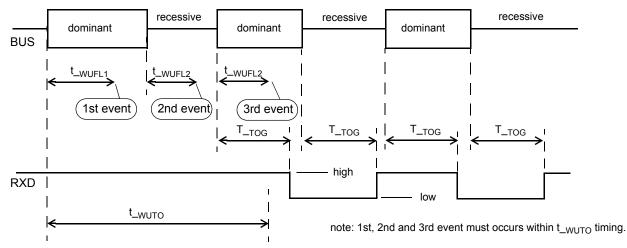
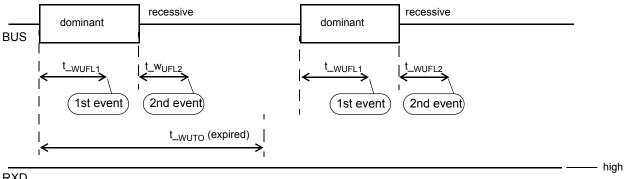
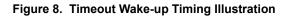


Figure 7. Wake-up Pattern Timing Illustration





note: only the 1st and the 2nd event occurred within  $t_{\_WUTO}$  timing.



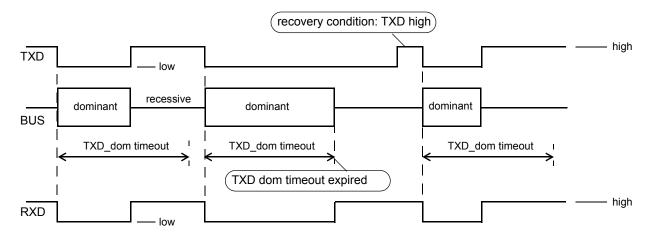


Figure 9. TXD Dominant Timeout Detection Illustration

# 5 Typical Applications

## 5.1 Application Diagrams

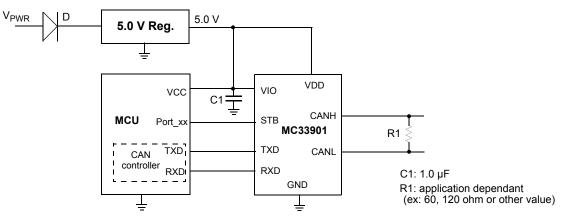
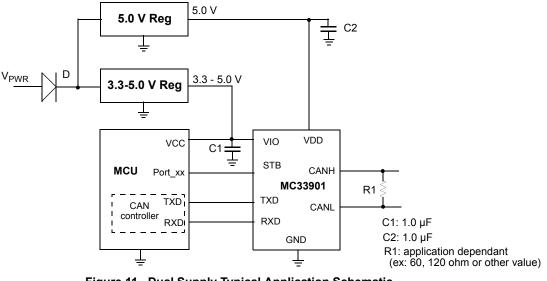
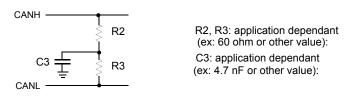


Figure 10. Single Supply Typical Application Schematic









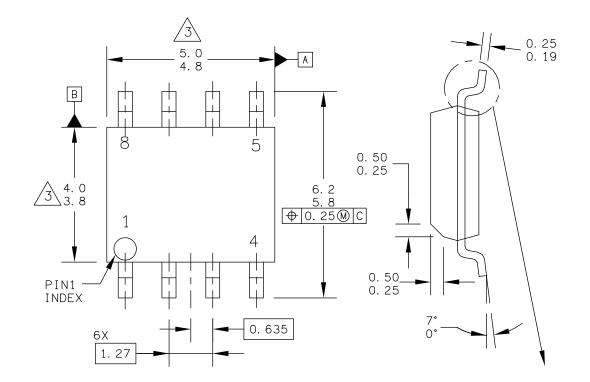
# 6 Packaging

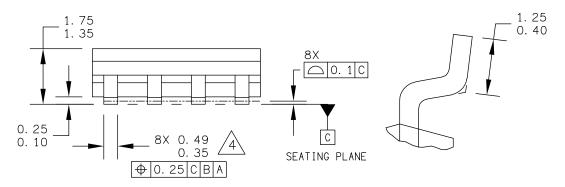
## 6.1 Package Mechanical Dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

### Table 8. Packaging Information

Package	Suffix	Package Outline Drawing Number
8-Pin SOICN	EF	98ASB42564B





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TITLE:		DOCUMENT NO	: 98ASB42564B	REV: V
8LD SOIC NARROW BODY		CASE NUMBER	2: 751–07	20 NOV 2007
		STANDARD: JE	DEC MS-012AA	

EF SUFFIX 8-PIN SOICN 98ASB42564B ISSUE V NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- A DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- A DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

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TITLE:		DOCUMENT NO	): 98ASB42564B	REV: V
8LD SOIC NARROW	I BODY	CASE NUMBER	8: 751–07	20 NOV 2007
		STANDARD: JE	DEC MS-012AA	

EF SUFFIX 8-PIN SOICN 98ASB42564B ISSUE V

# 7 Revision History

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	12/2013	Initial release



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