Freescale Semiconductor
Technical Data

Document Number: MMRF1005H
Rev. 0, 12/2013

√RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MMRF1005HR5
MMRF1005HSR5

RF power transistors designed for CW and pulse applications operating at 1300 MHz. These devices are suitable for use in defense and commercial CW and pulse applications, such as DME/IFF systems.

- Typical Pulse Performance: V_{DD} = 50 Vdc, I_{DQ} = 100 mA

Signal Type	P_{out} (W)	f (MHz)	G_{ps} (dB)	η_D (%)	IRL (dB)
Pulse (200 μsec, 10% Duty Cycle)	250 Peak	1300	22.7	57.0	-18

- Typical CW Performance: V_{DD} = 50 Vdc, I_{DQ} = 10 mA, T_C = 61°C

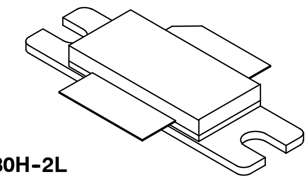
Signal Type	P_{out} (W)	f (MHz)	G_{ps} (dB)	η_D (%)	IRL (dB)
CW	230 CW	1300	20.0	53.0	-25

- Capable of Handling a Load Mismatch of 10:1 VSWR, @ 50 Vdc, 1300 MHz at all Phase Angles, 250 W Pulse Peak Power, 10% Duty Cycle, 200 μsec

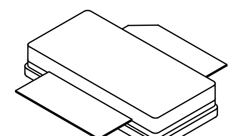
Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 50 V_{DD} Operation
- Characterized from 20 V to 50 V for Extended Power Range
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- In Tape and Reel. R5 Suffix = 50 Units, 56 mm Tape Width, 13-inch Reel.

1300 MHz, 250 W, 50 V
LATERAL N-CHANNEL
RF POWER MOSFETs



NI-780H-2L
MMRF1005HR5



NI-780S-2L
MMRF1005HSR5

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +120	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1)	T_J	225	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	476 2.38	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Pulse: Case Temperature 65°C, 250 W Peak, 200 μsec Pulse Width, 10% Duty Cycle, 50 Vdc, I_{DQ} = 100 mA, 1300 MHz CW: Case Temperature 77°C, 235 W CW, 50 Vdc, I_{DQ} = 10 mA, 1300 MHz	 $Z_{\theta JC}$ $R_{\theta JC}$	 0.07 0.42	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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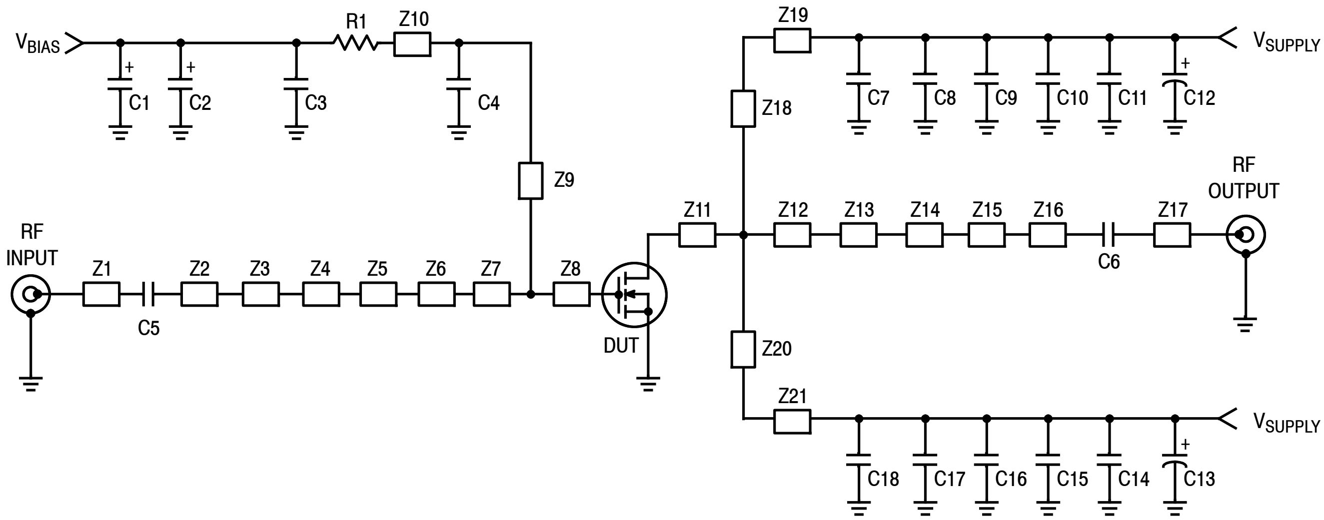
Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 50 mA)	$V_{(BR)DSS}$	120	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 90 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	20	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 640 μAdc)	$V_{GS(th)}$	1.0	1.8	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 100 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.0	2.4	3.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.58 Adc)	$V_{DS(on)}$	0.1	0.25	0.3	Vdc
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.2	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	58	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	340	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100 mA, P_{out} = 250 W Peak (25 W Avg.), f = 1300 MHz Pulse, 200 μsec Pulse Width, 10% Duty Cycle					
Power Gain	G_{ps}	21.5	22.7	24.0	dB
Drain Efficiency	η_D	53.5	57.0	—	%
Input Return Loss	IRL	—	-18	-9	dB
Typical CW Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 10 mA, P_{out} = 230 W CW, f = 1300 MHz, T_C = 61°C					
Power Gain	G_{ps}	—	20.0	—	dB
Drain Efficiency	η_D	—	53.0	—	%
Input Return Loss	IRL	—	-25	—	dB
Load Mismatch (In Freescale Application Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100 mA, P_{out} = 250 W Peak (25 W Avg.), f = 1300 MHz, Pulse, 200 μsec Pulse Width, 10% Duty Cycle					
VSWR 10:1 at all Phase Angles	Ψ	No Degradation in Output Power			

1. Part internally input matched.



Z1	0.447″ x 0.063″ Microstrip	Z11	0.162″ x 1.160″ Microstrip
Z2	0.030″ x 0.084″ Microstrip	Z12	0.419″ x 1.160″ Microstrip
Z3	0.120″ x 0.063″ Microstrip	Z13	0.468″ x 0.994″ Microstrip
Z4	0.855″ x 0.293″ Microstrip	Z14	0.131″ x 0.472″ Microstrip
Z5	0.369″ x 0.825″ Microstrip	Z15	0.264″ x 0.222″ Microstrip
Z6	0.203″ x 0.516″ Microstrip	Z16	0.500″ x 0.111″ Microstrip
Z7	0.105″ x 0.530″ Microstrip	Z17	0.291″ x 0.063″ Microstrip
Z8	0.105″ x 0.530″ Microstrip	Z18, Z20	0.105″ x 0.388″ Microstrip
Z9*	0.116″ x 0.050″ Microstrip	Z19*, Z21*	0.854″ x 0.052″ Microstrip
Z10	0.122″ x 0.050″ Microstrip		

*Line length includes microstrip bends.

Figure 1. MMRF1005HR5(HSR5) Test Circuit Schematic — 1300 MHz

Table 5. MMRF1005HR5(HSR5) Test Circuit Component Designations and Values — 1300 MHz

Part	Description	Part Number	Manufacturer
C1, C2	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C3, C11, C14	0.1 μF, 50 V Chip Capacitors	CDR33BX104AKWS	AVX
C4, C6, C7, C18	100 pF Chip Capacitors	ATC800B101JT500XT	ATC
C5	4.7 pF Chip Capacitor	ATC100B4R7CT500XT	ATC
C8, C17	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C9, C16	1000 pF Chip Capacitors	ATC700B102FT50XT	ATC
C10, C15	10K pF Chip Capacitors	ATC200B103KT50XT	ATC
C12, C13	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1	15 Ω, 1/4 W Chip Resistor	CRCW120615R0FKEA	Vishay
PCB	0.030″, ε_r = 3.50	RO4350B	Rogers

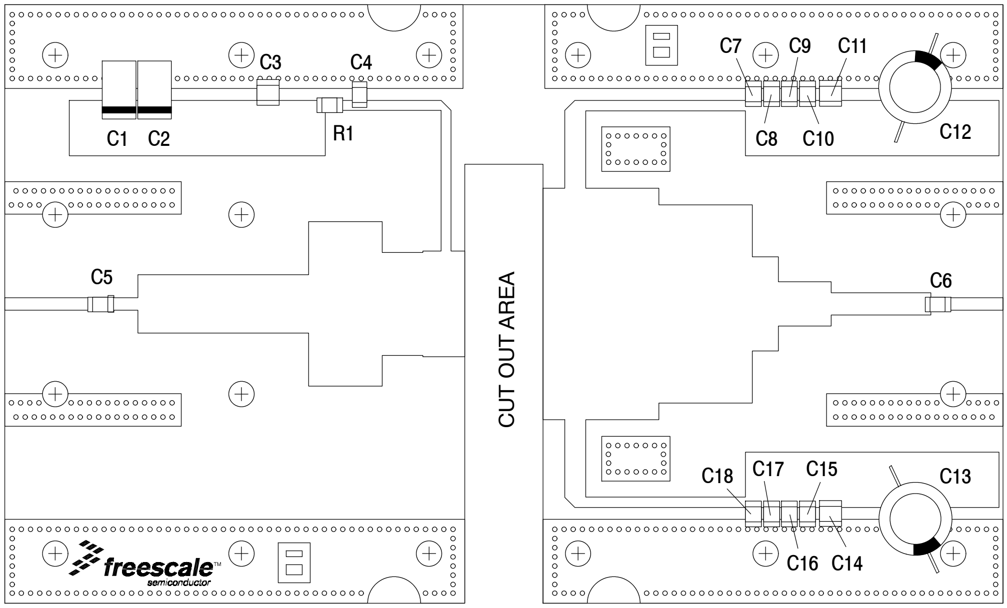


Figure 2. MMRF1005HR5(HSR5) Test Circuit Component Layout — 1300 MHz

TYPICAL CHARACTERISTICS — PULSE

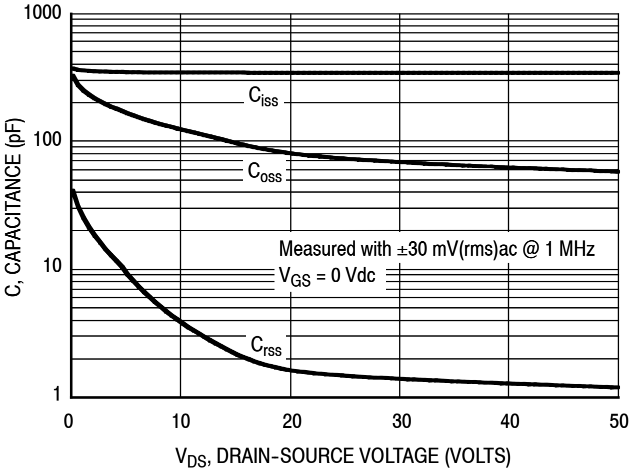


Figure 3. Capacitance versus Drain-Source Voltage

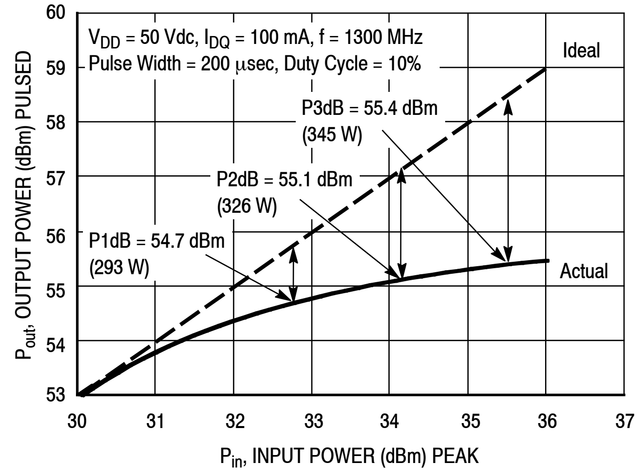


Figure 4. Output Power versus Input Power

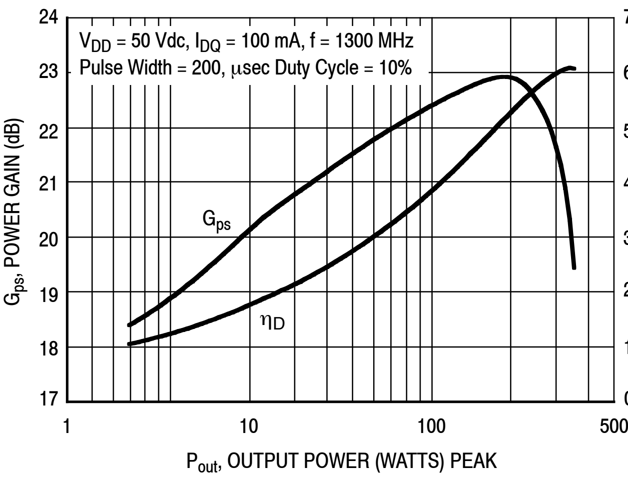


Figure 5. Power Gain and Drain Efficiency versus Output Power

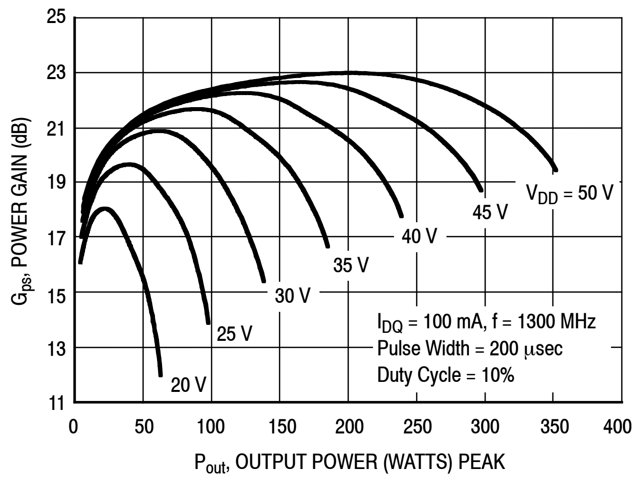


Figure 6. Power Gain versus Output Power

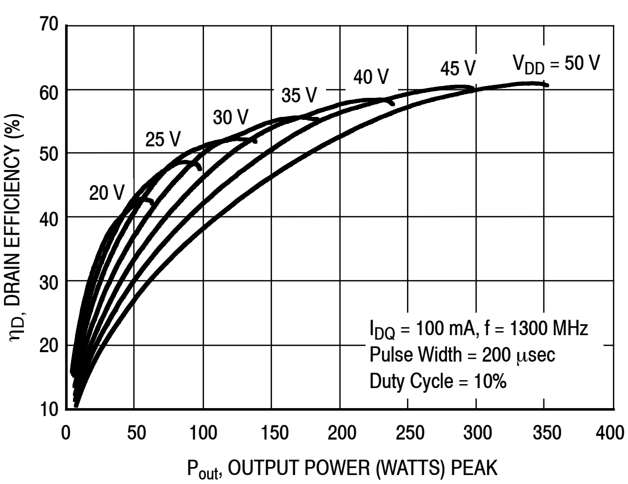


Figure 7. Efficiency versus Output Power

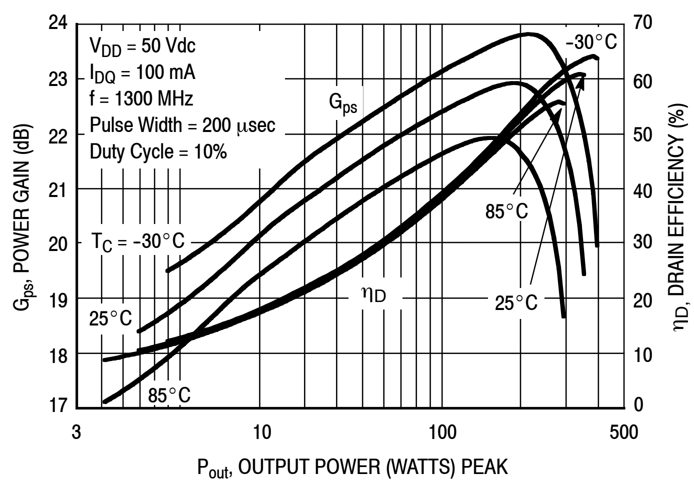
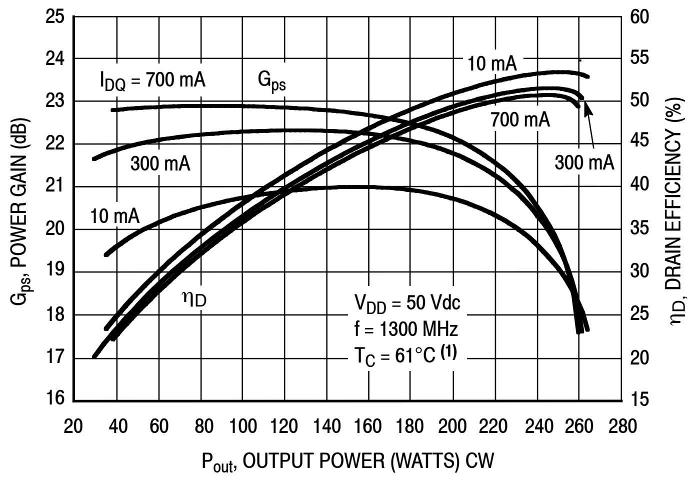


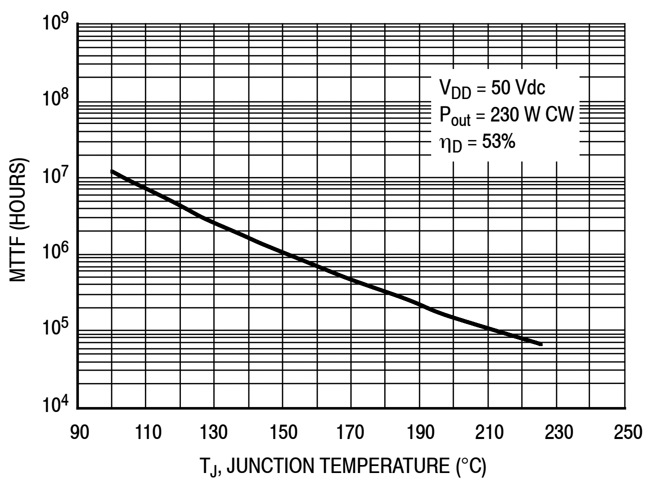
Figure 8. Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS — CW



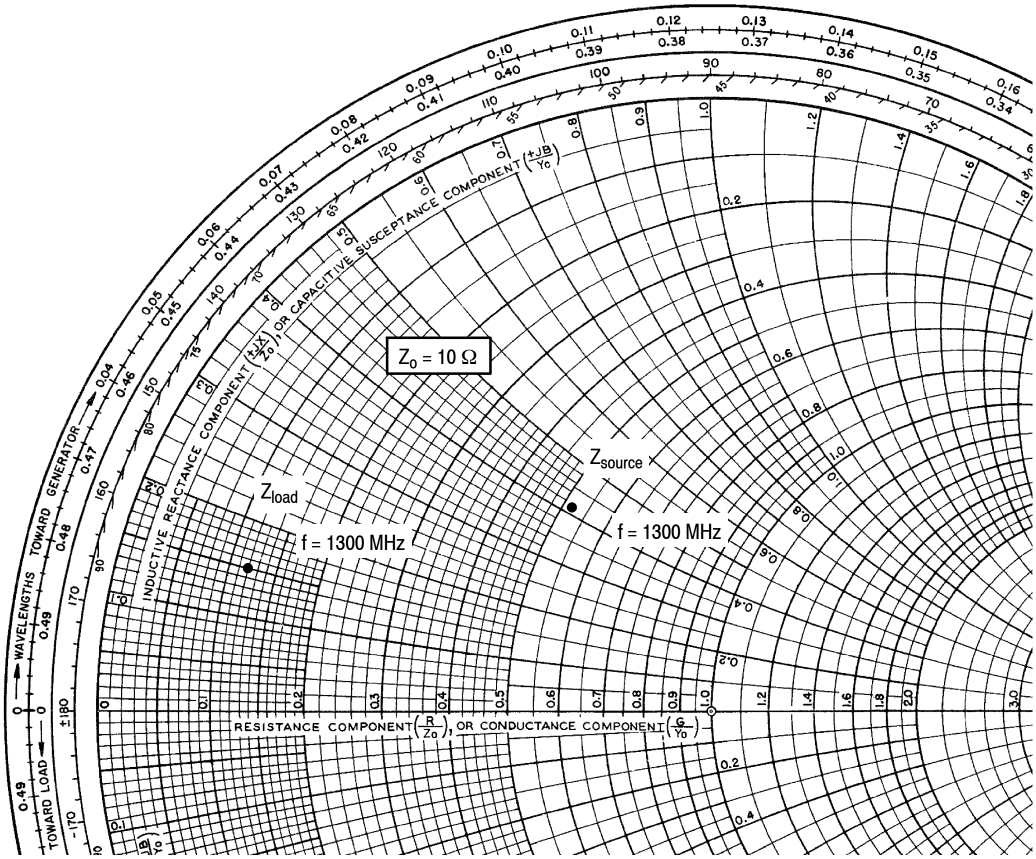
1. Data for graph was collected in a water cooled test fixture. The water inlet temperature = 25°C.

Figure 9. CW Power Gain and Drain Efficiency versus Output Power



MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 10. MTTF versus Junction Temperature — CW



V_{DD} = 50 Vdc, I_{DQ} = 100 mA, P_{out} = 250 W Peak

f MHz	Z_{source} Ω	Z_{load} Ω
1300	5.32 + j4.11	1.17 + j1.48

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

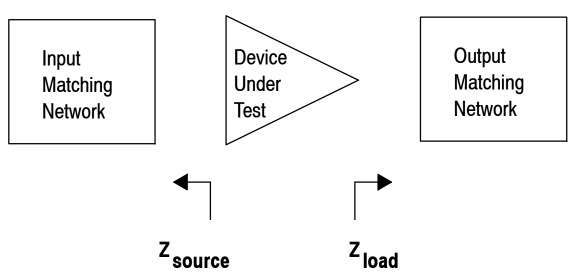
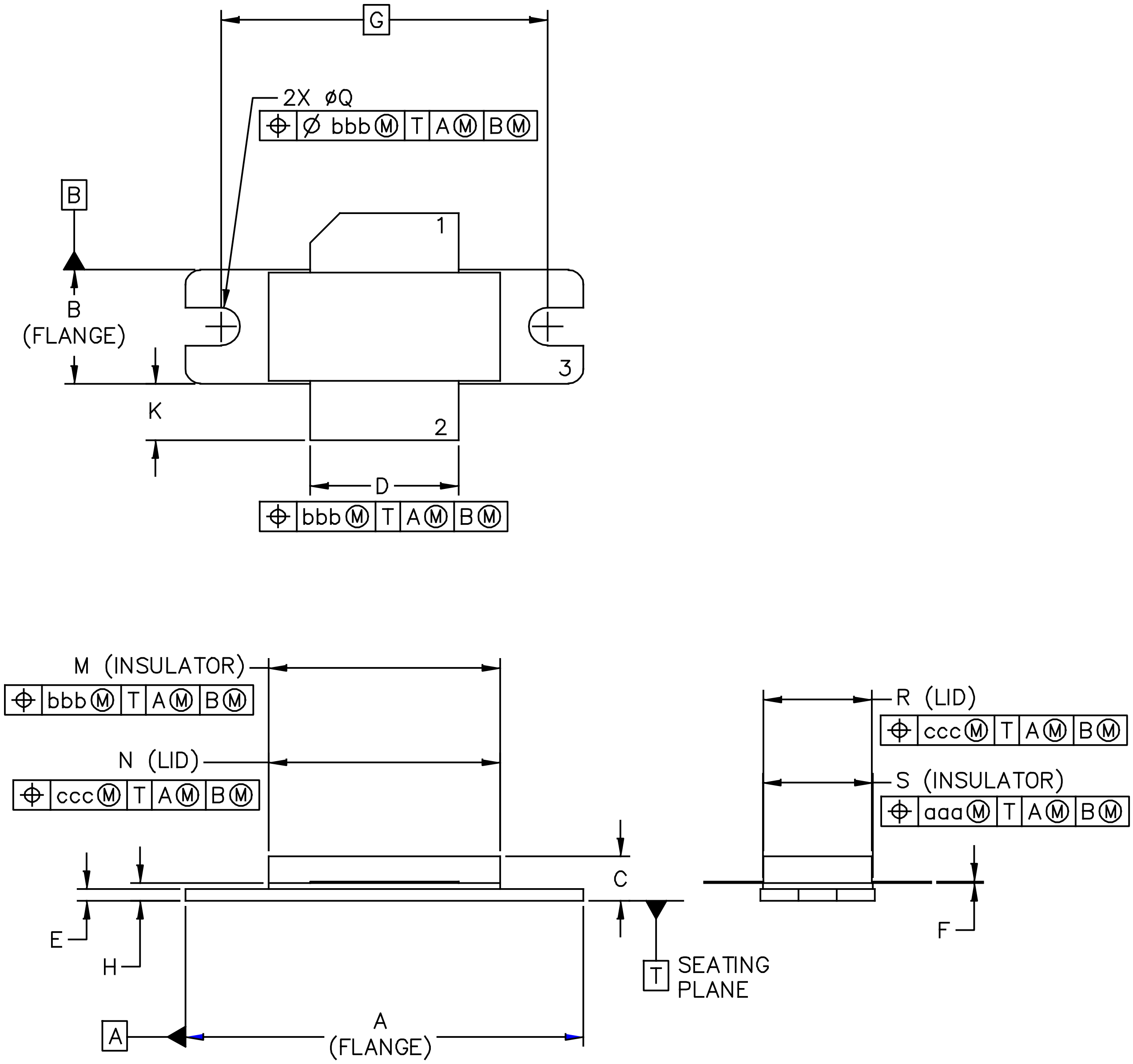


Figure 11. Series Equivalent Source and Load Impedance — Pulse



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	CASE NUMBER: 465-06		31 MAR 2005
	STANDARD: NON-JEDEC		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M—1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX	DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX
A	1.335	—	1.345	33.91	—	34.16	R	.365	—	.375	9.27	—	9.53
B	.380	—	.390	9.65	—	9.91	S	.365	—	.375	9.27	—	9.52
C	.125	—	.170	3.18	—	4.32	aaa	—	.005	—	—	0.127	—
D	.495	—	.505	12.57	—	12.83	bbb	—	.010	—	—	0.254	—
E	.035	—	.045	0.89	—	1.14	ccc	—	.015	—	—	0.381	—
F	.003	—	.006	0.08	—	0.15	—	—	—	—	—	—	—
G	1.100 BSC			27.94 BSC			—	—	—	—	—	—	—
H	.057	—	.067	1.45	—	1.7	—	—	—	—	—	—	—
K	.170	—	.210	4.32	—	5.33	—	—	—	—	—	—	—
M	.774	—	.786	19.66	—	19.96	—	—	—	—	—	—	—
N	.772	—	.788	19.6	—	20	—	—	—	—	—	—	—
Q	ø.118	—	ø.138	ø3	—	ø3.51	—	—	—	—	—	—	—

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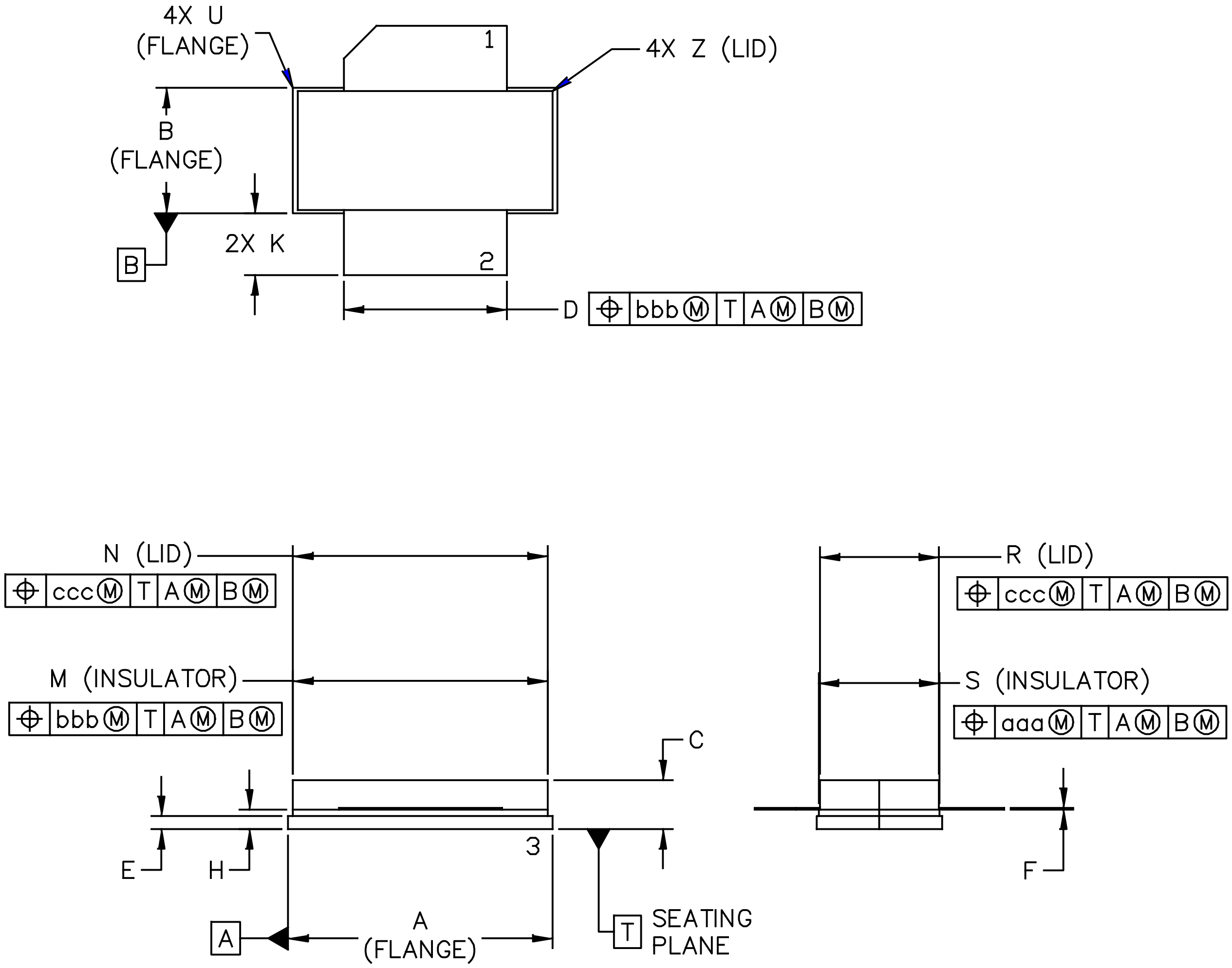

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3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX	DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX
A	.805	–	.815	20.45	–	20.7	U	–	–	.040	–	–	1.02
B	.380	–	.390	9.65	–	9.91	Z	–	–	.030	–	–	0.76
C	.125	–	.170	3.18	–	4.32	aaa	–	.005	–	–	0.127	–
D	.495	–	.505	12.57	–	12.83	bbb	–	.010	–	–	0.254	–
E	.035	–	.045	0.89	–	1.14	ccc	–	.015	–	–	0.381	–
F	.003	–	.006	0.08	–	0.15	–	–	–	–	–	–	–
H	.057	–	.067	1.45	–	1.7	–	–	–	–	–	–	–
K	.170	–	.210	4.32	–	5.33	–	–	–	–	–	–	–
M	.774	–	.786	19.61	–	20.02	–	–	–	–	–	–	–
N	.772	–	.788	19.61	–	20.02	–	–	–	–	–	–	–
R	.365	–	.375	9.27	–	9.53	–	–	–	–	–	–	–
S	.365	–	.375	9.27	–	9.52	–	–	–	–	–	–	–

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NI–780S

DOCUMENT NO: 98ASB16718C

REV: H

CASE NUMBER: 465A–06

31 MAR 2005

STANDARD: NON–JEDEC

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2013	• Initial Release of Data Sheet

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