



# RF LDMOS Wideband Integrated Power Amplifier

The MMRF2006N wideband integrated circuit is designed with on-chip matching that makes it usable from 1805 to 2170 MHz. This multi-stage structure is rated for 26 to 32 V operation and can be used in many RF amplifier modulation formats.

## Driver Application — 2100 MHz

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQ1} = 40$  mA,  $I_{DQ2} = 230$  mA,  $P_{out} = 2.4$  W Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	32.6	16.8	7.7	-51.3
2140 MHz	32.6	17.0	7.6	-51.4
2170 MHz	32.4	17.0	7.5	-51.6

- Capable of Handling 10:1 VSWR @ 32 Vdc, 2140 MHz,  $P_{out} = 33$  W CW (3 dB Input Overdrive from Rated  $P_{out}$ )
- Typical  $P_{out}$  @ 1 dB Compression Point  $\approx 20$  W CW

## Driver Application — 1800 MHz

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQ1} = 40$  mA,  $I_{DQ2} = 230$  mA,  $P_{out} = 2.4$  W Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
1805 MHz	31.8	17.4	7.6	-51.2
1840 MHz	31.8	17.4	7.7	-50.2
1880 MHz	31.8	17.4	7.7	-51.0

## Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- In Tape and Reel. T1 Suffix = 1,000 Units, 16 mm Tape Width, 13-inch Reel.

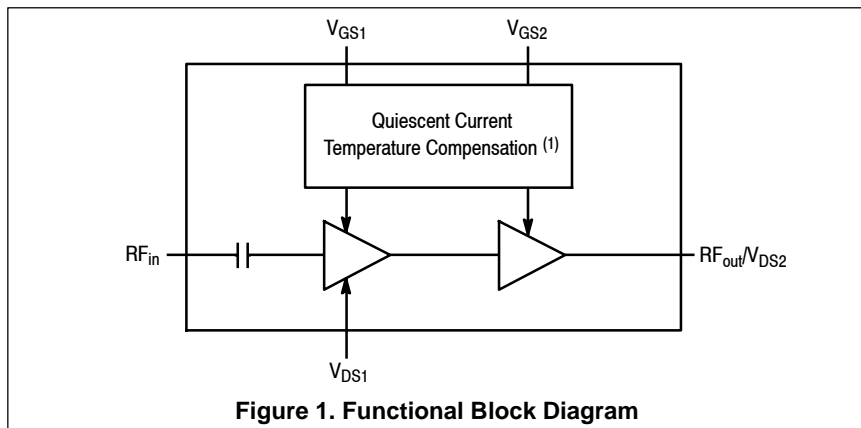


Figure 1. Functional Block Diagram

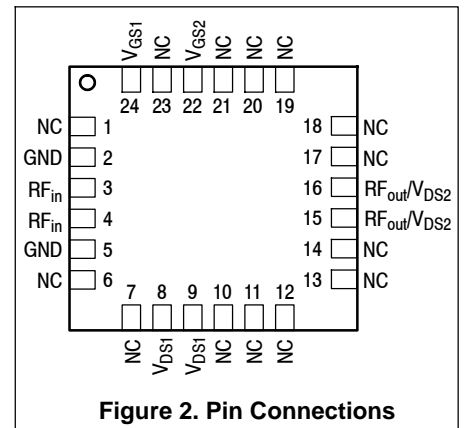
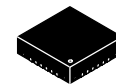


Figure 2. Pin Connections

1. Refer to AN1977, Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family, and to AN1987, Quiescent Current Control for the RF Integrated Circuit Device Family. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

MMRF2006NT1

1805-2170 MHz, 20 W CW, 28 V  
 RF LDMOS WIDEBAND  
 INTEGRATED POWER AMPLIFIER



PQFN 8 x 8  
 PLASTIC

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Operating Junction Temperature (1,2)	$T_J$	150	°C
Input Power	$P_{in}$	37	dBm

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 84°C, 2.4 W CW Stage 1, 28 Vdc, $I_{DQ1}$ = 40 mA, 2140 MHz Stage 2, 28 Vdc, $I_{DQ2}$ = 230 mA, 2140 MHz	$R_{\theta JC}$	9.0	°C/W
Case Temperature 92°C, 24 W CW Stage 1, 28 Vdc, $I_{DQ1}$ = 40 mA, 2140 MHz Stage 2, 28 Vdc, $I_{DQ2}$ = 230 mA, 2140 MHz		1.9	
		8.6	
		1.6	

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 1 — Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{A}$ dc
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	1	$\mu\text{A}$ dc
Gate-Source Leakage Current ( $V_{GS} = 1.5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{A}$ dc
<b>Stage 1 — On Characteristics</b>					
Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 12$ $\mu\text{A}$ dc)	$V_{GS(th)}$	1.0	2.0	3.0	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28$ Vdc, $I_{DQ1} = 40$ mAdc)	$V_{GS(Q)}$	—	2.9	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_{DQ1} = 40$ mAdc, Measured in Functional Test)	$V_{GG(Q)}$	6.2	6.9	7.7	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 2 — Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**Stage 2 — On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 75\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.0	2.0	3.0	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ2} = 230\text{ mAdc}$ )	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ2} = 230\text{ mAdc}$ , Measured in Functional Test)	$V_{GG(Q)}$	4.7	5.5	6.2	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 0.75\text{ Adc}$ )	$V_{DS(on)}$	—	0.3	0.8	Vdc

**Functional Tests** <sup>(1)</sup> (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 40\text{ mA}$ ,  $I_{DQ2} = 230\text{ mA}$ ,  $P_{out} = 2.4\text{ W Avg.}$ ,  $f = 2140\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Power Gain	$G_{ps}$	31.0	32.6	36.0	dB
Power Added Efficiency	PAE	16.0	17.0	—	%
Adjacent Channel Power Ratio	ACPR	—	-51.4	-47.0	dBc
Input Return Loss	IRL	—	-12	-10	dB

**Typical Performance over Frequency — 2100 MHz** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 40\text{ mA}$ ,  $I_{DQ2} = 230\text{ mA}$ ,  $P_{out} = 2.4\text{ W Avg.}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Frequency	$G_{ps}$ (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	32.6	16.8	7.7	-51.3	-14
2140 MHz	32.6	17.0	7.6	-51.4	-12
2170 MHz	32.4	17.0	7.5	-51.6	-11

**Typical Performance** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 40\text{ mA}$ ,  $I_{DQ2} = 230\text{ mA}$ , 2110-2170 MHz Bandwidth

Characteristic	Symbol	Min	Typ	Max	Unit
$P_{out}$ @ 1 dB Compression Point, CW	$P_{1dB}$	—	20	—	W
IMD Symmetry @ 9 W PEP, $P_{out}$ where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	$IMD_{sym}$	—	25	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	90	—	MHz
Quiescent Current Accuracy over Temperature <sup>(2)</sup> with 2 k $\Omega$ Gate Feed Resistors (-30 to 85°C)	$\Delta I_{QT}$	—	0.00 3.70	—	%
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 2.4\text{ W Avg.}$	$G_F$	—	0.2	—	dB
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.045	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P_{1dB}$	—	0.004	—	dB/°C

1. Part internally input matched.

2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

(continued)

MMRF2006NT1

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) **(continued)**

**Typical Performance over Frequency — 1800 MHz** (In Freescale 1800 MHz Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 40\text{ mA}$ ,  $I_{DQ2} = 230\text{ mA}$ ,  $P_{out} = 2.4\text{ W Avg.}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Frequency	$G_{ps}$ (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	31.8	17.4	7.6	-51.2	-13
1840 MHz	31.8	17.4	7.7	-50.2	-9
1880 MHz	31.8	17.4	7.7	-51.0	-6

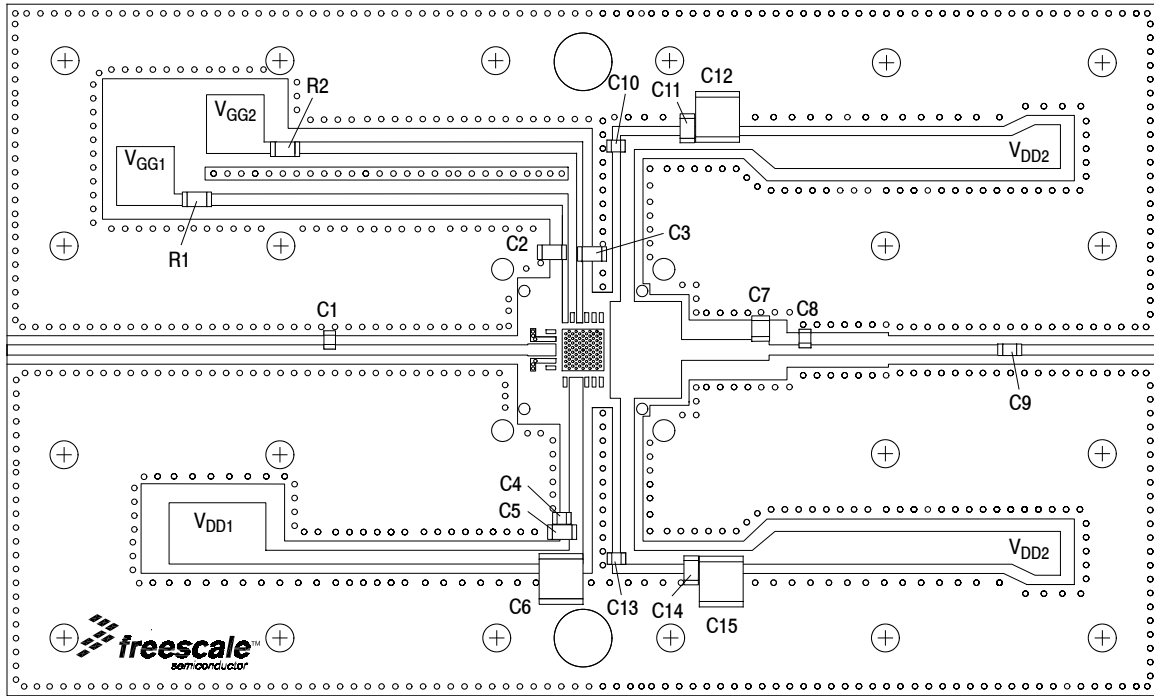


Figure 3. MMRF2006NT1 Test Circuit Component Layout

Table 6. MMRF2006NT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1.2 pF, Chip Capacitor	ATC600F1R2BT250XT	ATC
C2, C3, C11, C14	4.7 $\mu$ F, 50 V Chip Capacitors	GRM31CR71H475KA12L	Murata
C4, C9, C10, C13	33 pF Chip Capacitors	ATC600F330JT250XT	ATC
C5	1.0 $\mu$ F, 100 V Chip Capacitor	GRM31CR72A105KA01L	Murata
C6, C12, C15	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C7	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C8	0.6 pF Chip Capacitor	ATC600F0R6BT250XT	ATC
R1, R2	4.7 k $\Omega$ , 1/4 W Chip Resistors	CRCW12064K70FKEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	—	MTL

## TYPICAL CHARACTERISTICS

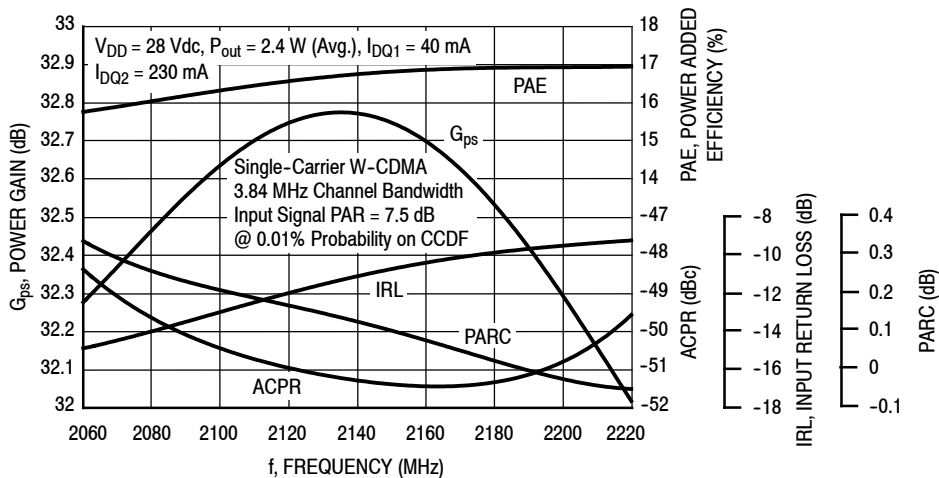


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 2.4$  Watts Avg.

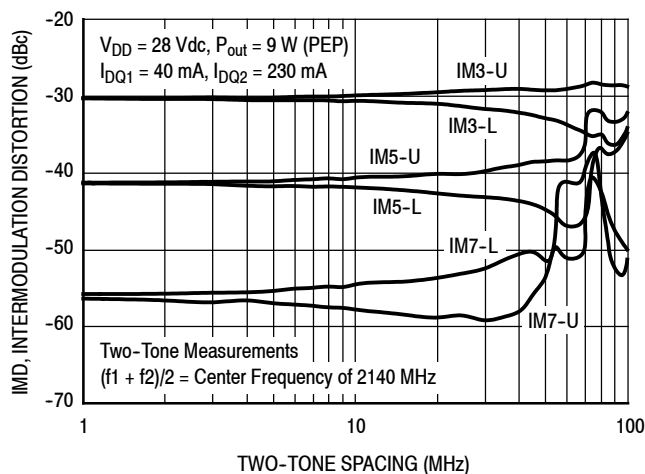


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

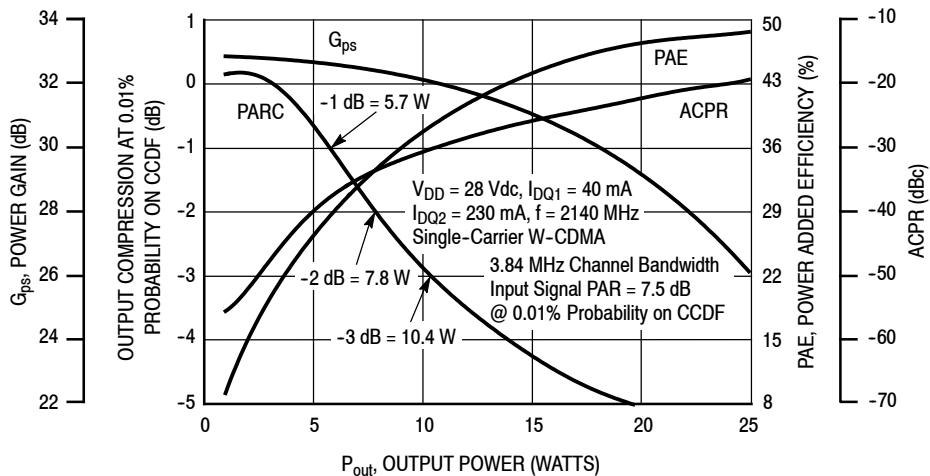


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

## TYPICAL CHARACTERISTICS

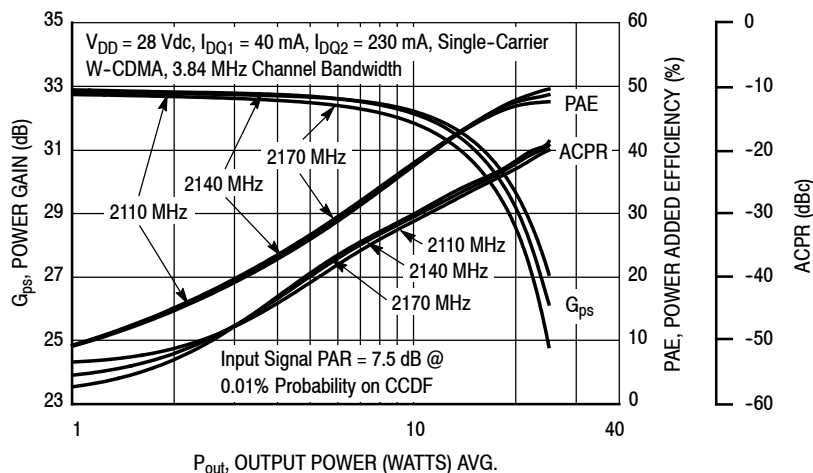


Figure 7. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

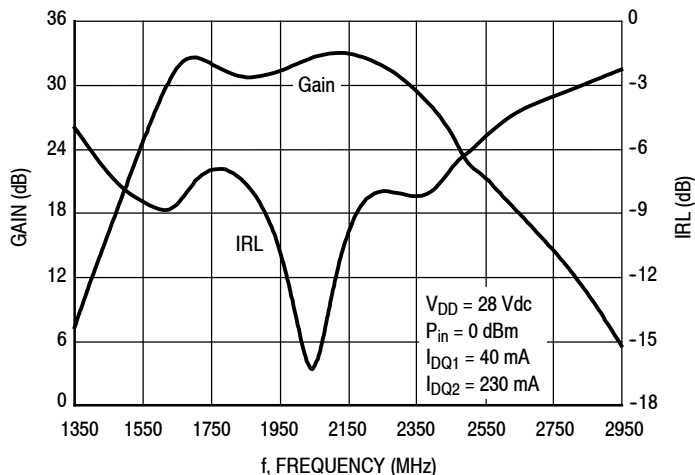
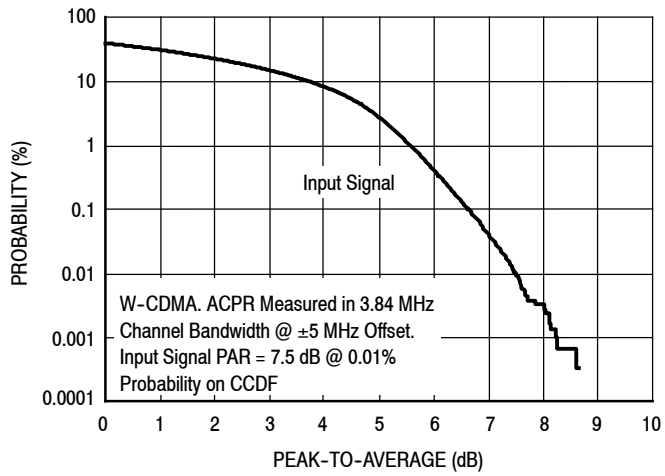
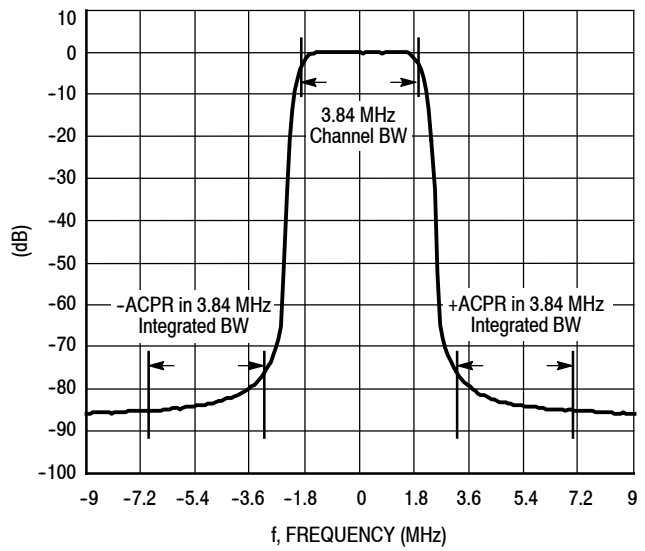


Figure 8. Broadband Frequency Response

## W-CDMA TEST SIGNAL



**Figure 9. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal**



**Figure 10. Single-Carrier W-CDMA Spectrum**

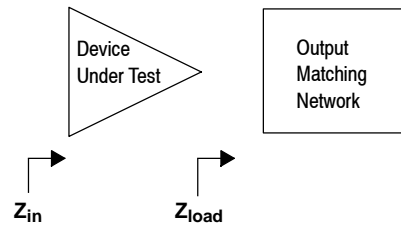


$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1} = 40 \text{ mA}$ ,  $I_{DQ2} = 230 \text{ mA}$ ,  $P_{out} = 2.4 \text{ W Avg.}$

f MHz	$Z_{in}$ $\Omega$	$Z_{load}$ $\Omega$
2060	53.3 - j50.4	7.28 - j4.02
2080	50.9 - j50.9	7.28 - j3.92
2100	47.8 - j51.0	7.28 - j3.82
2120	45.0 - j51.3	7.30 - j3.74
2140	41.7 - j51.0	7.32 - j3.68
2160	39.4 - j49.6	7.33 - j3.61
2180	37.4 - j48.5	7.35 - j3.54
2200	36.1 - j47.2	7.38 - j3.49
2220	34.9 - j45.9	7.42 - j3.46

$Z_{in}$  = Device input impedance as simulated from gate to ground.

$Z_{load}$  = Test circuit impedance as simulated from drain to ground.



**Figure 11. Series Equivalent Input and Load Impedance**

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1} = 30 \text{ mA}$ ,  $I_{DQ2} = 195 \text{ mA}$ , CW

f (MHz)	$Z_{in}$ ( $\Omega$ )	$Z_{load}^{(1)}$ ( $\Omega$ )	Max Output Power					
			P1dB			P3dB		
			(dBm)	(W)	PAE (%)	(dBm)	(W)	PAE (%)
2110	42.0 - j42.0	8.0 - j10.1	45.5	36	51.3	46.0	40	50.9
2140	42.6 - j42.0	7.8 - j10.4	45.5	36	50.7	46.0	39	50.4
2170	39.0 - j45.0	7.5 - j10.5	45.3	34	50.3	45.8	38	50.2

(1) Load impedance for optimum P1dB power.

$Z_{in}$  = Impedance as measured from input contact to ground.

$Z_{load}$  = Impedance as measured from drain contact to ground.

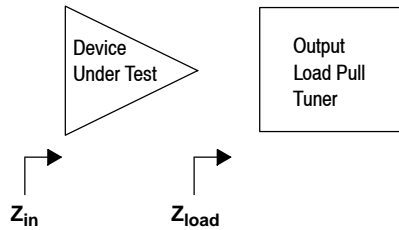


Figure 12. Load Pull Performance — Maximum P1dB Tuning

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1} = 30 \text{ mA}$ ,  $I_{DQ2} = 195 \text{ mA}$ , CW

f (MHz)	$Z_{in}$ ( $\Omega$ )	$Z_{load}^{(1)}$ ( $\Omega$ )	Max Power Added Efficiency					
			P1dB			P3dB		
			(dBm)	(W)	PAE (%)	(dBm)	(W)	PAE (%)
2110	43.0-j48.0	8.1-j4.5	44.3	27	57.2	44.8	30	55.4
2140	42.0-j48.0	7.6-j5.3	44.4	28	56.6	44.8	30	54.8
2170	36.5-j50.0	7.1-j5.8	44.3	27	56.0	44.7	30	54.5

(1) Load impedance for optimum P1dB efficiency.

$Z_{in}$  = Impedance as measured from input contact to ground.

$Z_{load}$  = Impedance as measured from drain contact to ground.

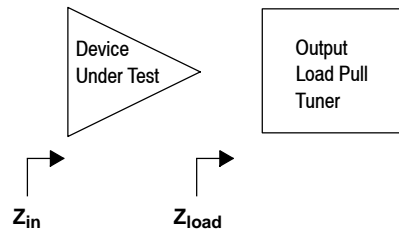


Figure 13. Load Pull Performance — Maximum Power Added Efficiency Tuning

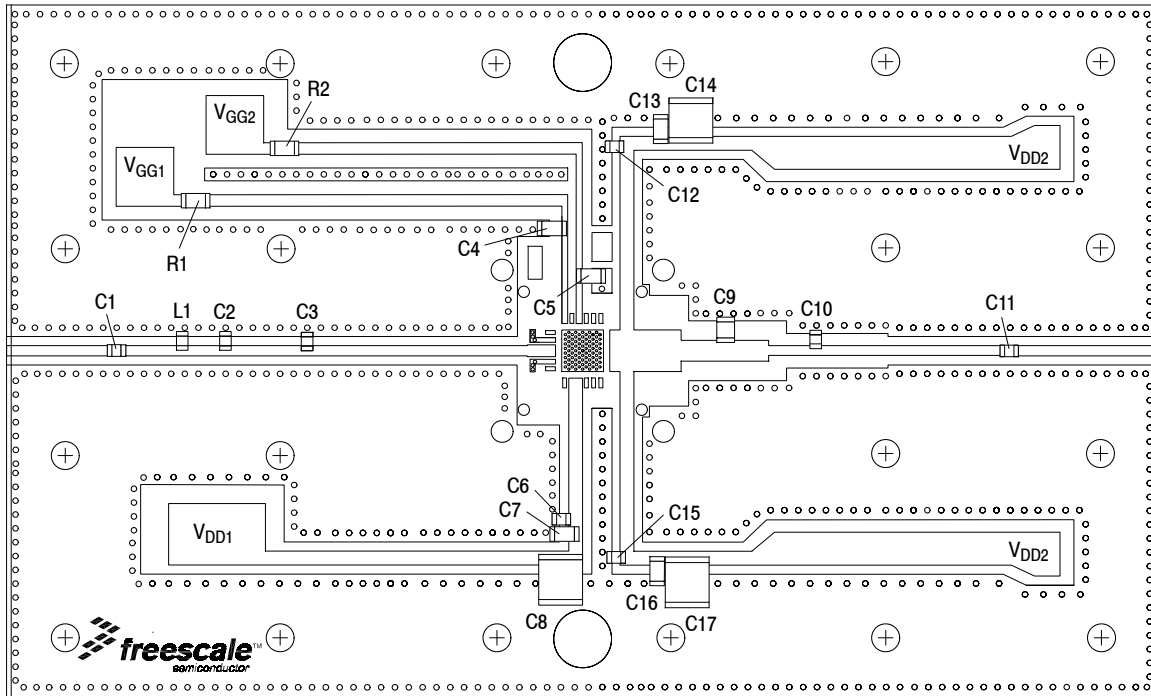


Figure 14. MMRF2006NT1 Test Circuit Component Layout — 1800 MHz

Table 7. MMRF2006NT1 Test Circuit Component Designations and Values — 1800 MHz

Part	Description	Part Number	Manufacturer
C1, C6, C12, C15	33 pF Capacitors	ATC600F330JT250XT	ATC
C2	1.1 pF Chip Capacitor	ATC600F1R1BT250XT	ATC
C3	1.6 pF Chip Capacitor	ATC600F1R6BT250XT	ATC
C4, C5, C13, C16	4.7 $\mu$ F, 50 V Chip Capacitors	GRM31CR71H475KA12L	Murata
C7	1.0 $\mu$ F, 100 V Chip Capacitor	GRM31CR72A105KA01L	Murata
C8, C14, C17	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C9	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C10	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C11	10 pF Capacitors	ATC600F100JT250XT	ATC
L1	12 nH Chip Inductor	L0805120JESTR	AVX
R1, R2	4.7 k $\Omega$ , 1/4 W Chip Resistors	CRCW12064K70FKEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	—	MTL

## TYPICAL CHARACTERISTICS — 1800 MHz

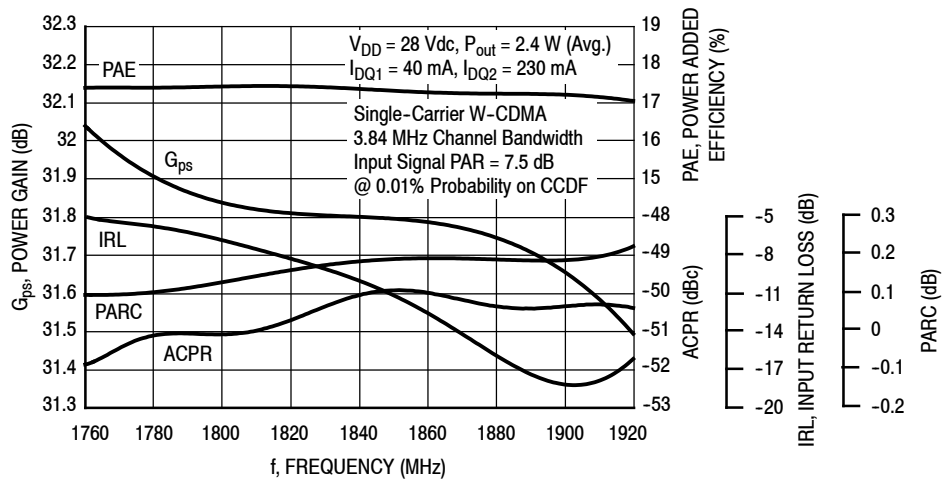


Figure 15. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 2.4$  Watts Avg.

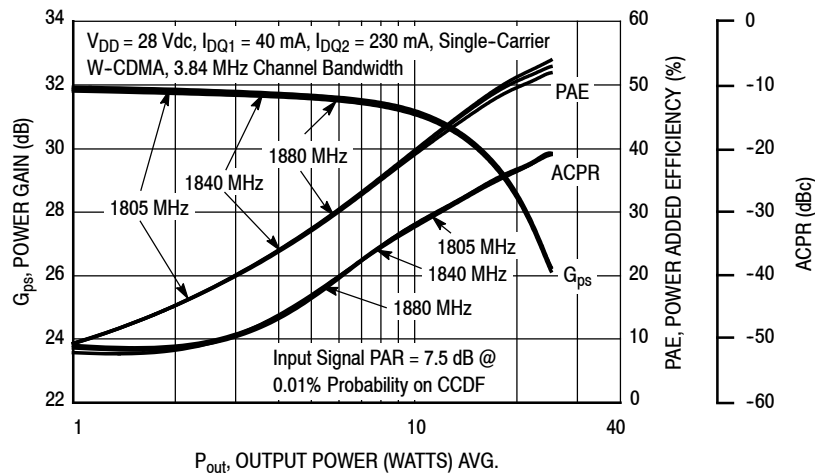


Figure 16. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

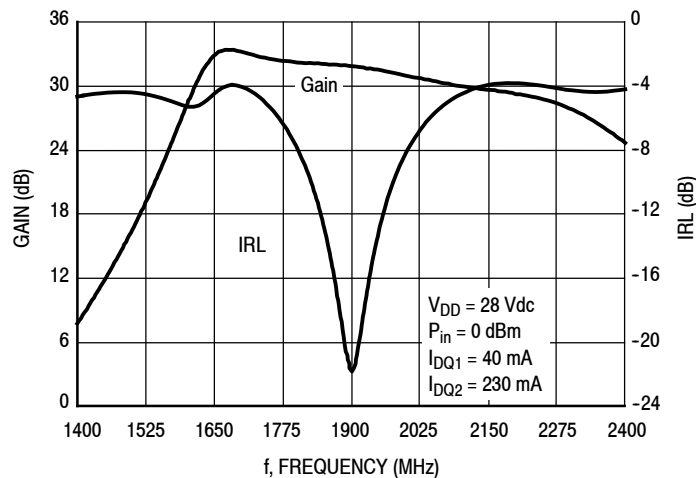


Figure 17. Broadband Frequency Response

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1} = 40 \text{ mA}$ ,  $I_{DQ2} = 230 \text{ mA}$ ,  $P_{out} = 2.4 \text{ W Avg.}$

f MHz	$Z_{in}$ $\Omega$	$Z_{load}$ $\Omega$
1760	46.6 + j14.0	14.4 - j7.06
1780	54.0 + j15.2	14.0 - j6.89
1800	62.4 + j14.5	13.6 - j6.71
1820	70.8 + j11.4	13.2 - j6.53
1840	78.8 + j5.70	12.9 - j6.34
1860	85.2 - j2.64	12.6 - j6.14
1880	88.8 - j12.5	12.4 - j5.94
1900	89.2 - j22.9	12.1 - j5.74
1920	86.7 - j32.6	11.9 - j5.53

$Z_{in}$  = Device input impedance as simulated from gate to ground.

$Z_{load}$  = Test circuit impedance as simulated from drain to ground.

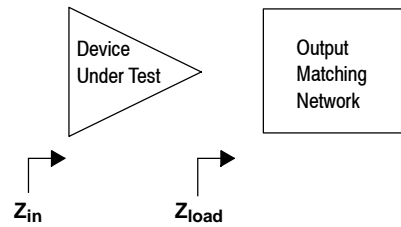
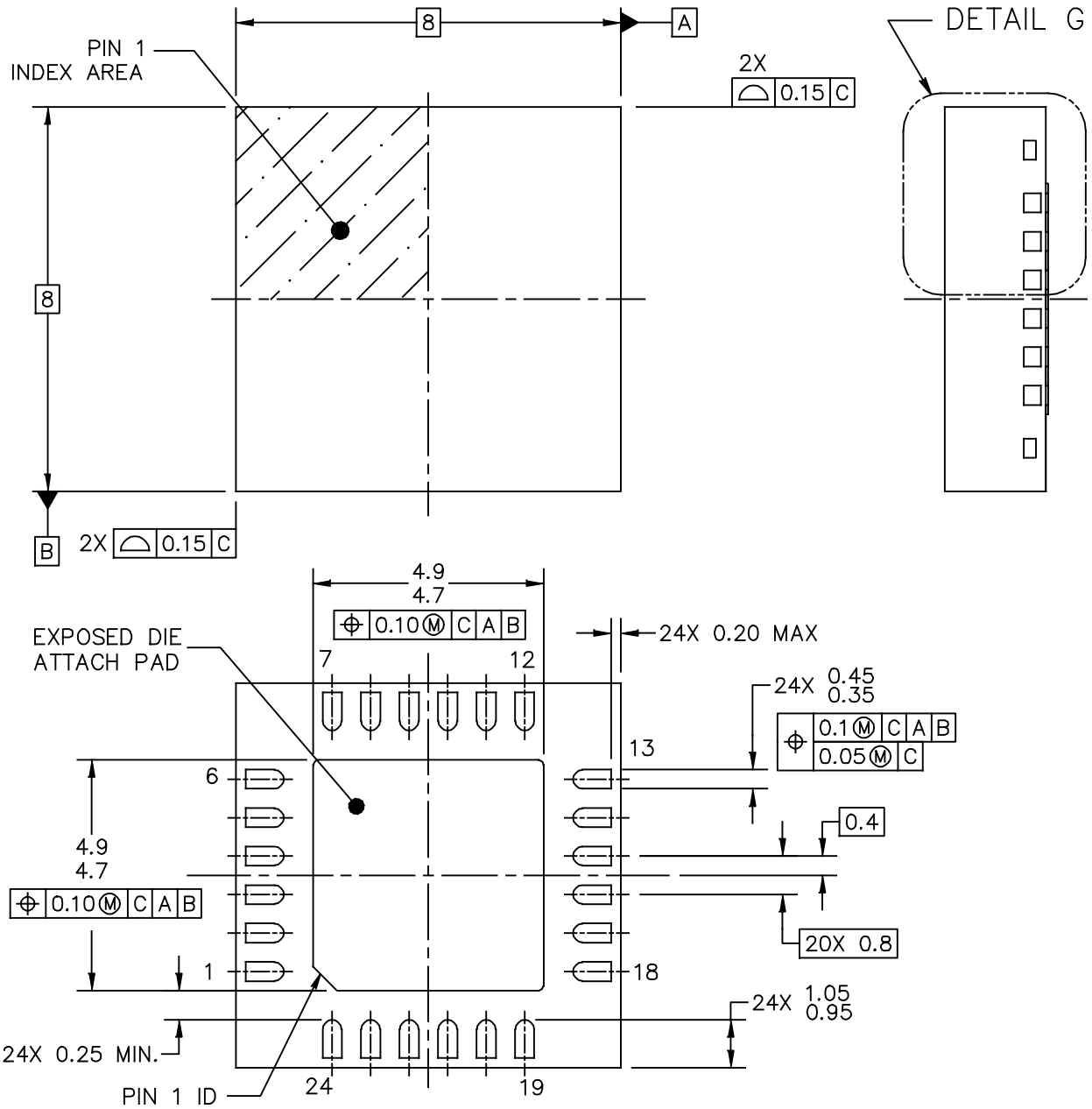
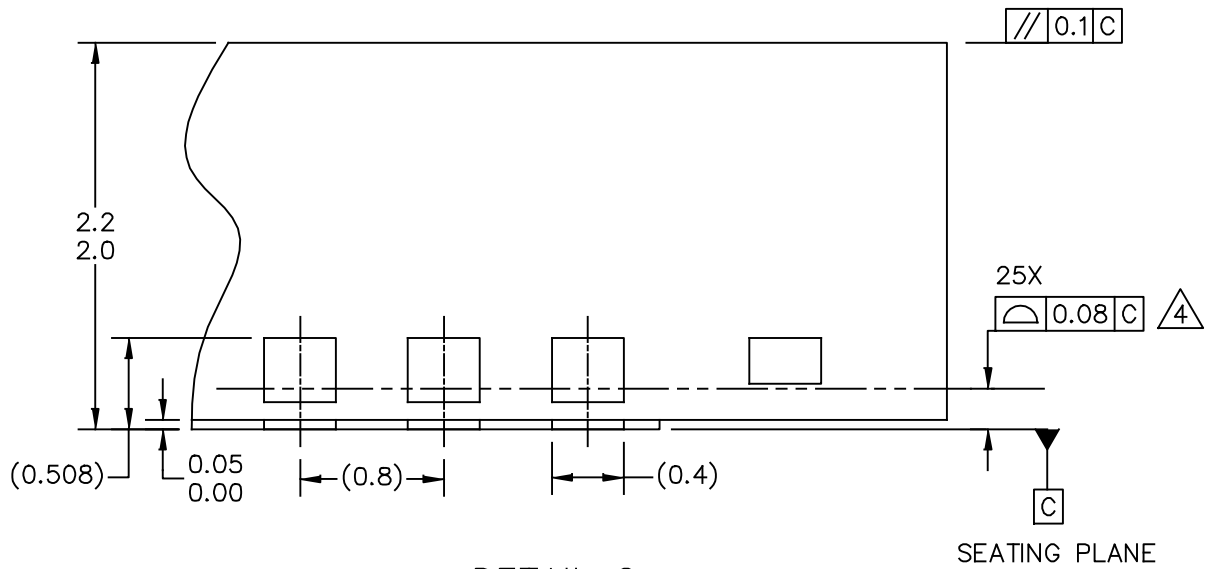


Figure 18. Series Equivalent Input and Load Impedance — 1800 MHz

### PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PQFN (SAW), THERMALLY ENHANCED 8 X 8 X 2.1, 0.8 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA10760D	REV: A	
	CASE NUMBER: 1894-02	29 MAY 2012	
	STANDARD: NON-JEDEC		



DETAIL G  
 VIEW ROTATED 90° CW

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PQFN (SAW), THERMALLY ENHANCED 8 X 8 X 2.1, 0.8 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA10760D	REV: A	
	CASE NUMBER: 1894-02	29 MAY 2012	
	STANDARD: NON-JEDEC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFN.

4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PQFN (SAW), THERMALLY ENHANCED 8 X 8 X 2.1, 0.8 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA10760D	REV: A	
	CASE NUMBER: 1894-02	29 MAY 2012	
	STANDARD: NON-JEDEC		



## PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following resources to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator

For Software, do a Part Number search at <http://www.freescale.com>, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2014	<ul style="list-style-type: none"><li>• Initial Release of Data Sheet</li></ul>

## ***How to Reach Us:***

**Home Page:**  
[freescale.com](http://freescale.com)

**Web Support:**  
[freescale.com/support](http://freescale.com/support)

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners.

© 2014 Freescale Semiconductor, Inc.

