CELLULAR

SARA-U2 series

3.75G HSPA Cellular Modules

Data Sheet

Abstract

Technical data sheet describing SARA-U2 series HSPA cellular modules.

These modules are a complete and cost efficient 3.75G solution offering 2-band high-speed HSPA and up to 2-band GSM/EGPRS voice and/or data transmission technology in a compact form factor.

26.0 x 16.0 x 3.0 mm

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Objective Specification	Document contains target values. Revised and supplementary data will be published later.
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This document applies to the following products:

Product name	Type number	Firmware version	PCN / IN
SARA-U260	SARA-U260-00S-00	23.20	UBX-14015739
SARA-U270	SARA-U270-00S-00	23.20	UBX-14015739
SARA-U280	SARA-U280-00S-00	TBD	TBD
SARA-U290	SARA-U290-00S-00	TBD	TBD
	SARA-U290-60S-00	TBD	TBD

Contents

1 Functional description

1.1 Overview

The SARA-U2 series modules are a 3.75G UMTS/HSPA solution in the miniature (26.0 x 16.0 mm) SARA LGA form factor that allows seamless drop-in migration from u-blox SARA-G3 series GSM/GPRS modules and easy migration to u-blox LISA-U series UMTS/HSPA+ modules, u-blox LISA-C2 series CDMA modules and to u-blox TOBY-L series LTE modules.

SARA-U2 modules feature HSPA data-rates of 7.2 Mb/s (downlink) and 5.76 Mb/s (uplink). The modules offer data and voice communication over an extended operating temperature range of –40 to +85 °C, with low power consumption and a rich feature set including dual-stack IPv4 / IPv6.

The SARA-U2 series include variants supporting band combination for North America and band combination for Europe, Asia and other countries. For each combination, a complete UMTS/GSM variant and a cost-saving UMTS-only variant are available.

SARA-U2 modules are complete, fully qualified and certified solutions, which reduce costs and enable short time to market. They are ideally suited to M2M and automotive applications such as: mobile Internet terminals, car infotainment and telematics, Automatic Meter Reading (AMR), Remote Monitoring Automation and Control (RMAC), surveillance and security, road pricing, asset tracking, fleet management, anti theft systems, and Point of Sales (PoS) terminals.

SARA-U2 modules support full access to u-blox GNSS receivers via serial port. Thus any host processor connected to the cellular module through a single serial port can control both the cellular module and the positioning chip/module.

The compact SARA 26.0 x 16.0 mm form factor with LGA pads (functionally, referred to as "pins") allows fully automated assembly with standard pick & place and reflow soldering equipment for cost-efficient, high-volume production.

1.2 Product features

Module	Data rate		Bands		Interfaces					Audio			Functions												
	HSUPA [Mb/s]	HSDPA [Mb/s]	3G bands [MHz]	2G bands [MHz]	UART	SPI	USB	DDC (I^2C)	GPIO	Analog Audio	Digital Audio over USB	Digital Audio over I^2S	Network indication	Antenna Supervisor	Jamming detection	Embedded TCP / UDP	Embedded HTTP, FTP	Embedded SSL / TLS	GNSS via Modem	AssistNow Software	CellLocate	FW update via serial	eCall / ERA-GLONASS	Rx diversity	Dual stack IPv4/IPv6
SARA-U260	5.76	7.2	850/1900	850/1900	1		1	1	9		F	1	•	•	•	•	•	•	•	•	•	•			•
SARA-U270	5.76	7.2	900/2100	900/1800	1		1	1	9		F	1	•	•	•	•	•	•	•	•	•	•	•		•
SARA-U280	5.76	7.2	850/1900		1		1	1	9		F	1	•	•	•	•	•	•	•	•	•	•			•
SARA-U290	5.76	7.2	900/2100		1		1	1	9		F	1	•	•	•	•	•	•	•	•	•	•	•		•

F = not supported by initial FW release

Table 1: SARA-U2 series[1] main features summary

[1] SARA-U290 modules include '00' and '60' FW versions: SARA-U290-60S is approved and locked for SoftBank Japanese network operator

1.3 Block diagram

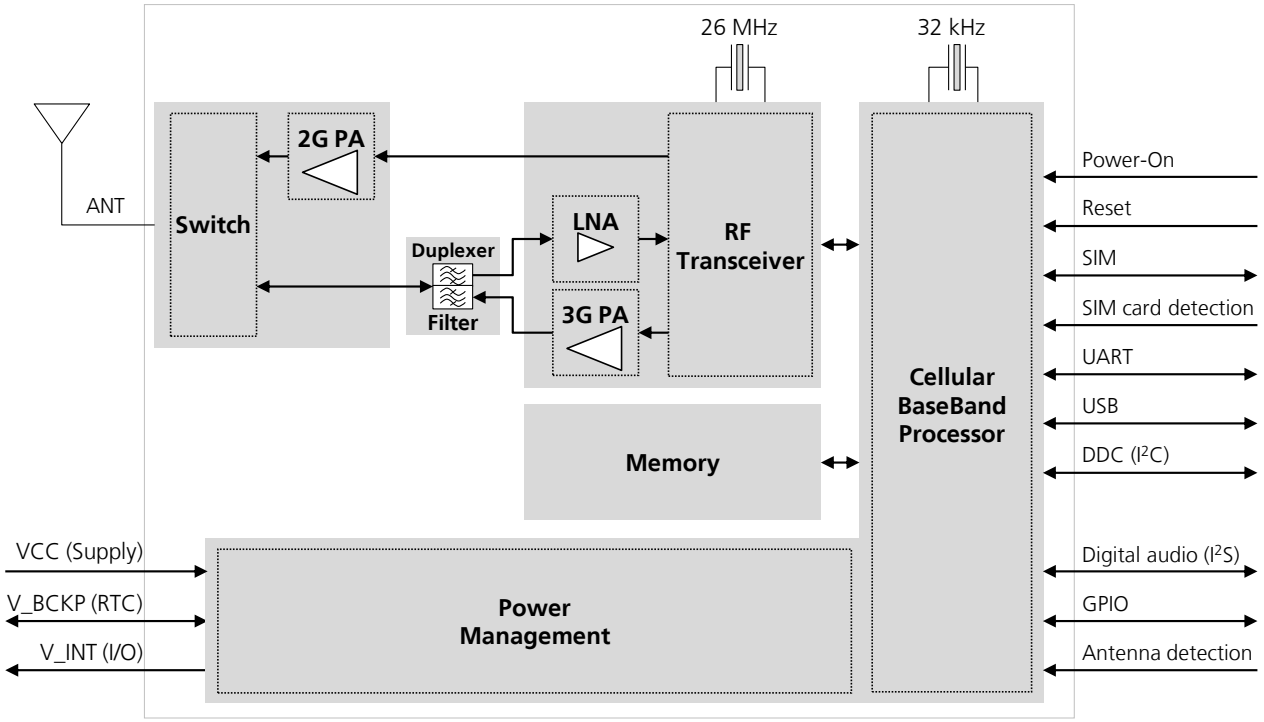

Figure 1: SARA-U260 and SARA-U270 block diagram

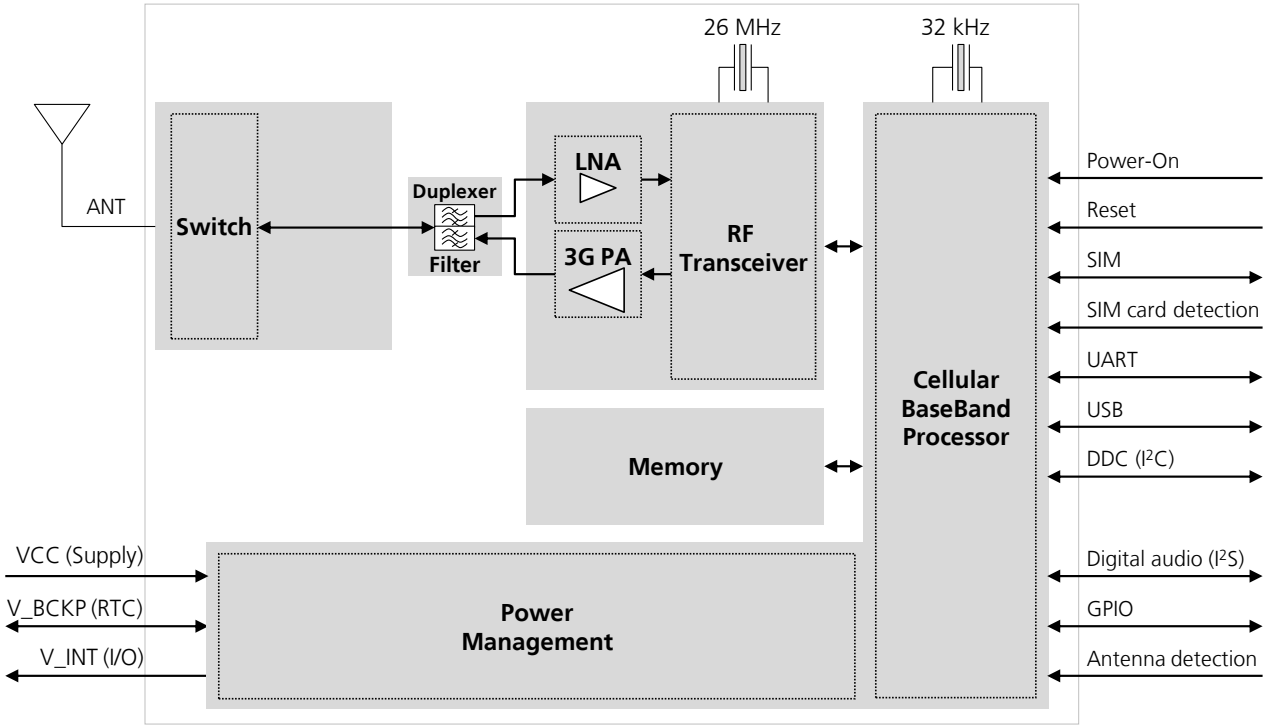

Figure 2: SARA-U280 and SARA-U290 block diagram

1.4 Product description

SARA-U2 series modules provide variants to support different band combinations for specific regions:

- SARA-U260 and SARA-U280 are mainly designed for operation in America
- SARA-U270 and SARA-U290 are mainly designed for operation in Europe, Asia and other countries

3G UMTS/HSDPA/HSUPA characteristics	2G GSM/GPRS/EDGE characteristics[2]
Class A User Equipment[3]	Class B Mobile Station[4]
3GPP Release 7 High Speed Packet Access (HSPA) UMTS Terrestrial Radio Access (UTRA) Frequency Division Duplex (FDD)	3GPP Release 7 Enhanced Data rate GSM Evolution (EDGE) GSM EGPRS Radio Access (GERA) Time Division Multiple Access (TDMA)
Dual-band support: • SARA-U260 and SARA-U280: Band V (850 MHz) Band II (1900 MHz) • SARA-U270 and SARA-U290: Band VIII (900 MHz) Band I (2100 MHz)	Dual-band support: • SARA-U260: GSM 850 MHz PCS 1900 MHz • SARA-U270: E-GSM 900 MHz DCS 1800 MHz
WCDMA/HSDPA/HSUPA Power Class • Power Class 3 (24 dBm) for WCDMA/HSDPA/HSUPA mode	GSM/GPRS/EDGE Power Class • Power Class 4 (33 dBm) for GSM/E-GSM bands • Power Class 1 (30 dBm) for DCS/PCS bands
PS (Packet Switched) data rate • HSUPA category 6, up to 5.76 Mb/s UL • HSDPA category 8, up to 7.2 Mb/s DL • WCDMA PS data, up to 384 kb/s DL/UL	PS (Packet Switched) data rate[5] • GPRS multi-slot class 12[6], CS1-CS4 up to 85.6 kb/s DL/UL • EDGE multi-slot class 12[7], MCS1-MCS9 up to 236.8 kb/s DL, MCS1-MCS4 up to 70.4 kb/s UL
CS (Circuit Switched) data rate • WCDMA CS data, up to 64 kb/s DL/UL	CS (Circuit Switched) data rate • GSM CS data, up to 9.6 kb/s DL/UL supported in transparent/non transparent mode

Table 2: SARA-U2 series 3G and 2G characteristics

Operation modes I to III are supported on GSM/GPRS networks, with user-defined preferred service selectable from GSM to GPRS. Paging messages for GSM calls can be optionally monitored during GPRS data transfer in not-coordinating NOM II-III. Direct Link mode is supported for TCP and UDP sockets.

[2] Supported only by SARA-U260 and SARA-U270 modules
[3] Device can work simultaneously in Packet Switch and Circuit Switch mode: voice calls are possible while the data connection is active without any interruption in service.
[4] Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time. If for example during data transmission an incoming call occurs, the data connection is suspended to allow the voice communication. Once the voice call has terminated, the data service is resumed.
[5] GPRS / EDGE multi-slot class determines the number of timeslots available for upload and download and thus the speed at which data can be transmitted and received, with higher classes typically allowing faster data transfer rates.
[6] GPRS multi-slot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total.
[7] EDGE multi-slot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total.

Basic features	Supplementary services	Short Message Service (SMS)
Display of Called Number	Call Hold/Resume (HOLD)	Text and PDU mode supported
Indication of Call Progress Signals	Call Waiting (CW)	Mobile-Originating SMS (MO SMS)
Country/PLMN Indication	Multi-Party (MTPY)	Mobile-Terminating SMS (MT SMS)
Country/PLMN Selection	Call Forwarding (CFU, CFB, CFNRy, CFNRc)	SMS indication and acknowledgement
International Access Function	Call Deflection (CD)	SMS Cell Broadcast (CBS)
Service Indicator	Explicit Call Transfer (ECT)	SMS during circuit-switched calls
Emergency Calls Capabilities	Call Barring (BAOC, BOIC, BOIC-exHC, BAIC, BIC_Roam)	SMS over CSD
Dual Tone Multi Frequency (DTMF)	Advice of Charge Charging (AoCC, AoCI)	SMS over PSD
Subscription Identity Management	Calling Line Identification Presentation (CLIP)	SMS storage on SIM
Service Provider Indication	Calling Line Identification Restriction (CLIR)	SMS storage on module memory
Abbreviated Dialing	Connected Line Identification Presentation (CoLP)	Concatenated SMS
Fixed Number Dialing	Connected Line Identification Restriction (CoLR)	
Barring of Dialed Numbers	Unstructured Supplementary Services Data (USSD)	
SIM Application Toolkit	Network Identify and Time Zone (NITZ)	
ME-SIM lock	Calling Name Presentation (CNAP)	
SIM Access Profile		

Table 3: SARA-U2 series mobile stations: basic features, supplementary services and SMS service summary[8]

1.5 AT command support

SARA-U2 series modules support AT commands according to the 3GPP Technical Specifications 27.007 [1], 27.005 [2], 27.010 [3], and the u-blox AT command extension.

☞ For the complete list of the supported AT commands and their syntax see the u-blox AT Commands Manual [4].

RIL (Radio Interface Layer) is provided with SARA-U2 modules and is compatible with following deliveries:

- Android 2.3 (Gingerbread)
- Android 4.0 (Ice Cream Sandwich)
- Android 4.1 (Jelly Bean)
- Android 4.2 (Jelly Bean)
- Android 4.3 (Jelly Bean)
- Windows Embedded CE 6.0
- Window Mobile 6.5
- Windows Embedded Compact 7

[8] All these functionalities are supported via AT commands (for more details see u-blox AT Commands Manual [4]).

1.6 Supported features

Table 4 lists the main features supported by SARA-U2 modules. For more details see the SARA-G3 and SARA-U2 series System Integration Manual [5] and u-blox AT commands manual [4].

Feature	Description
Network indication	GPIO configured to indicate the network status: registered home network, registered roaming, voice or data call enabled, no service. The feature can be enabled through the +UGPIOC AT command.
Antenna detection	The **ANT_DET** pin provides antenna presence detection capability, evaluating the resistance from the **ANT** pin to GND by means of an external antenna detection circuit implemented on the application board. The antenna detection feature can be enabled through the +UANTR AT command.
Jamming detection	Detects some "artificial" interference that obscures the operator's carriers entitled to give access to the GSM/UMTS service and reports the start and stop of such conditions to the application processor (AP). The AP can react appropriately by e.g. switching off the radio transceiver to reduce power consumption and monitoring the environment at constant periods. The feature can be enabled and configured through the +UCD AT command.
Embedded TCP and UDP stack	Embedded TCP/IP and UDP/IP stack including direct link mode for TCP and UDP sockets. Sockets can be set in Direct Link mode to establish a transparent end to end communication with an already connected TCP or UDP socket via serial interface.
FTP, FTPS	File Transfer Protocol as well as Secure File Transfer Protocol (SSL encryption of FTP control channel) functionalities are supported via AT commands.
HTTP, HTTPS	Hyper-Text Transfer Protocol as well as Secure Hyper-Text Transfer Protocol (SSL encryption) functionalities are supported via AT commands. HEAD, GET, POST, DELETE and PUT operations are available. Up to four client contexts can be simultaneously used.
IPv4/IPv6 dual-stack	Capability to move between IPv4 and dual stack network infrastructures. IPv4 and IPv6 addresses can be used.
GNSS via modem	Full access to u-blox positioning chips and modules is available through a dedicated DDC (I^2C) interface. This means that from any host processor a single serial port can control the cellular module and the positioning chip or module. For more details see the GNSS Implementation Application Note [6].
Embedded AssistNow Software	Embedded AssistNow Online and AssistNow Offline clients to provide better GNSS performance and faster Time-to-First-Fix. An AT command can enable / disable the clients.
CellLocate™	Enables the estimation of device position based on the parameters of the mobile network cells visible to the specific device based on the CellLocate database: • Normal scan: only the parameters of the visible home network cells are sent • Deep scan: the parameters of all surrounding cells of all mobile operators are sent CellLocate™ is implemented using a set of AT commands for CellLocate service configuration and position request.
Hybrid Positioning	The module current position is provided using a u-blox positioning chip or module or the estimated position from CellLocate depending by which positioning method provides the best and fastest solution according to the user configuration. Hybrid positioning is implemented through a set of AT commands that allow the configuration and the position request.
Firmware update Over AT commands (FOAT)	Firmware module upgrade over UART and USB interface using AT command.
SIM Access Profile (SAP)	Allows access and use of a remote (U)SIM card instead of the local SIM card directly connected to the module (U)SIM interface. The module acts as an SAP Client establishing a connection and performing data exchange to a SAP Server directly connected to the remote SIM. The modules provide a dedicated USB SAP channel and a dedicated multiplexer SAP channel over UART for communication with the remote (U)SIM card.

Feature	Description
Smart Temperature Supervisor	Constant monitoring of the module board temperature: • Warning notification when the temperature approaches an upper or lower predefined threshold • Shutdown notified and forced when the temperature value is outside the specified range (shutdown suspended in case of an emergency call in progress) The feature can be enabled or disabled through the +USTS AT command. ☞ The sensor measures board temperature inside the shield, which can differ from ambient temperature.
In-Band Modem[9]	In-Band modem solution for eCall and ERA-GLONASS emergency call applications over cellular networks implemented according to the 3GPP TS 26.267 specification [7]. When activated, the in-vehicle eCall / ERA-GLONASS system (IVS) creates an emergency call carrying both voice and data (including vehicle position data) directly to the nearest Public Safety Answering Point (PSAP) to determine whether rescue services should be dispatched to the known position.
DTMF decoder	During a voice call, the Dual-Tone Multi-Frequency detector analyses the RX speech (coming from the remote party). The detected DTMF symbols can be output via the related URC. For more details, see the +UDTMFD AT command.
Audio Over USB	Audio over USB capabilities can be enabled by specific AT command (see the u-blox AT Commands Manual [4]): the Audio Device Class provides a streaming interface, which transfers audio data on isochronous pipes.
Power saving	The power saving configuration is by default disabled, but it can be configured using an AT command. When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption. During idle-mode, the module processor core runs with the RTC 32 kHz reference clock, which is generated by the internal 32 kHz oscillator The feature can be enabled through the +UPSV AT command.

Table 4: SARA-U2 series' main supported features

☞ u-blox is extremely mindful of user privacy. When a position is sent to the CellLocate™ server u-blox is unable to track the SIM used or the specific device.

[9] Supported only by SARA-U270 and SARA-U290 modules

2 Interfaces

2.1 Power management

2.1.1 Module supply (VCC)

SARA-U2 modules must be supplied through the **VCC** pins by a DC power supply. Voltages must be stable: during operation, the current drawn from **VCC** can vary by some order of magnitude, especially due to the surging consumption profile of the GSM system (described in SARA-G3 and SARA-U2 series System Integration Manual [5]). It is important that the system power supply circuit is able to support peak power.

2.1.2 RTC supply (V_BCKP)

V_BCKP is the Real Time Clock (RTC) supply of SARA-U2 modules. When **VCC** voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the RTC and the same supply voltage is available on **V_BCKP** pin. If the **VCC** voltage is under the minimum operating limit (e.g. during not powered mode), the **V_BCKP** pin can externally supply the RTC.

2.1.3 Generic digital interfaces supply (V_INT)

SARA-U2 modules provide a 1.8 V supply rail output on the **V_INT** pin, which is internally generated when the module is switched on. The same voltage domain is used internally to supply the generic digital interfaces of the modules. The **V_INT** supply output can be used in place of an external discrete regulator optimizing the bill of material for various applications, e.g. with u-blox GNSS receivers operating at 1.8 V.

2.2 Antenna

2.2.1 Antenna RF interface (ANT)

The **ANT** pin has an impedance of 50 Ω and provides the RF antenna interface of SARA-U2 modules.

2.2.2 Antenna detection (ANT_DET)

The **ANT_DET** pin is an Analog to Digital Converter (ADC) input to sense the antenna presence (as optional feature), evaluating the resistance from the **ANT** pin to GND by means of an external antenna detection circuit implemented on the application board (for more details see the SARA-G3 and SARA-U2 series System Integration Manual [5] and the u-blox AT Commands Manual [4], +UANTR).

2.3 System functions

2.3.1 Module power-on

SARA-U2 modules can be switched on in one of the following ways:

- Rising edge on **VCC** pins to a valid voltage for module supply, i.e. applying module supply
- Low pulse on **PWR_ON** pin, i.e. forcing the pin (normally high with external pull-up) to a low level for a valid time period (see section 4.2.6): **PWR_ON** pin requires an external pull-up resistor to set its value to logic high and may not be left floating
- Rising edge on **RESET_N** pin, i.e. releasing the pin from the low level, normally high with internal pull-up
- RTC alarm, i.e. pre-programmed scheduled time by AT+CALA command

2.3.2 Module power-off

SARA-U2 modules can be properly switched off, with storage of current parameter settings and network detach, in one of these ways:

- AT+CPWROFF command
- Low pulse on the **PWR_ON** pin for at least 1 s

An abrupt under-voltage shutdown occurs on SARA-U2 modules when the **VCC** supply drops below the extended operating range minimum limit, but in this case it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory as well as the proper network detach.

An over-temperature or an under-temperature shutdown occurs on SARA-U2 modules when the temperature measured within the cellular module reaches the dangerous area, if the optional Smart Temperature Supervisor feature is enabled and configured by the dedicated AT command. For more details see the SARA-G3 and SARA-U2 series System Integration Manual [5] and u-blox AT commands manual [4], +USTS AT command.

2.3.3 Module reset

SARA-U2 modules can be properly reset (rebooted), with storage of current parameter settings and network detach, in this way:

- By the AT+CFUN command (see the u-blox AT Commands Manual [4]). This causes an "internal" or "software" reset of the baseband processor, excluding the integrated power management unit and the RTC internal block: the **V_INT** generic digital interfaces supply is enabled and each digital pin is set to its internal reset state (reported in Table 6), the **V_BCKP** supply and the RTC block are enabled.

An abrupt "external" or "hardware" reset occurs when a low level is applied to the **RESET_N** pin, which is normally set high by an internal pull-up, for a valid time period (see section 4.2.7). This causes a reset of the entire module, including the integrated power management unit, except for the RTC internal block: the **V_INT** generic digital interfaces supply is switched off and all the digital pins are tri-stated, but the **V_BCKP** supply and the RTC block are enabled. The current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.

2.4 SIM

2.4.1 (U)SIM interface

SARA-U2 modules provide a (U)SIM interface on the **VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST** pins: the high-speed SIM/ME interface is implemented as well as automatic detection of the required SIM supporting voltage.

Both 1.8 V and 3 V SIM card/chip types are supported (1.8 V and 3 V ME). Activation and deactivation with automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values proposed by the SIM card/chip.

2.4.2 SIM card detection (SIM_DET)

The **SIM_DET** pin of SARA-U2 modules is a 1.8 V digital input which is by default configured as an external interrupt to detect the SIM card presence (as a feature which can be optionally used) when it is properly connected to the mechanical switch of the SIM card holder (for more details see SARA-G3 and SARA-U2 series System Integration Manual [5]).

The **SIM_DET** pin of SARA-U2 modules can additionally be configured via AT command to provide the "SIM card hot insertion/removal" function (for more details see u-blox AT Commands Manual [4], +UDCONF=50).

The **SIM_DET** pin of SARA-U2 modules can additionally be configured via AT command as GPIO (for more details see section 2.7 and the u-blox AT Commands Manual [4], +UGPIOC, +UGPIOR, +UGPIOW).

2.5 Serial interfaces

SARA-U2 modules provide the following serial communication interfaces:

- UART interface: asynchronous serial interface available for AT commands, data communication, FW upgrade by means of the FOAT feature, FW upgrade by means of the u-blox EasyFlash tool
- USB interface: High-Speed USB 2.0 compliant interface available for AT commands, data communication, FW upgrade by means of the FOAT feature, FW upgrade by means of the u-blox EasyFlash tool and for diagnostic purpose
- DDC interface: I^2C compatible interface available for the communication with u-blox GNSS positioning chips/modules and with external I^2C devices as an audio codec

2.5.1 Asynchronous serial interface (UART)

The UART interface is a 9-wire 1.8 V unbalanced asynchronous serial interface provided for AT commands, data communication, FW upgrade by means of the FOAT feature, FW upgrade by means of the u-blox EasyFlash tool.

The UART features are:

- Complete serial port with RS-232 functionality conforming to the ITU-T V.24 Recommendation [8], with CMOS compatible signal levels (0 V for low data bit or ON state and 1.8 V for high data bit or OFF state)
- Data lines (**RxD** as output, **TxD** as input), hardware flow control lines (**CTS** as output, **RTS** as input), modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output) are provided
- Hardware flow control (default value), software flow control, or none flow control are supported
- Power saving indication available[10] on the hardware flow control output (CTS line): the line is driven to the OFF state when the module is not prepared to accept data by the UART interface
- 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600 b/s baud rates are supported for the AT interface
- Autobauding is by default enabled
- Frame format can be:
  - 8N2 (8 data bits, no parity, 2 stop bits)
  - 8N1 (8 data bits, no parity, 1 stop bit)
  - 8E1 (8 data bits, even parity, 1 stop bit)
  - 8O1 (8 data bits, odd parity, 1 stop bit)
  - 7E1 (7 data bits, even parity, 1 stop bit)
  - 7O1 (7 data bits, odd parity, 1 stop bit)
- Default frame configuration is 8N1

The UART serial interface can be conveniently configured through AT commands. For more details see the u-blox AT Commands Manual [4] (+IPR, +ICF, +IFC, &K, \Q, +UPSV AT command) and SARA-G3 and SARA-U2 series System Integration Manual [5].

[10] If enabled

2.5.1.1 Autobauding feature

Only one shot autobauding is supported: the baud rate detection is performed only once, at module start up.

After detection the module works at the fixed baud rate (the detected one) and the baud rate can only be changed via the appropriate AT command (+IPR, for more details see the u-blox AT Commands Manual [4]).

- The module detects the followings baud rates (b/s): 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400
- The only detectable frame configurations are: 7E1, 7O1, 8N1, 8E1, 8O1

2.5.1.2 Multiplexer protocol

SARA-U2 module has a software layer with MUX functionality, 3GPP TS 27.010 Multiplexer Protocol [3], available on the UART interface.

☞ The multiplexer protocol is supported over the UART physical interface only.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the cellular module (Data Circuit-terminating Equipment) and the application processor (Data Terminal Equipment) allowing simultaneous sessions over the UART physical link: the user can concurrently use AT command interface on one MUX channel and Data communication on another MUX channel. Each session consists of a stream of bytes transferring various kinds of data such as SMS, CBS, PSD, GNSS, AT commands in general.

SARA-U2 modules provide the following virtual channels:

- Channel 0: control channel
- Channel 1 – 5: AT commands / data connection
- Channel 6: GNSS tunneling
- Channel 7: SAP (SIM Access Profile)

For more details see the Mux Implementation Application Note [9].

2.5.2 Universal Serial Bus (USB)

SARA-U2 modules include a high-speed USB 2.0 compliant interface with maximum throughput of 480 Mb/s. The module itself acts as a USB device and can be connected to any USB host.

The USB is the suitable interface for transferring high speed data between SARA-U2 series and a host processor, available for AT commands, data communication, FW upgrade by means of the FOAT feature, FW upgrade by means of the u-blox EasyFlash tool and for diagnostic purpose.

Signals **USB_D+/USB_D-** carry the USB serial data and signaling. The USB interface is automatically enabled by an external valid USB VBUS supply voltage (5.0 V typical) applied on the **VUSB_DET** pin.

SARA-U2 modules provide by default 7 USB CDCs (Communications Device Class):

- USB1: AT and Data
- USB2: AT and Data
- USB3: AT and Data
- USB4: GNSS tunneling
- USB5: Primary Log (diagnostic purpose)
- USB6: Secondary Log (diagnostic purpose)
- USB7: SAP (SIM Access Profile)

The user can concurrently use the AT command interface on one CDC, and Packet-Switched / Circuit-Switched Data communication on another CDC.

Audio over USB capabilities can be enabled by specific AT command (see u-blox AT Commands Manual [4]): the Audio Device Class provides a streaming interface, which transfers audio data on isochronous pipes.

☞ The USB Audio Device Class is not supported by initial firmware release.

USB CDC/ACM drivers are available for the following operating system platforms:

- Windows 2000
- Windows XP
- Windows Vista
- Windows 7
- Windows 8
- Windows CE 5.0
- Windows Embedded CE 6.0
- Windows Embedded Compact 7
- Windows Embedded Automotive 7
- Windows Mobile 5
- Windows Mobile 6
- Windows Mobile 6.1
- Windows Mobile 6.5

SARA-U2 modules are compatible with standard Linux/Android USB kernel drivers.

2.5.3 DDC (I^2C) bus interface

SARA-U2 modules include an I^2C compatible DDC interface (**SDA**, **SCL**) available to communicate with a u-blox GNSS receiver and with external I^2C devices as an audio codec: SARA-U2 module acts as an I^2C master which can communicate with I^2C slaves in accordance to the I^2C bus specifications [10].

2.6 Audio

SARA-U2 modules have one 4-wire I^2S digital audio interface (**I2S_CLK**, **I2S_RXD**, **I2S_TXD** and **I2S_WA**) that can be configured by AT commands in PCM or in normal I^2S mode. (For more details see the u-blox AT Commands Manual [4] and the SARA-G3 and SARA-U2 series System Integration Manual [5].)

SARA-U2 modules provide a digital clock output (**CODEC_CLK**) for an external audio codec.

Audio over USB capabilities can be enabled by specific AT command (see u-blox AT Commands Manual [4]): the Audio Device Class provides a streaming interface, which transfers audio data on isochronous pipes.

☞ The USB Audio Device Class is not supported by initial firmware release.

2.7 GPIO

SARA-U2 modules provide nine pins (**GPIO1**, **GPIO2**, **GPIO3**, **GPIO4**, **I2S_RXD**, **I2S_TXD**, **I2S_CLK**, **I2S_WA**, **SIM_DET**) which can be configured as general purpose input/output, or to provide the custom functions listed in Table 5 via u-blox AT commands. For further details see the SARA-G3 and SARA-U2 series System Integration Manual [5] and the u-blox AT Commands Manual [4], +UGPIOC, +UGPIOR, +UGPIOW, +UGPS, +UGPRF, +USPM, +UDCONF=50 commands.

Function	Description	Module	Default GPIO	Configurable GPIOs
GSM Tx-burst indication	GSM transmit slot indication	SARA-U260, SARA-U270	--	GPIO1
GNSS supply enable	Enable/disable the supply of the u-blox GNSS receiver connected to the cellular module	All	GPIO2	GPIO1, GPIO2, GPIO3, GPIO4, SIM_DET
GNSS data ready	Sense when the u-blox GNSS receiver connected to the cellular module is ready for sending data over the DDC (I^2C) interface	All	GPIO3	GPIO3
GNSS RTC sharing	RTC synchronization signal to the u-blox GNSS receiver connected to the cellular module	All	GPIO4	GPIO4
SIM card detection	SIM card physical presence detection	All	SIM_DET	SIM_DET
SIM card hot insertion	SIM card hot insertion/removal	All	--	SIM_DET
Network status indication	Network status: registered 2G / 3G home network, registered 2G / 3G roaming, 2G / 3G data transmission, no service	All	--	GPIO1, GPIO2, GPIO3, GPIO4, SIM_DET
Module status indication	Module status: power off mode, i.e. module switched off, versus idle, active or connected mode, i.e. module switched on	All	--	GPIO1
Module operating mode indication	Module operating mode: idle mode versus active or connected mode	All	--	SIM_DET
I^2S digital audio interface	I^2S digital audio interface (**I2S_RXD**, **I2S_TXD**, **I2S_CLK**, **I2S_WA** respectively)	All	I2S_RXD, I2S_TXD, I2S_CLK, I2S_WA	I2S_RXD, I2S_TXD, I2S_CLK, I2S_WA
General purpose input	Input to sense high or low digital level	All	--	All
General purpose output	Output to set the high or the low digital level	All	--	All
Pin disabled	Tri-state with an internal active pull-down enabled	All	GPIO1	All

Table 5: GPIO custom functions configuration

3 Pin definition

3.1 Pin assignment

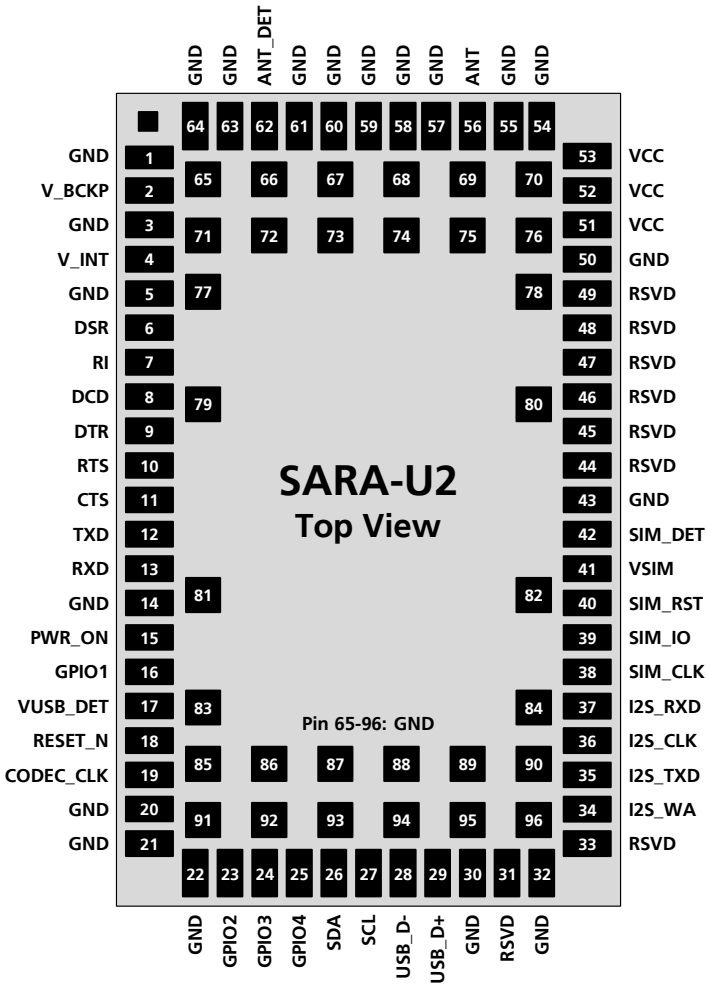

Figure 3: SARA-U2 series pin assignment

No	Module	Name	Power domain	I/O	Description	Remarks
1	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
2	All	V_BCKP	-	I/O	Real Time Clock supply input/output	V_BCKP = 1.8 V (typical) generated by the module to supply the Real Time Clock when VCC supply voltage is within valid operating range. See section 4.2.2 for detailed electrical specs.
3	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
4	All	V_INT	-	O	Generic Digital Interfaces supply output	V_INT = 1.8 V (typical) generated by the module when it is switched-on and the RESET_N (external reset input pin) is not forced to the low level. See section 4.2.2 for detailed electrical specs.
5	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
6	All	DSR	GDI	O	UART data set ready	Circuit 107 (DSR) in ITU-T V.24. Output driver class D. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
7	All	RI	GDI	O	UART ring indicator	Circuit 125 (RI) in ITU-T V.24. Output driver class C_0. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
8	All	DCD	GDI	O	UART data carrier detect	Circuit 109 (DCD) in ITU-T V.24. Output driver class C_0. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
9	All	DTR	GDI	I	UART data terminal ready	Circuit 108/2 (DTR) in ITU-T V. 24. Internal active pull-up to V_INT enabled. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
10	All	RTS	GDI	I	UART ready to send	Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to V_INT enabled. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
11	All	CTS	GDI	O	UART clear to send	Circuit 106 (CTS) in ITU-T V.24. Output driver class A. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
12	All	TXD	GDI	I	UART data input	Circuit 103 (TxD) in ITU-T V.24. Internal active pull-up to V_INT enabled. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
13	All	RXD	GDI	O	UART data output	Circuit 104 (RxD) in ITU-T V.24. Output driver class A. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
14	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
15	All	PWR_ON	POS	I	Power-on input	The PWR_ON pin has high input impedance: don't leave it floating in noisy environment (an external pull-up resistor is required) See section 4.2.6 for detailed electrical specs.
16	All	GPIO1	GDI	I/O	GPIO	GPIO configurable as described in Table 5. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
17	All	VUSB_DET	USB	I	USB detect input	Input for VBUS (5 V typical) USB supply sense. See section 4.2.10 for detailed electrical specs.
18	All	RESET_N	ERS	I	External reset input	Internal 10 kΩ pull-up resistor to V_BCKP. See section 4.2.7 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
19	All	CODEC_CLK	GDI	O	Clock output	Output driver class B. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
20	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
21	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
22	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
23	All	GPIO2	GDI	I/O	GPIO	GPIO configurable as described in Table 5. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
24	All	GPIO3	GDI	I/O	GPIO	GPIO configurable as described in Table 5. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
25	All	GPIO4	GDI	I/O	GPIO	GPIO configurable as described in Table 5. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
26	All	SDA	DDC	I/O	I^2C bus data line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
27	All	SCL	DDC	O	I^2C bus clock line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
28	All	USB_D-	USB	I/O	USB Data Line D-	90 Ω nominal differential impedance. Pull-up, pull-down and series resistors as required by USB 2.0 specifications [11] are part of the USB pin driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
29	All	USB_D+	USB	I/O	USB Data Line D+	90 Ω nominal differential impedance. Pull-up, pull-down and series resistors as required by USB 2.0 specifications [11] are part of the USB pin driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
30	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
31	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
32	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
33	All	RSVD	-	N/A	RESERVED pin	This pin must be connected to GND.
34	All	I2S_WA	GDI	I/O / I/O	I^2S word alignment / GPIO	Configurable as I^2S word alignment (Input with internal active pull-down enabled in slave mode, Output in master mode), or as GPIO (see Table 5). Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
35	All	I2S_TXD	GDI	O / I/O	I^2S transmit data / GPIO	Configurable as I^2S transmit data output, or as GPIO (see Table 5). Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
36	All	I2S_CLK	GDI	I/O / I/O	I^2S clock / GPIO	Configurable as I^2S clock (Input with internal active pull-down to GND enabled in slave mode, Output in master mode), or as GPIO (see Table 5). Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
37	All	I2S_RXD	GDI	I / I/O	I²S receive data / GPIO	Configurable as I²S receive data input (with internal active pull-down enabled), or as GPIO (see Table 5). Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
38	All	SIM_CLK	SIM	O	SIM clock	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
39	All	SIM_IO	SIM	I/O	SIM data	Internal 4.7 kΩ pull-up resistor to VSIM. Value at internal reset: L/PD. See section 4.2.8 for detailed electrical specs.
40	All	SIM_RST	SIM	O	SIM reset	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
41	All	VSIM	-	O	SIM supply output	VSIM = 1.80 V typical or 2.90 V typical generated by the module according to the SIM card type. See section 4.2.2 for detailed electrical specs.
42	All	SIM_DET	GDI	I	SIM detection	Configurable for the SIM card presence detection function, or as GPIO (see Table 5). PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
43	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
44	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
45	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
46	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
47	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
48	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
49	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
50	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
51	All	VCC	-	I	Module supply input	All VCC pins must be connected to external supply. See sections 4.2.2 and 4.2.3 for detailed specs.
52	All	VCC	-	I	Module supply input	All VCC pins must be connected to external supply. See sections 4.2.2 and 4.2.3 for detailed specs.
53	All	VCC	-	I	Module supply input	All VCC pins must be connected to external supply. See sections 4.2.2 and 4.2.3 for detailed specs.
54	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
55	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
56	All	ANT	-	I/O	RF input/output	50 Ω nominal impedance See section 4.2.4 for detailed electrical specs.
57	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
58	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
59	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
60	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
61	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
62	All	ANT_DET	ADC	I	Antenna detection	Antenna presence detection function. See section 4.2.5 for detailed electrical specs.
63	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
64	All	GND	-	N/A	Ground	All the GND pins must be connected to ground
65-96	All	GND	-	N/A	Ground	All the GND pins must be connected to ground

Table 6: SARA-U2 series module pin-out

☞ For more information about pin-out see the SARA-G3 and SARA-U2 series System Integration Manual [5].

☞ For an explanation of abbreviations and terms used, see Appendix A.

4 Electrical specifications

Stressing the device above one or more of the ratings listed in the Absolute Maximum Rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating Conditions sections (section 4.2) of the specification should be avoided. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating conditions ranges define those limits within which the functionality of the device is guaranteed.

Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum rating

Limiting values given below are in accordance with the Absolute Maximum Rating System (IEC 134).

Symbol	Description	Condition	Min.	Max.	Unit
VCC	Module supply voltage	Input DC voltage at VCC pins	-0.30	5.50	V
VUSB_DET	USB detection pin	Input DC voltage at VUSB_DET pin	-0.30	5.35	V
USB	USB D+/D- pins	Input DC voltage at USB_D+ and USB_D- pins	-1.00	5.35	V
V_BCKP	RTC supply voltage	Input DC voltage at V_BCKP pin	-0.15	2.00	V
GDI	Generic digital interfaces	Input DC voltage at Generic digital interfaces pins	-0.30	3.60	V
DDC	DDC interface	Input DC voltage at DDC interface pins	-0.30	3.60	V
SIM	SIM interface	Input DC voltage at SIM interface pin	-0.30	3.60	V
ERS	External reset signal	Input DC voltage at RESET_N external reset pin	-0.15	2.10	V
POS	Power-on signal	Input DC voltage at PWR_ON power-on pin	-0.30	5.50	V
ADC	Antenna detection pin	Input DC voltage at ANT_DET pin	-0.15	3.00	V
P_ANT	Antenna power	Input RF power at ANT pin		-10	dBm
Rho_ANT	Antenna ruggedness	Output RF load mismatch ruggedness at ANT pin		15:1	VSWR
Tstg	Storage Temperature		-40	90	°C

Table 7: Absolute maximum ratings

The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD

Parameter	Module	Min.	Typ.	Max.	Unit	Remarks
ESD sensitivity for all pins except ANT pin				1000	V	Human Body Model according to JESD22-A114F
ESD sensitivity for ANT pin				1000	V	Human Body Model according to JESD22-A114F
ESD immunity for ANT pin				2000	V	Contact Discharge according to IEC 61000-4-2
				4000	V	Air Discharge according to IEC 61000-4-2

Table 8: Maximum ESD ratings

SARA-U2 modules are Electrostatic Sensitive Devices (ESD) and require special precautions when handling. See section 7.4 for ESD handling instructions.

4.2 Operating conditions

Unless otherwise indicated, all operating condition specifications are at an ambient temperature of 25°C.

Operation beyond the operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating temperature range

Symbol	Parameter	Min.	Typ.	Max.	Units	Remarks
Topr	Operating temperature range	-40		+85	°C	
		-20		+55	°C	Normal operating temperature range See section 4.2.1.1
		-40		-20	°C	Extended operating temperature range 1 See section 4.2.1.2
		+65		+85	°C	Extended operating temperature range 2 See section 4.2.1.3

Table 9: Environmental conditions

4.2.1.1 Normal operating temperature range

The cellular module is fully functional and meets the 3GPP specification across the specified temperature range.

4.2.1.2 Extended operating temperature range 1

The cellular module is fully functional across the specified temperature range. Occasional deviations from the 3GPP specification may occur.

4.2.1.3 Extended operating temperature range 2

The cellular module is functional across the specified temperature range. Occasional deviations from the 3GPP specification may occur. Thermal protection including automatic shutdown is implemented for protection against overheating. Thermal protection is disabled for emergency calls. For more details, see the u-blox AT Commands Manual [4], +USTS AT command).

4.2.2 Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Module supply normal operating input voltage[11]	3.30	3.80	4.40	V
	Module supply extended operating input voltage[12]	3.10		4.50	V
V_BCKP	RTC supply input voltage	1.00	1.80	1.90	V
I_BCKP	RTC supply average current consumption, at V_BCKP = 1.8 V		2.00		µA

Table 10: Input characteristics of Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VSIM	SIM supply output voltage	1.76	1.80	1.83	V
		2.84	2.90	2.94	V
V_BCKP	RTC supply output voltage	1.71	1.80	1.89	V
I_BCKP	RTC supply output current capability			3	mA
V_INT	Digital I/O Interfaces supply output voltage	1.73	1.80	1.87	V
V_INT_RIPPLE	Digital I/O Interfaces supply output peak-to-peak voltage ripple during active or connected mode			15	mV
	Digital I/O Interfaces supply output peak-to-peak voltage ripple during low power idle mode with power saving enabled by AT+UPSV command			70	mV
I_INT	Digital I/O Interfaces supply output current capability			70	mA

Table 11: Output characteristics of Supply/Power pins

[11] Input voltage at **VCC** must be above the normal operating range minimum limit to switch-on the module.
[12] Occasional deviations from the 3GPP specifications may occur. Ensure that input voltage at **VCC** never drops below the extended operating range minimum limit during module operation: the module may switch-off when the **VCC** voltage value drops below the extended operating range minimum limit.

4.2.3 Current consumption

Mode	Condition	Band	Min	Typ[13]	Max[14]	Unit
Power Off Mode	Averaged current, module switched off			65		µA
2G Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV, Module registered with network)	Averaged current, DRX = 9[15], AT+UPSV=2 or 3, USB interface disconnected	All		0.9		mA
	Averaged current, DRX = 5[16], AT+UPSV=1, USB interface disconnected	All		1.2		mA
	Averaged current, DRX = 5[16], AT+UPSV=1, USB interface connected and suspended	All		1.6		mA
2G Active-Mode (Power Saving disabled by AT+UPSV, Module registered with network)	Averaged current, DRX = 5[16], AT+UPSV=0, USB interface disconnected	All		14.7		mA
	Averaged current, DRX = 5[16], AT+UPSV=0, USB interface connected and not suspended	All		34.3		mA
GSM Connected Mode (Tx / Rx call enabled)	Peak current[17] during a 1-slot Tx burst Maximum Tx power (32.5 dBm typ.)	GSM 850		1.50	1.90	A
		EGSM 900		1.55	1.90	A
	Averaged current, 1 Tx + 1 Rx slot Maximum Tx power (32.5 dBm typ.)	GSM 850		200		mA
		EGSM 900		215		mA
	Averaged current, 1 Tx + 1 Rx slot Maximum Tx power (29.5 dBm typ.)	DCS 1800		140		mA
		PCS 1900		130		mA
GPRS Connected Mode (Tx / Rx call enabled)	Averaged current, 4 Tx + 1 Rx slots Maximum Tx power (30.5 dBm typ.)[18]	GSM 850		540		mA
		EGSM 900		580		mA
	Averaged current, 4 Tx + 1 Rx slots Maximum Tx power (27.5 dBm typ.)[18]	DCS 1800		360		mA
		PCS 1900		340		mA
3G Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV, Module registered with network)	Averaged current, DRX = 9[19], AT+UPSV=2 or 3, USB interface disconnected	All		0.9		mA
	Averaged current, DRX = 7[20], AT+UPSV=1, USB interface disconnected	All		1.3		mA
	Averaged current, DRX = 7[20], AT+UPSV=1, USB interface connected and suspended	All		1.7		mA
3G Active-Mode (Power Saving disabled by AT+UPSV, Module registered with network)	Averaged current, DRX = 7[20], AT+UPSV=0, USB interface disconnected	All		14.1		mA
	Averaged current, DRX = 7[20], AT+UPSV=0, USB interface connected and not suspended	All		33.6		mA
UMTS Connected Mode (Tx / Rx call enabled)	Averaged current, 12.2 kb/s UL, 12.2 kb/s DL Tx power = 0 dBm	Band I (2100)		145		mA
		Band II (1900)		150		mA
		Band V (850)		140		mA
		Band VIII (900)		140		mA
	Averaged current, 12.2 kb/s UL, 12.2 kb/s DL Maximum Tx power (22.5 dBm typ.)	Band I (2100)		610		mA
		Band II (1900)		640		mA
		Band V (850)		560		mA
		Band VIII (900)		590		mA
HSDPA Connected Mode (Tx / Rx call enabled)	Averaged current, Max. DL data rate (HSDPA)Maximum Tx power (22.5 dBm typ.)	Band I (2100)		690		mA
		Band II (1900)		720		mA
		Band V (850)		640		mA
		Band VIII (900)		670		mA
HSUPA or HSPA Connected Mode (Tx / Rx call enabled)	Averaged current, Max. UL data rate (HSUPA) or Maximum both UL and DL data rates (HSPA)Maximum Tx power (21.0 dBm typ.)	Band I (2100)		585		mA
		Band II (1900)		615		mA
		Band V (850)		535		mA
		Band VIII (900)		565		mA

Table 12: VCC current consumption

[13] Typical values with a matched antenna
[14] Maximum values with a mismatched antenna
[15] Module is registered with the network, with a paging period of 2.12 s (2G network DRX setting = 9), with none neighbour cell.
[16] Module is registered with the network, with a paging period of 1.18 s (2G network DRX setting = 5), with 16 neighbour cells.
[17] It is recommended to use this figure to dimension maximum current capability of power supply.
[18] Condition for GPRS multi-slot output power: Multi-Slot Power Reduction profile 2 (+UDCONF=40 AT command default value).
[19] Module is registered with the network, with a paging period of 5.12 s (3G network DRX setting = 9).
[20] Module is registered with the network, with a paging period of 1.28 s (3G network DRX setting = 7).

4.2.4 RF characteristics

Parameter		Min.	Max.	Unit	Remarks
Frequency range GSM 850	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range E-GSM 900	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range DCS 1800	Uplink	1710	1785	MHz	Module transmit
	Downlink	1805	1880	MHz	Module receive
Frequency range PCS 1900	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 850 (band V)	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range UMTS 900 (band VIII)	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range UMTS 1900 (band II)	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 2100 (band I)	Uplink	1920	1980	MHz	Module transmit
	Downlink	2110	2170	MHz	Module receive

Table 13: Operating RF frequency bands

Parameter	Min.	Typ.	Max.	Unit	Remarks
Receiver input sensitivity GSM 850 / E-GSM 900		-109.0		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity DCS 1800 / PCS 1900		-109.0		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity UMTS 850 (band V)		-111.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 900 (band VIII)		-110.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 1900 (band II)		-110.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 2100 (band I)		-110.0		dBm	Downlink RF level for RMC @ BER < 0.1 %

Condition: 50 Ω source

Table 14: Receiver sensitivity performance

Parameter	Min.	Typ.	Max.	Unit	Remarks
Maximum output power GSM 850 / E-GSM 900		32.5		dBm	Uplink burst RF power for GSM or GPRS 1-slot TCH at PCL 5 or Gamma 3
		32.5		dBm	Uplink burst RF power for GPRS 2-slot TCH at Gamma 3
		31.7		dBm	Uplink burst RF power for GPRS 3-slot TCH at Gamma 3
		30.5		dBm	Uplink burst RF power for GPRS 4-slot TCH at Gamma 3
Maximum output power DCS 1800 / PCS 1900		29.5		dBm	Uplink burst RF power for GSM or GPRS 1-slot TCH at PCL 0 or Gamma 3
		29.5		dBm	Uplink burst RF power for GPRS 2-slot TCH at Gamma 3
		28.7		dBm	Uplink burst RF power for GPRS 3-slot TCH at Gamma 3
		27.5		dBm	Uplink burst RF power for GPRS 4-slot TCH at Gamma 3
Maximum output power UMTS 850 (Band V)		22.5		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 900 (Band VIII)		22.5		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 1900 (Band II)		22.5		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 2100 (Band I)		22.5		dBm	Uplink continuous RF power for RMC at maximum power

Condition for all parameters: 50 Ω output load
Condition for GPRS multi-slot output power: Multi-Slot Power Reduction profile 2 (+UDCONF=40 AT command default value)

Table 15: Transmitter maximum output power

4.2.5 ANT_DET pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
ANT_DET	Output DC current pulse value		10		µA	
	Output DC current pulse time length		128		µs	

Table 16: ANT_DET pin characteristics

4.2.6 PWR_ON pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
PWR_ON	Internal supply for Power-On Input Signal	1.71	1.80	1.89	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.65	V	High input impedance (no internal pull-up)
	H-level input	1.50		4.40	V	High input impedance (no internal pull-up)
	L-level input current		-6		µA	
	PWR_ON low time to switch-on the module	50		80	µs	
	PWR_ON low time to switch-off the module	1000			ms	

Table 17: PWR_ON pin characteristics (POS domain)

4.2.7 RESET_N pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
RESET_N	Internal supply for External Reset Input Signal	1.71	1.80	1.89	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.51	V	
	H-level input	1.32		2.01	V	
	L-level input current		-180		µA	
	Pull-up resistance		10		kΩ	Internal pull-up to RTC supply (V_BCKP)
	RESET_N low time to perform a proper reset	50			ms	

Table 18: RESET_N pin characteristics (ERS domain)

4.2.8 (U)SIM pins

The SIM pins are a dedicated interface to the external SIM card/chip. The electrical characteristics fulfill regulatory specification requirements. The values in Table 19 are for information only.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Low-level input	0.00		0.35	V	VSIM = 1.80 V
	0.00		0.57	V	VSIM = 2.90 V
High-level input	1.29		3.30	V	VSIM = 1.80 V
	2.07		3.30	V	VSIM = 2.90 V
Low-level output		0.00	0.35	V	VSIM = 1.80 V, Max value at I_{OL} = +1.0 mA
		0.00	0.35	V	VSIM = 2.90 V, Max value at I_{OL} = +1.0 mA
High-level output	1.26	1.80		V	VSIM = 1.80 V, Min value at I_{OH} = -1.0 mA
	2.03	2.90		V	VSIM = 2.90 V, Min value at I_{OH} = -1.0 mA
Input/Output leakage current			0.7	µA	0.2V < V_{IN} < 3.3V
Internal pull-up resistor on SIM_IO to VSIM		4.7		kΩ	
Clock frequency on SIM_CLK		3.25		MHz	

Table 19: (U)SIM pins characteristics (SIM domain)

4.2.9 Generic Digital Interfaces pins

Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for GDI domain	1.73	1.80	1.87	V	Generic Digital Interfaces supply (V_INT)
Input characteristic: L-level input	-0.20		0.35	V	
Input characteristic: H-level input	1.31		1.93	V	
Output characteristics: L-level output		0.00	0.20	V	Max value at I_{OL} = +0.1 mA for driver class A
		0.00	0.35	V	Max value at I_{OL} = +6.0 mA for driver class A
		0.00	0.20	V	Max value at I_{OL} = +0.1 mA for driver class B
		0.00	0.35	V	Max value at I_{OL} = +4.0 mA for driver class B
		0.00	0.20	V	Max value at I_{OL} = +0.1 mA for driver class C
		0.00	0.35	V	Max value at I_{OL} = +2.0 mA for driver class C
		0.00	0.45	V	Max value at I_{OL} = +2.0 mA for driver class C_0
		0.00	0.20	V	Max value at I_{OL} = +0.1mA for driver class D
		0.00	0.35	V	Max value at I_{OL} = +1.0 mA for driver class D
		0.00	0.20	V	Max value at I_{OL} = +0.1 mA for driver class E
Output characteristics: H-level output	1.45	1.80		V	Min value at I_{OH} = -6.0 mA for driver class A
	1.60	1.80		V	Min value at I_{OH} = -0.1 mA for driver class A
	1.45	1.80		V	Min value at I_{OH} = -4.0 mA for driver class B
	1.60	1.80		V	Min value at I_{OH} = -0.1 mA for driver class B
	1.45	1.80		V	Min value at I_{OH} = -2.0 mA for driver class C
	1.60	1.80		V	Min value at I_{OH} = -0.1 mA for driver class C
	1.35	1.80		V	Min value at I_{OH} = -2.0 mA for driver class C_0
	1.45	1.80		V	Min value at I_{OH} = -1.0 mA for driver class D
	1.60	1.80		V	Min value at I_{OH} = -0.1 mA for driver class D
	1.60	1.80		V	Min value at I_{OH} = -0.1 mA for driver class E
Input/Output leakage current			0.7	µA	0.2 V < V_{IN} < 1.93 V
Pull-up input current			-240	µA	PU Class a
			-150	µA	PU Class b
			-125	µA	PU Class c
Pull-down input current			+200	µA	PD Class a
			+150	µA	PD Class b
			+45	µA	PD Class c

Table 20: Generic Digital Interfaces pins characteristics (GDI domain)

4.2.9.1 AC characteristics of digital audio interfaces pins

The 4-wire I^2S digital audio interface can be configured in 4 different modes:

- Normal I^2S mode – Master mode
- Normal I^2S mode – Slave mode
- PCM mode – Master mode
- PCM mode – Slave mode

AC characteristics of the 4 different modes of the I^2S digital audio interface are reported as follows.

Normal I²S mode – Master mode

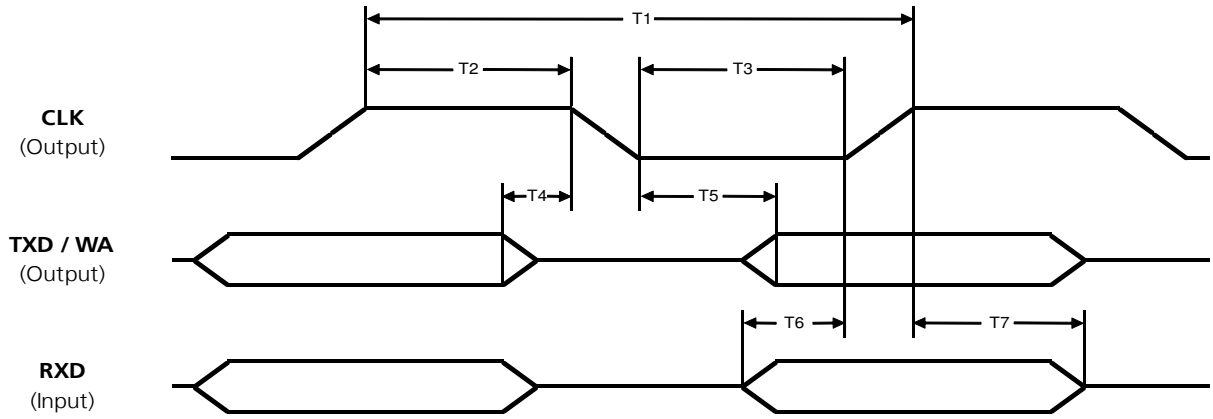

Figure 4: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 2,4,6,8,10,12) and Master mode enabled

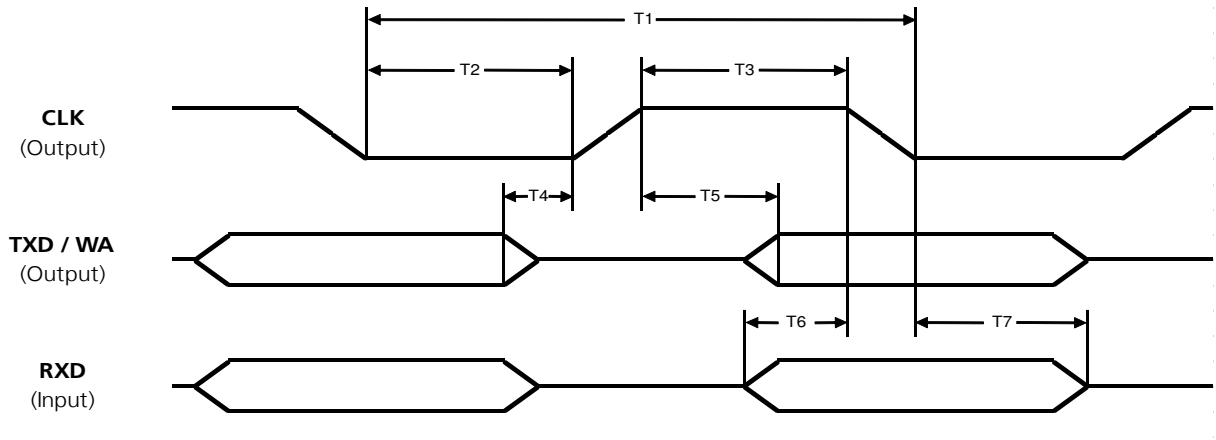

Figure 5: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 3,5,7,9,11,13) and Master mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I²S clock period	3.902	3.906		µs	<I2S_sample_rate>=0
		2.830	2.834		µs	<I2S_sample_rate>=1
		2.600	2.604		µs	<I2S_sample_rate>=2
		1.949	1.953		µs	<I2S_sample_rate>=3
		1.413	1.417		µs	<I2S_sample_rate>=4
		1.298	1.302		µs	<I2S_sample_rate>=5
		0.973	0.977		µs	<I2S_sample_rate>=6
		0.705	0.709		µs	<I2S_sample_rate>=7
		0.647	0.651		µs	<I2S_sample_rate>=8
1/T1	I²S clock frequency		256.0	256.3	kHz	<I2S_sample_rate>=0
			352.8	353.3	kHz	<I2S_sample_rate>=1
			384.0	384.6	kHz	<I2S_sample_rate>=2
			512.0	513.1	kHz	<I2S_sample_rate>=3
			705.6	707.6	kHz	<I2S_sample_rate>=4
			768.0	770.4	kHz	<I2S_sample_rate>=5
			1024	1028	kHz	<I2S_sample_rate>=6
			1411	1419	kHz	<I2S_sample_rate>=7
			1536	1545	kHz	<I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T2	I²S clock high time	1.933	1.953		µs	<I2S_sample_rate>=0
		1.397	1.417		µs	<I2S_sample_rate>=1
		1.282	1.302		µs	<I2S_sample_rate>=2
		0.957	0.977		µs	<I2S_sample_rate>=3
		0.689	0.709		µs	<I2S_sample_rate>=4
		0.631	0.651		µs	<I2S_sample_rate>=5
		0.468	0.488		µs	<I2S_sample_rate>=6
		0.334	0.354		µs	<I2S_sample_rate>=7
		0.306	0.326		µs	<I2S_sample_rate>=8
T3	I²S clock low time	1.933	1.953		µs	<I2S_sample_rate>=0
		1.397	1.417		µs	<I2S_sample_rate>=1
		1.282	1.302		µs	<I2S_sample_rate>=2
		0.957	0.977		µs	<I2S_sample_rate>=3
		0.689	0.709		µs	<I2S_sample_rate>=4
		0.631	0.651		µs	<I2S_sample_rate>=5
		0.468	0.488		µs	<I2S_sample_rate>=6
		0.334	0.354		µs	<I2S_sample_rate>=7
		0.306	0.326		µs	<I2S_sample_rate>=8
	I²S word alignment period		125.0		µs	<I2S_sample_rate>=0
			90.70		µs	<I2S_sample_rate>=1
			83.33		µs	<I2S_sample_rate>=2
			62.50		µs	<I2S_sample_rate>=3
			45.35		µs	<I2S_sample_rate>=4
			41.67		µs	<I2S_sample_rate>=5
			31.25		µs	<I2S_sample_rate>=6
			22.68		µs	<I2S_sample_rate>=7
			20.83		µs	<I2S_sample_rate>=8
	I²S word alignment frequency		8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
			48.00		kHz	<I2S_sample_rate>=8
T4	I²S TXD invalid before I²S CLK high end (before shifting edge of I²S CLK)			24	ns	<I2S_mode> = 2,4,6,8,10,12
	I²S TXD invalid before I²S CLK low end (before shifting edge of I²S CLK)			24	ns	<I2S_mode> = 3,5,7,9,11,13
T5	I²S TXD valid after I²S CLK low begin (after shifting edge of I²S CLK)			32	ns	<I2S_mode> = 2,4,6,8,10,12
	I²S TXD valid after I²S CLK high begin (after shifting edge of I²S CLK)			32	ns	<I2S_mode> = 3,5,7,9,11,13
T6	I²S RXD setup time before I²S CLK low end (before latching edge of I²S CLK)	60			ns	<I2S_mode> = 2,4,6,8,10,12
	I²S RXD setup time before I²S CLK high end (before latching edge of I²S CLK)	60			ns	<I2S_mode> = 3,5,7,9,11,13
T7	I²S RXD hold time after I²S CLK high begin (after latching edge of I²S CLK)	10			ns	<I2S_mode> = 2,4,6,8,10,12
	I²S RXD hold time after I²S CLK low begin (after latching edge of I²S CLK)	10			ns	<I2S_mode> = 3,5,7,9,11,13

Table 21: AC characteristics of digital audio interface in Normal I²S mode and Master mode enabled

Normal I²S mode – Slave mode

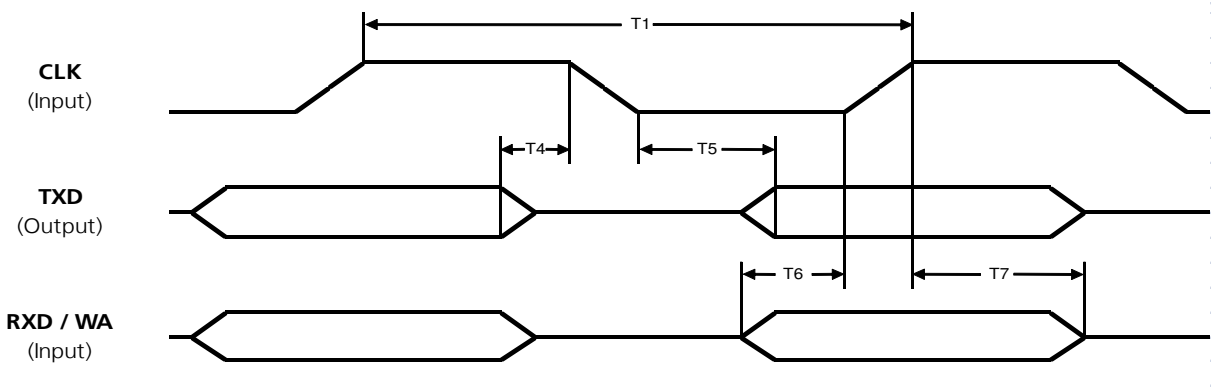

Figure 6: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 2,4,6,8,10,12) and Slave mode enabled

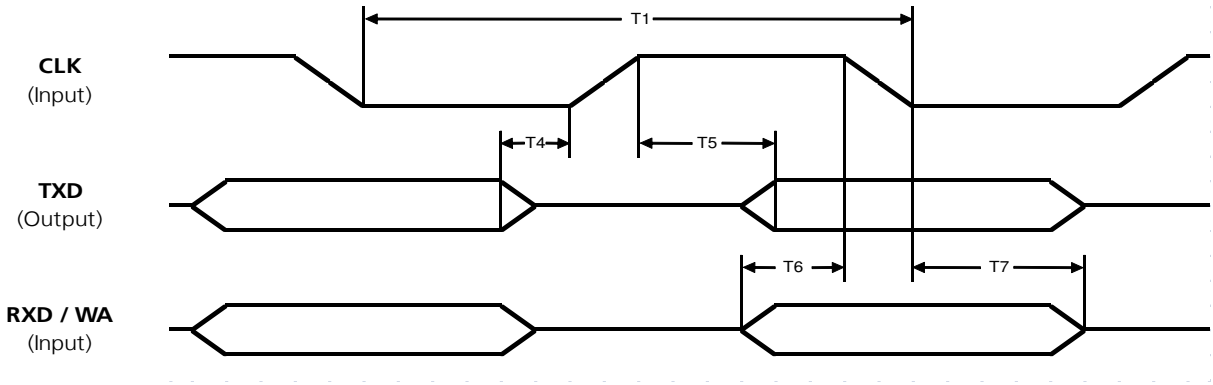

Figure 7: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 3,5,7,9,11,13) and Slave mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I²S clock period	3.906			µs	<I2S_sample_rate>=0
		2.834			µs	<I2S_sample_rate>=1
		2.604			µs	<I2S_sample_rate>=2
		1.953			µs	<I2S_sample_rate>=3
		1.417			µs	<I2S_sample_rate>=4
		1.302			µs	<I2S_sample_rate>=5
		0.977			µs	<I2S_sample_rate>=6
		0.709			µs	<I2S_sample_rate>=7
		0.651			µs	<I2S_sample_rate>=8
1/T1	I²S clock frequency			256.0	kHz	<I2S_sample_rate>=0
				352.8	kHz	<I2S_sample_rate>=1
				384.0	kHz	<I2S_sample_rate>=2
				512.0	kHz	<I2S_sample_rate>=3
				705.6	kHz	<I2S_sample_rate>=4
				768.0	kHz	<I2S_sample_rate>=5
				1024	kHz	<I2S_sample_rate>=6
				1411	kHz	<I2S_sample_rate>=7
				1536	kHz	<I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
	I²S word alignment period	125.0			µs	<I2S_sample_rate>=0
		90.70			µs	<I2S_sample_rate>=1
		83.33			µs	<I2S_sample_rate>=2
		62.50			µs	<I2S_sample_rate>=3
		45.35			µs	<I2S_sample_rate>=4
		41.67			µs	<I2S_sample_rate>=5
		31.25			µs	<I2S_sample_rate>=6
		22.68			µs	<I2S_sample_rate>=7
		20.83			µs	<I2S_sample_rate>=8
	I²S word alignment frequency			8.000	kHz	<I2S_sample_rate>=0
				11.03	kHz	<I2S_sample_rate>=1
				12.00	kHz	<I2S_sample_rate>=2
				16.00	kHz	<I2S_sample_rate>=3
				22.05	kHz	<I2S_sample_rate>=4
				24.00	kHz	<I2S_sample_rate>=5
				32.00	kHz	<I2S_sample_rate>=6
				44.10	kHz	<I2S_sample_rate>=7
				48.00	kHz	<I2S_sample_rate>=8
T4	I²S TXD invalid before I²S CLK falling edge (before shifting edge of I²S CLK)			24	ns	<I2S_mode> = 2,4,6,8,10,12
	I²S TXD invalid before I²S CLK rising edge (before shifting edge of I²S CLK)			24	ns	<I2S_mode> = 3,5,7,9,11,13
T5	I²S TXD valid after I²S CLK falling edge (after shifting edge of I²S CLK)			32	ns	<I2S_mode> = 2,4,6,8,10,12
	I²S TXD valid after I²S CLK rising edge (after shifting edge of I²S CLK)			32	ns	<I2S_mode> = 3,5,7,9,11,13
T6	I²S RXD setup time before I²S CLK rising edge (before latching edge of I²S CLK)	60			ns	<I2S_mode> = 2,4,6,8,10,12
	I²S RXD setup time before I²S CLK falling edge (before latching edge of I²S CLK)	60			ns	<I2S_mode> = 3,5,7,9,11,13
T7	I²S RXD hold time after I²S CLK rising edge (after latching edge of I²S CLK)	10			ns	<I2S_mode> = 2,4,6,8,10,12
	I²S RXD hold time after I²S CLK falling edge (after latching edge of I²S CLK)	10			ns	<I2S_mode> = 3,5,7,9,11,13

Table 22: AC characteristics of digital audio interface in Normal I²S mode and Slave mode enabled

PCM mode – Master mode

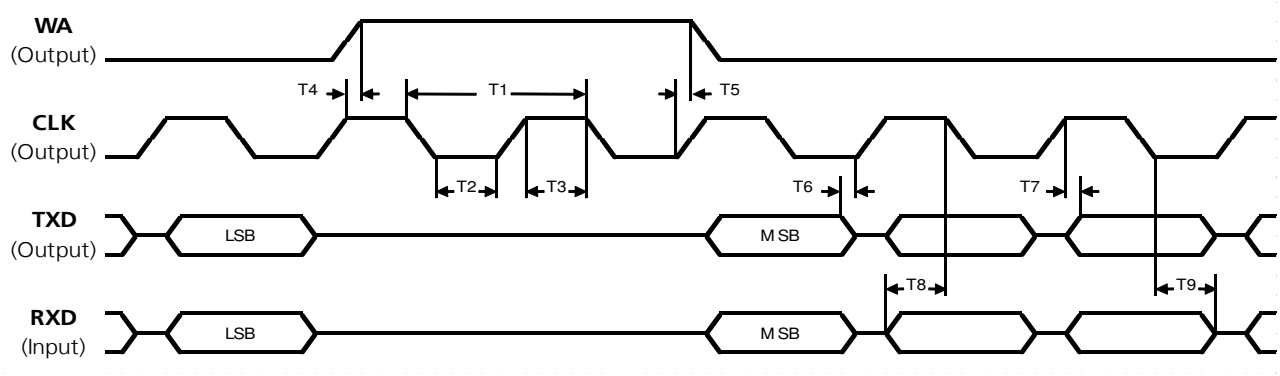

Figure 8: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0) and Master mode enabled

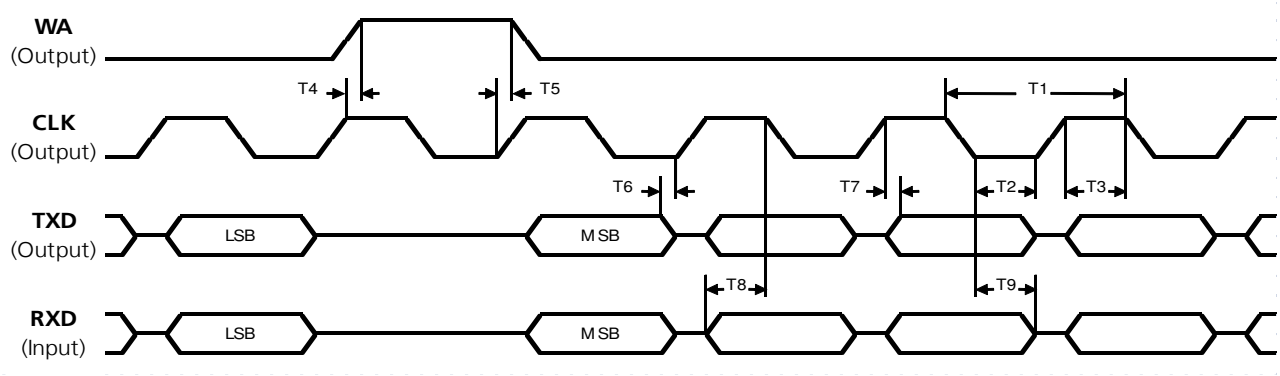

Figure 9: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 1) and Master mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I²S clock period	6.940	6.944		µs	<I2S_mode>=0, <I2S_sample_rate>=0
		7.349	7.353		µs	<I2S_mode>=1, <I2S_sample_rate>=0
		5.035	5.039		µs	<I2S_mode>=0, <I2S_sample_rate>=1
		5.331	5.335		µs	<I2S_mode>=1, <I2S_sample_rate>=1
		4.626	4.630		µs	<I2S_mode>=0, <I2S_sample_rate>=2
		4.898	4.902		µs	<I2S_mode>=1, <I2S_sample_rate>=2
		3.468	3.472		µs	<I2S_mode>=0, <I2S_sample_rate>=3
		3.672	3.676		µs	<I2S_mode>=1, <I2S_sample_rate>=3
		2.516	2.520		µs	<I2S_mode>=0, <I2S_sample_rate>=4
		2.664	2.668		µs	<I2S_mode>=1, <I2S_sample_rate>=4
		2.311	2.315		µs	<I2S_mode>=0, <I2S_sample_rate>=5
		2.447	2.451		µs	<I2S_mode>=1, <I2S_sample_rate>=5
		1.732	1.736		µs	<I2S_mode>=0, <I2S_sample_rate>=6
		1.834	1.838		µs	<I2S_mode>=1, <I2S_sample_rate>=6
		1.256	1.260		µs	<I2S_mode>=0, <I2S_sample_rate>=7
		1.330	1.334		µs	<I2S_mode>=1, <I2S_sample_rate>=7
		1.153	1.157		µs	<I2S_mode>=0, <I2S_sample_rate>=8
		1.221	1.225		µs	<I2S_mode>=1, <I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
1/T1	I²S clock frequency		144.0	144.1	kHz	<I2S_mode>=0, <I2S_sample_rate>=0
			136.0	136.1	kHz	<I2S_mode>=1, <I2S_sample_rate>=0
			198.5	198.6	kHz	<I2S_mode>=0, <I2S_sample_rate>=1
			187.4	187.6	kHz	<I2S_mode>=1, <I2S_sample_rate>=1
			216.0	216.2	kHz	<I2S_mode>=0, <I2S_sample_rate>=2
			204.0	204.2	kHz	<I2S_mode>=1, <I2S_sample_rate>=2
			288.0	288.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=3
			272.0	272.3	kHz	<I2S_mode>=1, <I2S_sample_rate>=3
			396.9	397.5	kHz	<I2S_mode>=0, <I2S_sample_rate>=4
			374.9	375.4	kHz	<I2S_mode>=1, <I2S_sample_rate>=4
			432.0	432.7	kHz	<I2S_mode>=0, <I2S_sample_rate>=5
			408.0	408.7	kHz	<I2S_mode>=1, <I2S_sample_rate>=5
			576.0	577.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=6
			544.0	545.2	kHz	<I2S_mode>=1, <I2S_sample_rate>=6
			793.8	796.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=7
			749.7	752.0	kHz	<I2S_mode>=1, <I2S_sample_rate>=7
			864.0	867.0	kHz	<I2S_mode>=0, <I2S_sample_rate>=8
			816.0	818.7	kHz	<I2S_mode>=1, <I2S_sample_rate>=8
T2	I²S clock low time	3.452	3.472		µs	<I2S_mode>=0, <I2S_sample_rate>=0
		3.656	3.676		µs	<I2S_mode>=1, <I2S_sample_rate>=0
		2.500	2.520		µs	<I2S_mode>=0, <I2S_sample_rate>=1
		2.648	2.668		µs	<I2S_mode>=1, <I2S_sample_rate>=1
		2.295	2.315		µs	<I2S_mode>=0, <I2S_sample_rate>=2
		2.431	2.451		µs	<I2S_mode>=1, <I2S_sample_rate>=2
		1.716	1.736		µs	<I2S_mode>=0, <I2S_sample_rate>=3
		1.818	1.838		µs	<I2S_mode>=1, <I2S_sample_rate>=3
		1.240	1.260		µs	<I2S_mode>=0, <I2S_sample_rate>=4
		1.314	1.334		µs	<I2S_mode>=1, <I2S_sample_rate>=4
		1.137	1.157		µs	<I2S_mode>=0, <I2S_sample_rate>=5
		1.205	1.225		µs	<I2S_mode>=1, <I2S_sample_rate>=5
		0.848	0.868		µs	<I2S_mode>=0, <I2S_sample_rate>=6
		0.899	0.919		µs	<I2S_mode>=1, <I2S_sample_rate>=6
		0.610	0.630		µs	<I2S_mode>=0, <I2S_sample_rate>=7
		0.647	0.667		µs	<I2S_mode>=1, <I2S_sample_rate>=7
		0.559	0.579		µs	<I2S_mode>=0, <I2S_sample_rate>=8
		0.593	0.613		µs	<I2S_mode>=1, <I2S_sample_rate>=8
T3	I²S clock high time	3.452	3.472		µs	<I2S_mode>=0, <I2S_sample_rate>=0
		3.656	3.676		µs	<I2S_mode>=1, <I2S_sample_rate>=0
		2.500	2.520		µs	<I2S_mode>=0, <I2S_sample_rate>=1
		2.648	2.668		µs	<I2S_mode>=1, <I2S_sample_rate>=1
		2.295	2.315		µs	<I2S_mode>=0, <I2S_sample_rate>=2
		2.431	2.451		µs	<I2S_mode>=1, <I2S_sample_rate>=2
		1.716	1.736		µs	<I2S_mode>=0, <I2S_sample_rate>=3
		1.818	1.838		µs	<I2S_mode>=1, <I2S_sample_rate>=3
		1.240	1.260		µs	<I2S_mode>=0, <I2S_sample_rate>=4
		1.314	1.334		µs	<I2S_mode>=1, <I2S_sample_rate>=4
		1.137	1.157		µs	<I2S_mode>=0, <I2S_sample_rate>=5
		1.205	1.225		µs	<I2S_mode>=1, <I2S_sample_rate>=5
		0.848	0.868		µs	<I2S_mode>=0, <I2S_sample_rate>=6
		0.899	0.919		µs	<I2S_mode>=1, <I2S_sample_rate>=6
		0.610	0.630		µs	<I2S_mode>=0, <I2S_sample_rate>=7
		0.647	0.667		µs	<I2S_mode>=1, <I2S_sample_rate>=7

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
		0.559	0.579		µs	<I2S_mode>=0, <I2S_sample_rate>=8
		0.593	0.613		µs	<I2S_mode>=1, <I2S_sample_rate>=8
	I^2S word alignment period		125.0		µs	<I2S_sample_rate>=0
			90.70		µs	<I2S_sample_rate>=1
			83.33		µs	<I2S_sample_rate>=2
			62.50		µs	<I2S_sample_rate>=3
			45.35		µs	<I2S_sample_rate>=4
			41.67		µs	<I2S_sample_rate>=5
			31.25		µs	<I2S_sample_rate>=6
			22.68		µs	<I2S_sample_rate>=7
			20.83		µs	<I2S_sample_rate>=8
	I^2S word alignment frequency		8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
			48.00		kHz	<I2S_sample_rate>=8
T4	I^2S CLK high begin to I^2S WA high begin	-24		32	ns	<I2S_mode> = 0
T5	I^2S CLK low end to I^2S WA high end	-24		32	ns	<I2S_mode> = 0
T6	I^2S TXD invalid before I^2S CLK low end			24	ns	<I2S_mode> = 0
T7	I^2S TXD valid after I^2S CLK high begin			22	ns	<I2S_mode> = 0
T8	I^2S RXD setup time before I^2S CLK high end	60			ns	<I2S_mode> = 0
T9	I^2S RXD hold time after I^2S CLK low begin	12			ns	<I2S_mode> = 0

Table 23: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0,1) and Master mode enabled

PCM mode – Slave mode

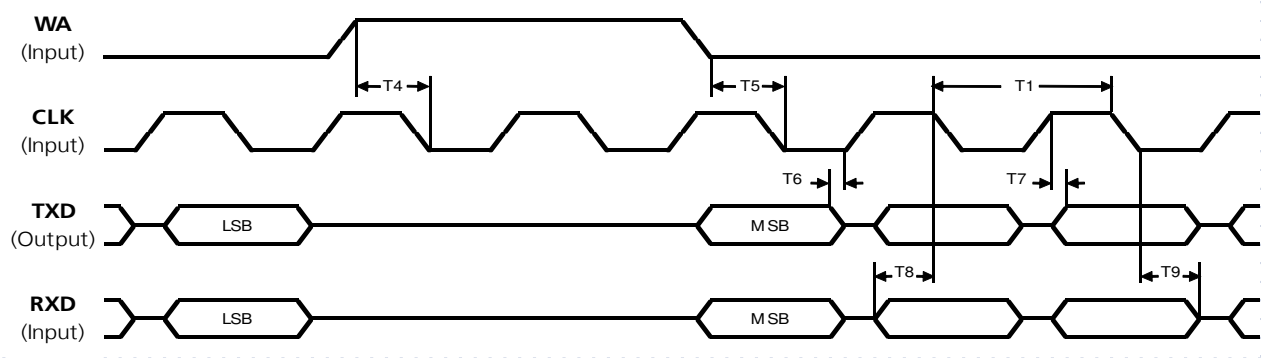

Figure 10: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0) and Slave mode enabled

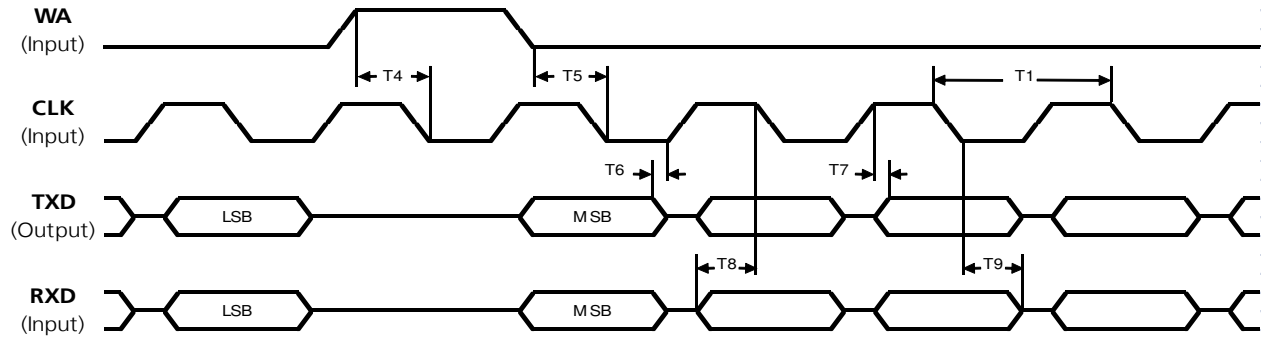

Figure 11: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 1) and Slave mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I^2S clock period	6.944			µs	<I2S_mode>=0, <I2S_sample_rate>=0
		7.353			µs	<I2S_mode>=1, <I2S_sample_rate>=0
		5.039			µs	<I2S_mode>=0, <I2S_sample_rate>=1
		5.335			µs	<I2S_mode>=1, <I2S_sample_rate>=1
		4.630			µs	<I2S_mode>=0, <I2S_sample_rate>=2
		4.902			µs	<I2S_mode>=1, <I2S_sample_rate>=2
		3.472			µs	<I2S_mode>=0, <I2S_sample_rate>=3
		3.676			µs	<I2S_mode>=1, <I2S_sample_rate>=3
		2.520			µs	<I2S_mode>=0, <I2S_sample_rate>=4
		2.668			µs	<I2S_mode>=1, <I2S_sample_rate>=4
		2.315			µs	<I2S_mode>=0, <I2S_sample_rate>=5
		2.451			µs	<I2S_mode>=1, <I2S_sample_rate>=5
		1.736			µs	<I2S_mode>=0, <I2S_sample_rate>=6
		1.838			µs	<I2S_mode>=1, <I2S_sample_rate>=6
		1.260			µs	<I2S_mode>=0, <I2S_sample_rate>=7
		1.334			µs	<I2S_mode>=1, <I2S_sample_rate>=7
		1.157			µs	<I2S_mode>=0, <I2S_sample_rate>=8
		1.225			µs	<I2S_mode>=1, <I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
1/T1	I²S clock frequency	144.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=0
		136.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=0
		198.5			kHz	<I2S_mode>=0, <I2S_sample_rate>=1
		187.4			kHz	<I2S_mode>=1, <I2S_sample_rate>=1
		216.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=2
		204.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=2
		288.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=3
		272.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=3
		396.9			kHz	<I2S_mode>=0, <I2S_sample_rate>=4
		374.9			kHz	<I2S_mode>=1, <I2S_sample_rate>=4
		432.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=5
		408.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=5
		576.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=6
		544.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=6
		793.8			kHz	<I2S_mode>=0, <I2S_sample_rate>=7
		749.7			kHz	<I2S_mode>=1, <I2S_sample_rate>=7
		864.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=8
		816.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=8
	I²S word alignment period		125.0		µs	<I2S_sample_rate>=0
			90.70		µs	<I2S_sample_rate>=1
			83.33		µs	<I2S_sample_rate>=2
			62.50		µs	<I2S_sample_rate>=3
			45.35		µs	<I2S_sample_rate>=4
			41.67		µs	<I2S_sample_rate>=5
			31.25		µs	<I2S_sample_rate>=6
			22.68		µs	<I2S_sample_rate>=7
			20.83		µs	<I2S_sample_rate>=8
	I²S word alignment frequency		8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
			48.00		kHz	<I2S_sample_rate>=8
T4	I²S WA high begin before I²S CLK low begin (latching edge of I²S CLK)	36			ns	<I2S_mode> = 0
T5	I²S WA low begin before I²S CLK low begin (latching edge of I²S CLK)	36			ns	<I2S_mode> = 0
T6	I²S TXD invalid before I²S CLK rising edge (shifting edge of I²S CLK)			12	ns	<I2S_mode> = 0
T7	I²S TXD valid after I²S CLK rising edge (shifting edge of I²S CLK)			79	ns	<I2S_mode> = 0
T8	I²S RXD setup time before I²S CLK falling edge (latching edge of I²S CLK)	22			ns	<I2S_mode> = 0
T9	I²S RXD hold time after I²S CLK falling edge (latching edge of I²S CLK)	24			ns	<I2S_mode> = 0

Table 24: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0,1) and Slave mode enabled

4.2.9.2 AC characteristics of Digital Clock Output pin

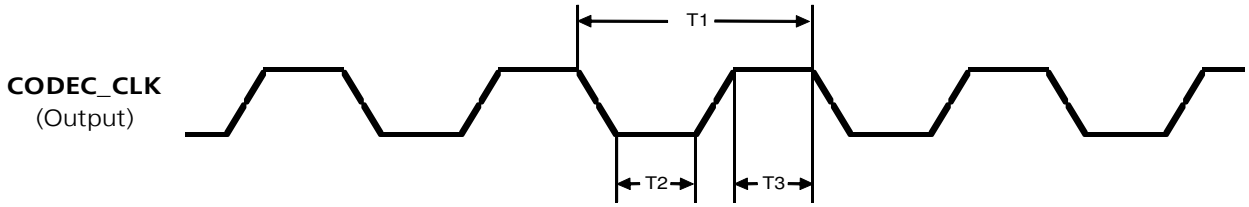

Figure 12: AC characteristics of CODEC_CLK digital clock output

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	CODEC_CLK clock period		38		ns	CODEC_CLK output set to 26 MHz
			77		ns	CODEC_CLK output set to 13 MHz
1/T1	CODEC_CLK clock frequency		26		MHz	CODEC_CLK output set to 26 MHz
			13		MHz	CODEC_CLK output set to 13 MHz
T2	CODEC_CLK clock low time	10			ns	CODEC_CLK output set to 26 MHz
		26			ns	CODEC_CLK output set to 13 MHz
T3	CODEC_CLK clock high time	10			ns	CODEC_CLK output set to 26 MHz
		26			ns	CODEC_CLK output set to 13 MHz

Table 25: AC characteristics of CODEC_CLK digital clock output

4.2.10 USB pins

USB data lines (**USB_D+** and **USB_D-**) are compliant to the USB 2.0 high-speed specification. See the Universal Serial Bus Revision 2.0 specification [11] for detailed electrical characteristics. The values in Table 26 related to USB 2.0 high-speed physical layer specifications are for information only.

Parameter	Min.	Typ.	Max.	Unit	Remarks
USB detection voltage on pin VUSB_DET	4.40	5.00	5.25	V	
Current sink at VUSB_DET		30		µA	
High-speed squelch detection threshold (input differential signal amplitude)	100		150	mV	
High speed disconnect detection threshold (input differential signal amplitude)	525		625	mV	
High-speed data signaling input common mode voltage range	-50		500	mV	
High-speed idle output level	-10		10	mV	
High-speed data signaling output high level	360		440	mV	
High-speed data signaling output low level	-10		10	mV	
Chirp J level (output differential voltage)	700		1100	mV	
Chirp K level (output differential voltage)	-900		-500	mV	

Table 26: USB pins characteristics

4.2.11 DDC (I^2C) pins

DDC (I^2C) lines (**SCL** and **SDA**) are compliant to the I^2C-bus standard mode specification. See the I^2C-bus Specifications [10] for detailed electrical characteristics. The values in Table 27 related to I^2C-bus standard mode specifications are for information only.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for DDC domain	1.73	1.80	1.87	V	Generic Digital Interfaces supply (V_INT)
L-level input	-0.20		0.35	V	
H-level input	1.31		1.93	V	
L-level output		0.00	0.35	V	Max value at I_{OL} = +1.0 mA
Input/Output leakage current			0.7	µA	0.2 V < V_{IN} < 1.93 V
Clock frequency on SCL		100		kHz	

Table 27: DDC (I^2C) pins characteristics (DDC domain)

5 Mechanical specifications

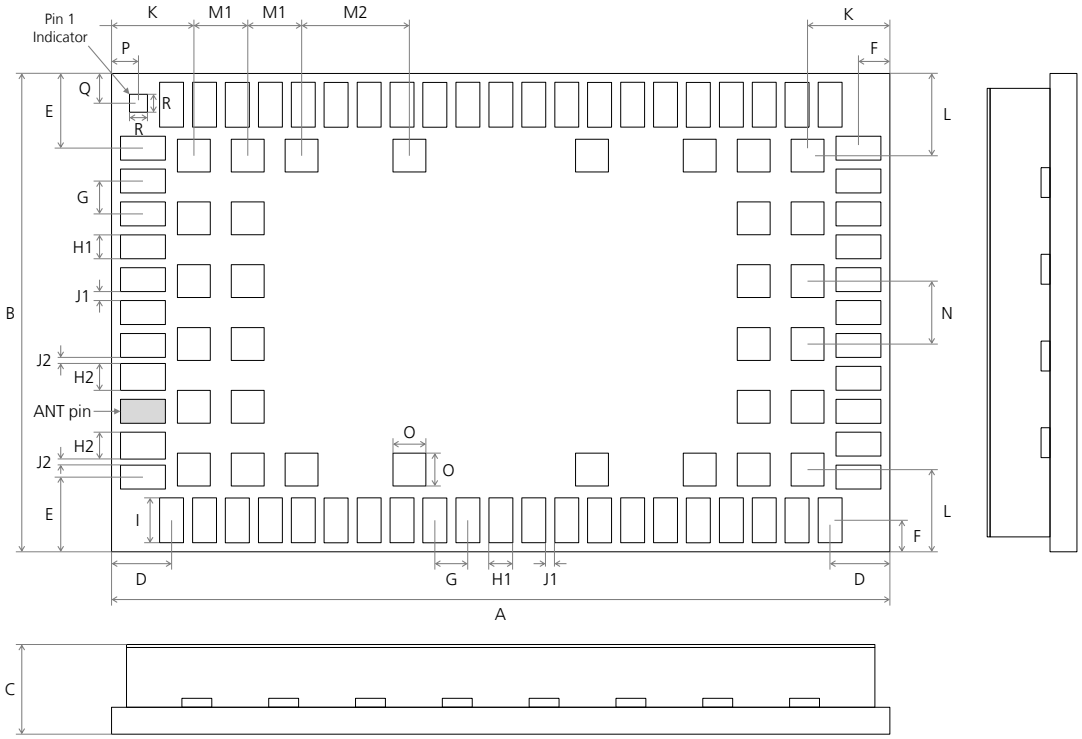

Figure 13: SARA-U2 series dimensions (bottom and sides views)

Parameter	Description	Typical		Tolerance	
A	Module Height [mm]	26.0	(1023.6 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
B	Module Width [mm]	16.0	(629.9 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
C	Module Thickness [mm]	3.0	(118.4 mil)	+0.25/-0.15	(+9.8/-5.9 mil)
D	Horizontal Edge to Lateral Pin Pitch [mm]	2.0	(78.7 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
E	Vertical Edge to Lateral Pin Pitch [mm]	2.5	(98.4 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
F	Edge to Lateral Pin Pitch [mm]	1.05	(41.3 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
G	Lateral Pin to Pin Pitch [mm]	1.1	(43.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
H1	Lateral Pin Height [mm]	0.8	(31.5 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
H2	Lateral Pin close to ANT Height [mm]	0.9	(35.4 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
I	Lateral Pin Width [mm]	1.5	(59.1 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
J1	Lateral Pin to Pin Distance [mm]	0.3	(11.8 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
J2	Lateral Pin to Pin close to ANT Distance [mm]	0.2	(7.9 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
K	Horizontal Edge to Central Pin Pitch [mm]	2.75	(108.3 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
L	Vertical Edge to Central Pin Pitch [mm]	2.75	(108.3 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
M1	Central Pin to Pin Horizontal Pitch [mm]	1.8	(70.9 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
M2	Central Pin to Pin Horizontal Pitch [mm]	3.6	(141.7 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
N	Central Pin to Pin Vertical Pitch [mm]	2.1	(82.7 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
O	Central Pin Height and Width [mm]	1.1	(43.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
P	Horizontal Edge to Pin 1 Indicator Pitch [mm]	0.9	(35.4 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
Q	Vertical Edge to Pin 1 Indicator Pitch [mm]	1.0	(39.4 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
R	Pin 1 Indicator Height and Width [mm]	0.6	(23.6 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
Weight	Module Weight [g]	< 3			

Table 28: SARA-U2 series dimensions

For information regarding Footprint and Paste Mask see the SARA-G3 and SARA-U2 series System Integration Manual [5].

6 Reliability tests and approvals

6.1 Reliability tests

Tests for product family qualifications are according to ISO 16750 “Road vehicles - Environmental conditions and testing for electrical and electronic equipment“, and appropriate standards.

6.2 Approvals

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" RoHS).

SARA-U2 modules are RoHS compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

Table 29 lists the SARA-U2 series main approvals.

Regulatory / Standard / Operator	SARA-U260-00S	SARA-U270-00S	SARA-U280-00S	SARA-U290-00S	SARA-U290-60S
GCF (Global Certification Forum)		•		•	•
PTCRB (Personal communications service Type Certification Review Board)	•		•		
R&TTE (Radio & Telecommunications Terminal Equipment EU Directive)		•		•	•
CE (Conformité Européenne, European Conformity)		•		•	•
FCC (United States Federal Communications Commission)	•		•		
IC (Industry Canada)	•		•		
SoftBank (Japanese network operator)					•

Table 29: SARA-U2 series main certification approvals

☞ For all the certificates of compliancy and for the complete list of approvals (including countries’ and network operators’ approvals) of SARA-U2 series modules, see our website, http://www.u-blox.com/.

7 Product handling & soldering

7.1 Packaging

SARA-U2 modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see u-blox Package Information Guide [12].

Figure 14: Reeled SARA-U2 modules

7.1.1 Reels

SARA-U2 modules are deliverable in quantities of 250 pieces on a reel. SARA-U2 modules are delivered using reel Type B as described in the u-blox Package Information Guide [12].

Parameter	Specification
Reel Type	B
Delivery Quantity	250

Table 30: Reel information for SARA-U2 modules

☞ Quantities of less than 250 pieces are also available. Contact u-blox for more information.

7.1.2 Tapes

Figure 15 specifies the dimensions and orientations of the tapes for SARA-U2 series module.

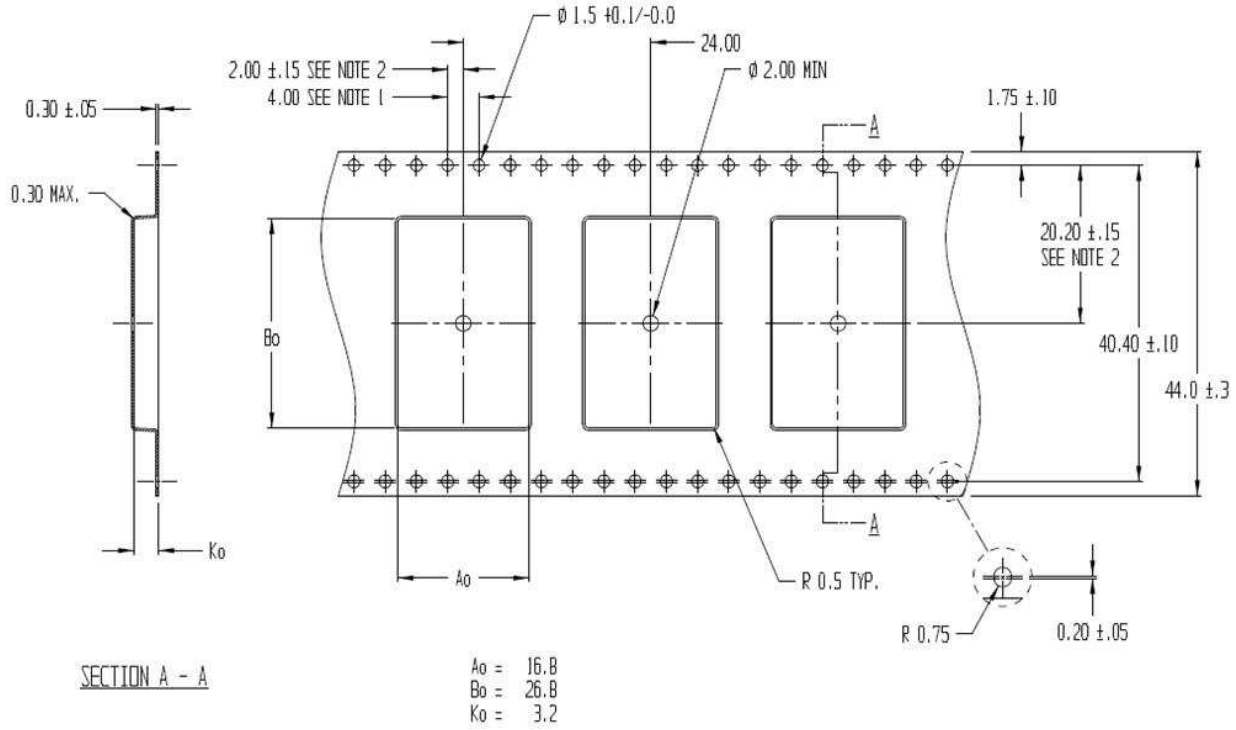

Figure 15: SARA-U2 series tape dimensions (mm)

Parameter	Value
A_0	16.8
B_0	26.8
K_0	3.2

Table 31: SARA-U2 series tape dimensions (mm)

Note 1: 10 sprocket hole pitch cumulative tolerance ± 0.2.

Note 2: pocket position relative to sprocket hole is measured as true position of pocket, not pocket hole.

Note 3: A_0 and B_0 are calculated on a plane at a distance "R" above the bottom of the pocket.

7.2 Moisture Sensitivity Levels

SARA-U2 modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. SARA-U2 modules are rated at MSL level 4. For more information regarding moisture sensitivity levels, labeling, storage and drying see the u-blox Package Information Guide [12].

For MSL standard see IPC/JEDEC J-STD-020 (can be downloaded from http://www.jedec.org/).

7.3 Reflow soldering

Reflow profiles are to be selected according to u-blox recommendations (see SARA-G3 and SARA-U2 series System Integration Manual [5]).

Failure to observe these recommendations can result in severe damage to the device!

7.4 ESD precautions

SARA-U2 modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling SARA-U2 modules without proper ESD protection may destroy or damage them permanently.

SARA-U2 modules are Electrostatic Sensitive Devices (ESD) and require special ESD precautions typically applied to ESD sensitive components.

Table 8 reports the maximum ESD ratings of the SARA-U2 module.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates SARA-U2 module.

ESD precautions should be implemented on the application board where the module is mounted, as described in SARA-G3 and SARA-U2 series System Integration Manual [5].

Failure to observe these precautions can result in severe damage to the device!

8 Default settings

Interface	AT settings	Comments
UART interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: • Channel 0: control channel • Channel 1 – 5: AT commands / data connection • Channel 6: GNSS tunneling • Channel 7: SAP (SIM Access Profile)
	AT+IPR=0	One-shot automatic baud rate detection enabled
	AT+ICF=3,1	Frame format: 8 bits, no parity, 1 stop bit ☞ Where AT+IPR=0 is the default value, the AT+ICF value in the profile is not applied (AT+IPR=0 overrules the AT+ICF setting) and the one-shot automatic frame detection is active.
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the module enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
USB interface	Enabled	7 USB CDCs (Communications Device Class) by default available: • USB1: AT and data • USB2: AT and data • USB3: AT and data • USB4: GNSS tunneling • USB5: Primary Log (diagnostic purpose) • USB6: Secondary Log (diagnostic purpose) • USB7: SAP (SIM Access Profile) Audio over USB capabilities can be enabled by specific AT command (see the u-blox AT Commands Manual [4]): the Audio Device Class provides a streaming interface, which transfers audio data on isochronous pipes (not supported by initial firmware release).
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the module enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
Power saving	AT+UPSV=0	Disabled
Network registration	AT+COPS=0	Self network registration

Table 32: SARA-U2 series default settings

See the u-blox AT Commands Manual [4] and the SARA-G3 and SARA-U2 series System Integration Manual [5] for information about further settings.

9 Labeling and ordering information

9.1 Product labeling

The labels of SARA-U2 series modules include important product information as described in this section.

Figure 16 illustrates the label of all the SARA-U2 series modules, and includes: u-blox logo, production lot, Pb-free marking, product Type Number, IMEI number, FCC and IC certification numbers (if applicable), CE marking with the Notified Body number and production country.

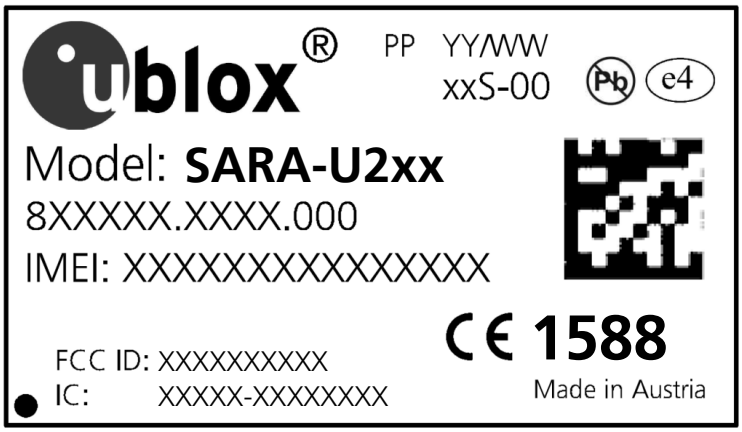

Figure 16: SARA-U2 series modules label

For information about the approval codes and for all the certificates of compliancy of SARA-U2 series modules, see our website, http://www.u-blox.com/.

9.2 Explanation of codes

Three different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all the u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 33 details these 3 different formats:

Format	Structure
Product Name	SARA-TGVV
Ordering Code	SARA-TGVV-TTQ
Type Number	SARA-TGVV-TTQ-XX

Table 33: Product code formats

Table 34 explains the parts of the product code.

Code	Meaning	Example
PPP(P)	Form factor (3 or 4 digit, typically 4 for cellular products)	SARA
TG	Platform (Technology and Generation) • Technology: G:GSM; U: HSUPA; L:LTE, C:CDMA 1xRTT; D:EV-DO • Generation: 1…9	U2
VV	Variant function set based on the same platform [00…99]	00
TT	Major product version [00…99]	00
Q	Quality grade/production site • S = standard • A = automotive	S
XX	Minor product version (not relevant for certification)	Default value is 00

Table 34: Part identification code

9.3 Ordering information

Ordering No.	Product
SARA-U260-00S	UMTS/HSPA 850/1900 MHz and GSM/EGPRS 850/1900 MHz bands for America, 26.0 x 16.0 x 3.0 mm, 250 pcs/reel
SARA-U270-00S	UMTS/HSPA 900/2100 MHz and GSM/EGPRS 900/1800 MHz bands for Europe, Asia and other countries, 26.0 x 16.0 x 3.0 mm, 250 pcs/reel
SARA-U280-00S	UMTS/HSPA 850/1900 MHz bands for America, 26.0 x 16.0 x 3.0 mm, 250 pcs/reel
SARA-U290-00S	UMTS/HSPA 900/2100 MHz bands for Europe, Asia and other countries, 26.0 x 16.0 x 3.0 mm, 250 pcs/reel
SARA-U290-60S	UMTS/HSPA 900/2100 MHz bands, FW version approved and locked for SoftBank Japanese network operator, 26.0 x 16.0 x 3.0 mm, 250 pcs/reel

Table 35: Product ordering codes

Appendix

A Glossary

Name	Definition
ADC	Analog to Digital Converter
BER	Bit Error Rate
DDC	Display Data Channel (I^2C compatible) Interface
DL	Down-link (Reception)
Driver Class	Output Driver Class: see Table 20 for definition
DRX	Discontinuous Reception
EDGE	Enhanced Data rates for GSM Evolution
ERS	External Reset Input Signal
GDI	Generic Digital Interfaces (V_INT supply power domain)
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications
H	High logic digital level
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I^2C	Inter-Integrated Circuit Interface
I^2S	Inter-IC Sound Interface
L	Low logic digital level
LGA	Land Grid Array
N/A	Not Applicable
PCN / IN	Product Change Notification / Information Note
PD	Pull-Down
POS	Power-On Input Signal (power domain)
PU	Pull-Up
PU/PD Class	Pull-Up / Pull-Down Class: see Table 20 for definition
RMC	Reference Measurement Channel
SIM	SIM Interface (power domain)
SPI	Serial Peripheral Interface
T	Tristate (Output of the pin set to tri-state, i.e. high impedance state)
T/PD	Tristate with internal active Pull-Down enabled
T/PU	Tristate with internal active Pull-Up enabled
TBD	To Be Defined
UART	Universal Asynchronous Receiver-Transmitter serial interface
UL	Up-link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus (power domain)

Table 36: Explanation of abbreviations and terms used

Related documents

[1] 3GPP TS 27.007 - AT command set for User Equipment (UE)

[2] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

[3] 3GPP TS 27.010 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol

[4] u-blox AT Commands Manual, Docu No UBX-13002752

[5] u-blox SARA-G3 and SARA-U2 series System Integration Manual, Docu No UBX-13000995

[6] u-blox GNSS Implementation Application Note, Docu No UBX-13001849

[7] 3GPP TS 26.267 eCall Data Transfer; In-band modem solution; General description

[8] ITU-T Recommendation V24, 02-2000. List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Connection Equipment (DCE)

[9] u-blox Mux Implementation Application Note for wireless modules, Docu No UBX-13001887

[10] I^2C-bus specification and user manual - Rev. 5 - 9 October 2012 - NXP Semiconductors, http://www.nxp.com/documents/user_manual/UM10204.pdf

[11] Universal Serial Bus Revision 2.0 specification, http://www.usb.org/developers/docs/usb20_docs/

[12] u-blox Package Information Guide, Docu No UBX-14001652

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Revision history

Revision	Date	Name	Status / Comments
R01	22-Jan-2014	sfal / sses	Initial release
R02	29-Apr-2014	sses	Updated: receiver sensitivity performance, normal operating temperature range, maximum ESD ratings, USB audio device class support, GPIO configuration table.
R03	20-Jun-2014	sses	Advance Information document status. Added VCC current consumption characteristics.
R04	18-Jul-2014	sses	Early Production Information document status. Added VCC current consumption characteristics for 3G Tx/Rx connected modes.

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