# MCP3901

## Two-Channel Analog Front End

### Features

- Two Synchronous Sampling 16/24-bit Resolution Delta-Sigma A/D Converters with Proprietary Multi-Bit Architecture
- 91 dB SINAD, -104 dBc Total Harmonic Distortion (THD) (up to 35$^{th}$ harmonic), 109 dB Spurious-free Dynamic Range (SFDR) for Each Channel
- Programmable Data Rate up to 64 ksps
- Ultra Low-Power Shutdown mode with <2 µA
- -133 dB Crosstalk Between the Two Channels
- Low Drift Internal Voltage Reference: 12 ppm/°C
- Differential Voltage Reference Input Pins
- High Gain PGA on Each Channel (up to 32 V/V)
- Phase Delay Compensation Between the Two Channels with 1 µs time Resolution
- Separate Modulator Outputs for Each Channel
- High-Speed, Addressable 20 MHz SPI Interface with Mode 0,0 and 1,1 Compatibility
- Independent Analog and Digital Power Supplies: 4.5V-5.5V $AV_{DD}$, 2.7V-5.5V $DV_{DD}$
- Low-Power Consumption: (14 mW typical at 5V)
- Available in Small 20-lead SSOP and QFN Packages
- Industrial Temperature Ranges:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

### Applications

- Energy Metering and Power Measurement
- Automotive
- Portable Instrumentation
- Medical and Power Monitoring

### Description

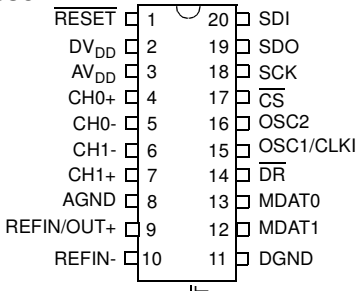
The MCP3901 is a dual channel Analog Front End (AFE) containing two synchronous sampling Delta-Sigma Analog-to-Digital Converters (ADC), two PGAs, phase delay compensation block internal voltage reference, modulator output block, and high-speed 20 MHz SPI compatible serial interface. The converters contain a proprietary dithering algorithm for reduced Idle tones and improved THD.

The internal register map contains 24-bit wide ADC data words, a modulator output byte, as well as six writable control registers to program gain, oversampling ratio, phase, resolution, dithering, shutdown, Reset and several communication features. The communication is largely simplified with various Continuous Read modes that can be accessed by the Direct Memory Access (DMA) of an MCU and with a separate data ready pin that can be connected directly to an Interrupt Request (IRQ) input of an MCU.

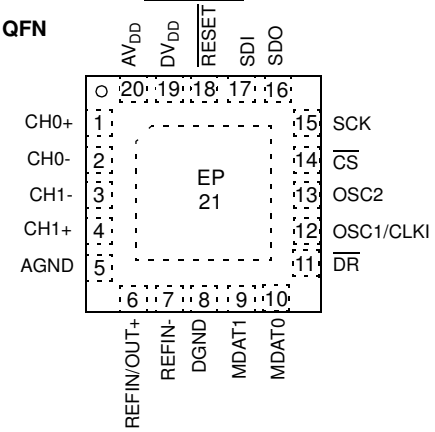
The MCP3901 is capable of interfacing to a large variety of voltage and current sensors, including shunts, current transformers, Rogowski coils and Hall-effect sensors.

### Package Type

**20-Lead SSOP**

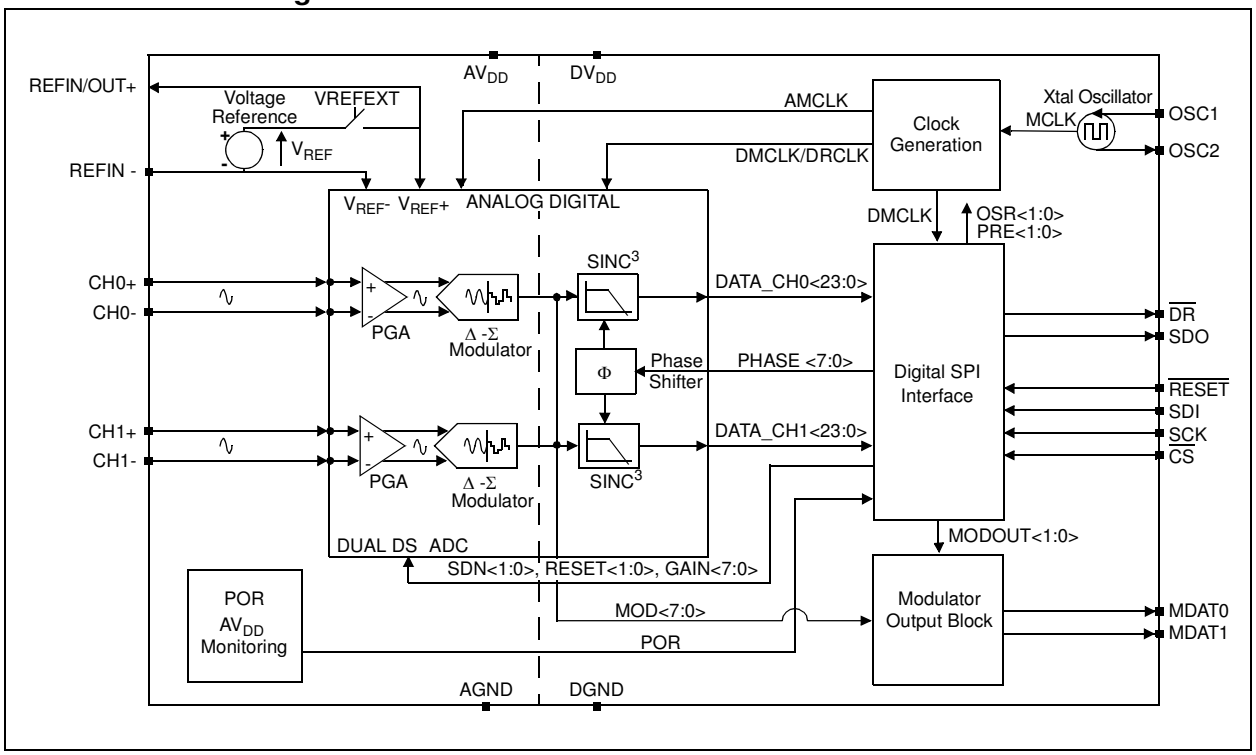



**20-Lead QFN**




* Includes Exposed Thermal Pad (EP); see Table 3-1.

## Functional Block Diagram



# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

$V_{DD}$ .....7.0V
Digital inputs and outputs w.r.t. $A_{GND}$..... -0.6V to $V_{DD}$ +0.6V
Analog input w.r.t. $A_{GND}$ .....-6V to +6V
$V_{REF}$ input w.r.t. $A_{GND}$ ..... -0.6V to $V_{DD}$ +0.6V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) .....7.0 kV, 400V
ESD on all other pins (HBM,MM) .....7.0 kV, 400V

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, $AV_{DD}$ = 4.5 to 5.5V, $DV_{DD}$ = 2.7 to 5.5V; -40°C < $T_A$ < +85°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; $V_{IN}$ = -0.5 dBFS = 333 $mV_{RMS}$ @ 50/60 Hz

| Parameters | Symbol | Min | Typical | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Internal Voltage Reference** | | | | | | |
| Internal Voltage Reference Tolerance | $V_{REF}$ | -2% | 2.37 | +2% | V | VREFEXT = 0 |
| Temperature Coefficient | $TC_{REF}$ | — | 12 | — | ppm/°C | VREFEXT = 0 |
| Output Impedance | $ZOUT_{REF}$ | — | 7 | — | kΩ | $AV_{DD}$ = 5V, VREFEXT = 0 |
| **Voltage Reference Input** | | | | | | |
| Input Capacitance | | — | — | 10 | pF | |
| Differential Input Voltage Range ($V_{REF+} - V_{REF-}$) | $V_{REF}$ | 2.2 | — | 2.6 | V | $V_{REF} = (V_{REF+} - V_{REF-})$, VREFEXT = 1 |
| Absolute Voltage on REFIN+ Pin | $V_{REF+}$ | 1.9 | — | 2.9 | V | VREFEXT = 1 |
| Absolute Voltage on REFIN- Pin | $V_{REF-}$ | -0.3 | — | 0.3 | V | |
| **ADC Performance** | | | | | | |
| Resolution (No Missing Codes) | | 24 | — | — | bits | OSR = 256 (See Table 5-3) |
| Sampling Frequency | $f_S$ | See Table 4-2 | | | kHz | $f_S$ = DMCLK = MCLK/ (4 x PRESCALE) |

**Note 1:** This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance is specified at -0.5 dB below the maximum signal range, $V_{IN}$ = -0.5 dBFS @ 50/60 Hz = 353 $mV_{RMS}$, $V_{REF}$ = 2.4V.

**2:** See terminology section for definition.

**3:** This parameter is established by characterization and not 100% tested.

**4:** For these operating currents, the following bit settings apply: SHUTDOWN<1:0> = 00, RESET<1:0> = 00, VREFEXT = 0, CLKEXT = 0.

**5:** For these operating currents, the following Configuration bit settings apply: SHUTDOWN<1:0> = 11, VREFEXT = 1, CLKEXT = 1.

**6:** Applies to all gains. Offset error is dependant on PGA gain setting (see Figure 2-19 for typical values).

**7:** Outside of this range, the ADC accuracy is not specified. An extended input range of ±6V can be applied continuously to the part with no risk for damage.

**8:** For proper operation and to keep ADC accuracy, AMCLK should always be in the range of 1 to 5 MHz with BOOST bits off. With BOOST bits on, AMCLK should be in the range of 1 to 8.192 MHz, AMCLK = MCLK/PRESCALE. When using a crystal, the CLKEXT bit should be equal to '0'.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, $AV_{DD}$ = 4.5 to 5.5V, $DV_{DD}$ = 2.7 to 5.5V; -40°C < $T_A$ < +85°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; $V_{IN}$ = -0.5 dBFS = 333 $mV_{RMS}$ @ 50/60 Hz

| Parameters | Symbol | Min | Typical | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Output Data Rate | $f_D$ | See Table 4-2 | | | ksps | $f_D$ = DRCLK = DMCLK/ OSR = MCLK/ (4 x PRESCALE x OSR) |
| Analog Input Absolute Voltage on CH0+, CH0-, CH1+, CH1- Pins | CHn+ | -1 | — | +1 | V | All analog input channels, measured to AGND **(Note 7)** |
| Analog Input Leakage Current | $A_{IN}$ | — | 1 | — | nA | **(Note 4)** |
| | | — | 2 | — | nA | -40°C < $T_A$ < 125°C |
| Differential Input Voltage Range | (CHn+ – CHn-) | — | — | 500/GAIN | mV | **(Note 1)** |
| Offset Error **(Note 2)** | $V_{OS}$ | -3 | — | +3 | mV | **(Note 6)** |
| Offset Error Drift | | — | 3 | — | µV/°C | From -40°C to +125°C |
| Gain Error **(Note 2)** | GE | — | -0.4 | — | % | G = 1 |
| | | -2.5 | — | +2.5 | % | All Gains |
| Gain Error Drift | | — | 1 | — | ppm/°C | From -40°C to +125°C |
| Integral Nonlinearity **(Note 2)** | INL | — | 15 | — | ppm | GAIN = 1, DITHER = On |
| Input Impedance | $Z_{IN}$ | 350 | — | — | kΩ | Proportional to 1/AMCLK |
| Signal-to-Noise and Distortion Ratio **(Notes 2, 3)** | SINAD | 89 | 91 | — | dB | OSR = 256, DITHER = On |
| | | 78 | 79 | — | dB | |
| Total Harmonic Distortion **(Notes 2, 3)** | THD | — | -104 | -102 | dB | OSR = 256, DITHER = On |
| | | — | -85 | -84 | dB | |
| Signal-to-Noise Ratio **(Notes 2, 3)** | SNR | 89 | 91 | — | dB | OSR = 256, DITHER = On |
| | | 80 | 81 | — | dB | |
| Spurious Free Dynamic Range **(Note 2)** | SFDR | — | 109 | — | dB | OSR = 256, DITHER = On |
| | | — | 87 | — | dB | |
| Crosstalk (50/60 Hz) **(Note 2)** | CTALK | — | -133 | — | dB | OSR = 256, DITHER = On |

**Note 1:** This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance is specified at -0.5 dB below the maximum signal range, $V_{IN}$ = -0.5 dBFS @ 50/60 Hz = 353 $mV_{RMS}$, $V_{REF}$ = 2.4V.

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## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, $AV_{DD}$ = 4.5 to 5.5V, $DV_{DD}$ = 2.7 to 5.5V; -40°C < $T_A$ < +85°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; $V_{IN}$ = -0.5 dBFS = 333 $mV_{RMS}$ @ 50/60 Hz

| Parameters | Symbol | Min | Typical | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| AC Power Supply Rejection | AC PSRR | — | -77 | — | dB | $AV_{DD}$ and $DV_{DD}$ = 5V + 1 $V_{PP}$ @ 50/60 Hz |
| DC Power Supply Rejection | DC PSRR | — | -77 | — | dB | $AV_{DD}$ and $DV_{DD}$ = 4.5 to 5.5V |
| DC Common-Mode Rejection Ratio (**Note 2**) | CMRR | — | -72 | — | dB | $V_{CM}$ varies from -1V to +1V |
| **Oscillator Input** | | | | | | |
| Master Clock Frequency Range | MCLK | 1 | — | 16.384 | MHz | (**Note 8**) |
| **Power Specifications** | | | | | | |
| Operating Voltage, Analog | $AV_{DD}$ | 4.5 | — | 5.5 | V | |
| Operating Voltage, Digital | $DV_{DD}$ | 2.7 | 3.6 | 5.5 | V | |
| Power On Reset Threshold | POR | — | 4.2 | — | V | (**Note 3**) |
| | | — | 4.6 | — | | -40°C < $T_A$ < 125°C, (**Note 3**) |
| Operating Current, Analog (**Note 4**) | $AI_{DD}$ | — | 2.1 | 2.8 | mA | BOOST<1:0> = 00 |
| | | — | 2.1 | 3.3 | mA | -40°C < $T_A$ < 125°C, BOOST<1:0> = 00 |
| | | — | 3.8 | 5.6 | mA | BOOST<1:0> = 11 |
| | | — | 3.8 | 7 | mA | -40°C < $T_A$ < 125°C, BOOST<1:0> = 11 |
| Operating Current, Digital | $DI_{DD}$ | — | 0.45 | 1.0 | mA | $DV_{DD}$ = 5V, MCLK = 4 MHz |
| | | — | 0.25 | 0.45 | mA | $DV_{DD}$ = 2.7V, MCLK = 4 MHz |
| | | — | 1.2 | 1.6 | mA | $DV_{DD}$ = 5V, MCLK = 8.192 MHz |
| Shutdown Current, Analog | $I_{DDS,A}$ | — | — | 1 | µA | $AV_{DD}$ pin only (**Note 5**) |
| Shutdown Current, Digital | $I_{DDS,D}$ | — | — | 1 | µA | $DV_{DD}$ pin only (**Note 5**) |

**Note 1:** This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance is specified at -0.5 dB below the maximum signal range, $V_{IN}$ = -0.5 dBFS @ 50/60 Hz = 353 $mV_{RMS}$, $V_{REF}$ = 2.4V.

**2:** See terminology section for definition.

**3:** This parameter is established by characterization and not 100% tested.

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**5:** For these operating currents, the following Configuration bit settings apply: SHUTDOWN<1:0> = 11, VREFEXT = 1, CLKEXT = 1.

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**8:** For proper operation and to keep ADC accuracy, AMCLK should always be in the range of 1 to 5 MHz with BOOST bits off. With BOOST bits on, AMCLK should be in the range of 1 to 8.192 MHz, AMCLK = MCLK/PRESCALE. When using a crystal, the CLKEXT bit should be equal to '0'.

## SERIAL INTERFACE SPECIFICATIONS

**Electrical Specifications:** Unless otherwise indicated, all parameters apply: $AV_{DD}$ = 4.5 to 5.5V, $DV_{DD}$ = 2.7 to 5.5V, -40°C < $T_A$ < +85°C, $C_{LOAD}$ = 30 pF

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Serial Clock Frequency | $f_{SCK}$ | —<br>— | —<br>— | 20<br>10 | MHz<br>MHz | $4.5 \le DV_{DD} \le 5.5$<br>$2.7 \le DV_{DD} < 5.5$ |
| $\overline{CS}$ Setup Time | $t_{CSS}$ | 25<br>50 | —<br>— | —<br>— | ns<br>ns | $4.5 \le DV_{DD} \le 5.5$<br>$2.7 \le DV_{DD} \le 5.5$ |
| $\overline{CS}$ Hold Time | $t_{CSH}$ | 50<br>100 | —<br>— | —<br>— | ns<br>ns | $4.5 \le DV_{DD} \le 5.5$<br>$2.7 \le DV_{DD} < 5.5$ |
| $\overline{CS}$ Disable Time | $t_{CSD}$ | 50 | — | — | ns | |
| Data Setup Time | $t_{SU}$ | 5<br>10 | —<br>— | —<br>— | ns<br>ns | $4.5 \le DV_{DD} \le 5.5$<br>$2.7 \le DV_{DD} < 5.5$ |
| Data Hold Time | $t_{HD}$ | 10<br>20 | —<br>— | —<br>— | ns<br>ns | $4.5 \le DV_{DD} \le 5.5$<br>$2.7 \le DV_{DD} < 5.5$ |
| Serial Clock High Time | $t_{HI}$ | 20<br>50 | —<br>— | —<br>— | ns<br>ns | $4.5 \le DV_{DD} \le 5.5$<br>$2.7 \le DV_{DD} < 5.5$ |
| Serial Clock Low Time | $t_{LO}$ | 20<br>50 | —<br>— | —<br>— | ns<br>ns | $4.5 \le DV_{DD} \le 5.5$<br>$2.7 \le DV_{DD} < 5.5$ |
| Serial Clock Delay Time | $t_{CLD}$ | 50 | — | — | ns | |
| Serial Clock Enable Time | $t_{CLE}$ | 50 | — | — | ns | |
| Output Valid from SCK Low | $t_{DO}$ | — | — | 50 | ns | $2.7 \le DV_{DD} < 5.5$ |
| Modulator Output Valid from AMCLK High | $t_{DOMDAT}$ | — | — | 1/2 * AMCLK | s | |
| Output Hold Time | $t_{HO}$ | 0 | — | — | ns | **(Note 1)** |
| Output Disable Time | $t_{DIS}$ | —<br>— | —<br>— | 25<br>50 | ns<br>ns | $4.5 \le DV_{DD} \le 5.5$<br>$2.7 \le DV_{DD} < 5.5$ **(Note 1)** |
| Reset Pulse Width ($\overline{RESET}$) | $t_{MCLR}$ | 100 | — | — | ns | $2.7 \le DV_{DD} < 5.5$ |
| Data Transfer Time to $\overline{DR}$ (data ready) | $t_{DODR}$ | — | — | 50 | ns | $2.7 \le DV_{DD} < 5.5$ |
| Data Ready Pulse Low Time | $t_{DRP}$ | — | 1/DMCLK | — | µs | $2.7 \le DV_{DD} < 5.5$ |
| Schmitt Trigger High-Level Input Voltage | $V_{IH1}$ | .7 $DV_{DD}$ | — | $DV_{DD}$ + 1 | V | |
| Schmitt Trigger Low-Level Input Voltage | $V_{IL1}$ | -0.3 | — | 0.2 $DV_{DD}$ | V | |
| Hysteresis of Schmitt Trigger Inputs (all digital inputs) | $V_{HYS}$ | 300 | — | — | mV | |
| Low-Level Output Voltage, SDO Pin | $V_{OL}$ | — | — | 0.4 | V | SDO pin only,<br>$I_{OL}$ = +2.0 mA, $V_{DD}$ = 5.0V |
| Low-level output voltage, $\overline{DR}$ and MDAT Pins | $V_{OL}$ | — | — | 0.4 | V | $\overline{DR}$ and MDAT pins only,<br>$I_{OL}$ = +800 mA, $V_{DD}$ = 5.0V |
| High-level output voltage, SDO pin | $V_{OH}$ | $DV_{DD}$ – 0.5 | — | — | V | SDO pin only,<br>$I_{OH}$ = -2.0 mA, $V_{DD}$ = 5.0V |
| High-level output voltage, $\overline{DR}$ and MDAT pins | $V_{OH}$ | $DV_{DD}$ – 0.5 | — | — | V | $\overline{DR}$ and MDAT pins only,<br>$I_{OH}$ = -800 µA, $V_{DD}$ = 5.0V |
| Input leakage current | $I_{LI}$ | — | — | ±1 | µA | $\overline{CS}$ = $DV_{DD}$,<br>$V_{IN}$ = DGND or $DV_{DD}$ |
| Output leakage current | $I_{LO}$ | — | — | ±1 | µA | $\overline{CS}$ = $DV_{DD}$,<br>$V_{OUT}$ = DGND or $DV_{DD}$ |
| Internal capacitance (all inputs and outputs) | $C_{INT}$ | — | — | 7 | pF | $T_A$ = 25°C,<br>SCK = 1.0 MHz,<br>$DV_{DD}$ = 5.0V **(Note 1)** |

**Note 1:** This parameter is periodically sampled and not 100% tested.

## TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD}$ = 4.5 to 5.5V, $DV_{DD}$ = 2.7 to 5.5V

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | (Note 1) |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 20L SSOP | $\theta_{JA}$ | — | 89.3 | — | °C/W | |
| Thermal Resistance, 20L QFN | $\theta_{JA}$ | — | 43 | — | °C/W | |

**Note 1:** The internal junction temperature ($T_J$) must not exceed the absolute maximum specification of +150°C.

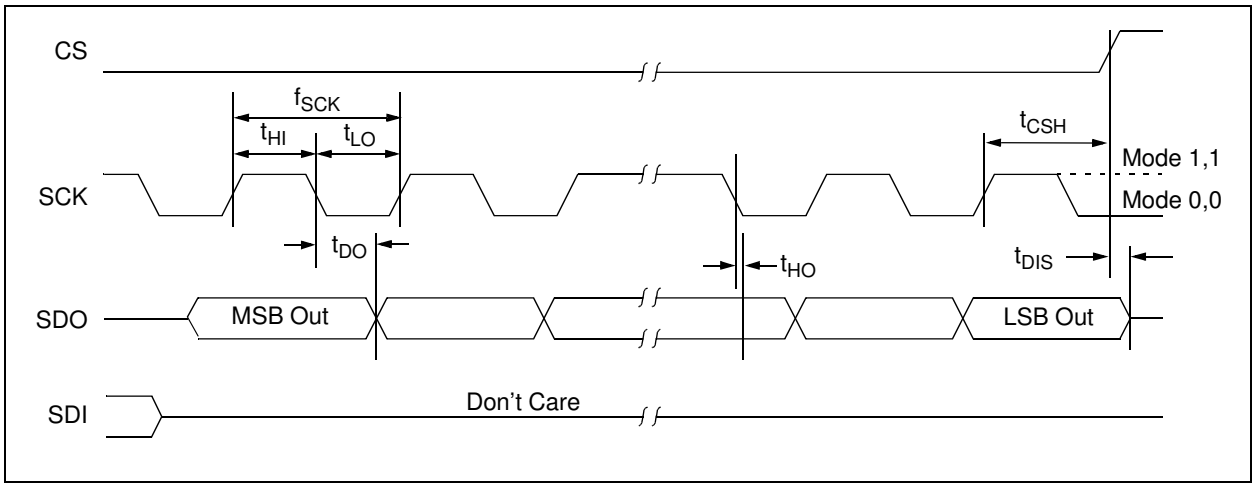



***FIGURE 1-1:*** *Serial Output Timing Diagram.*

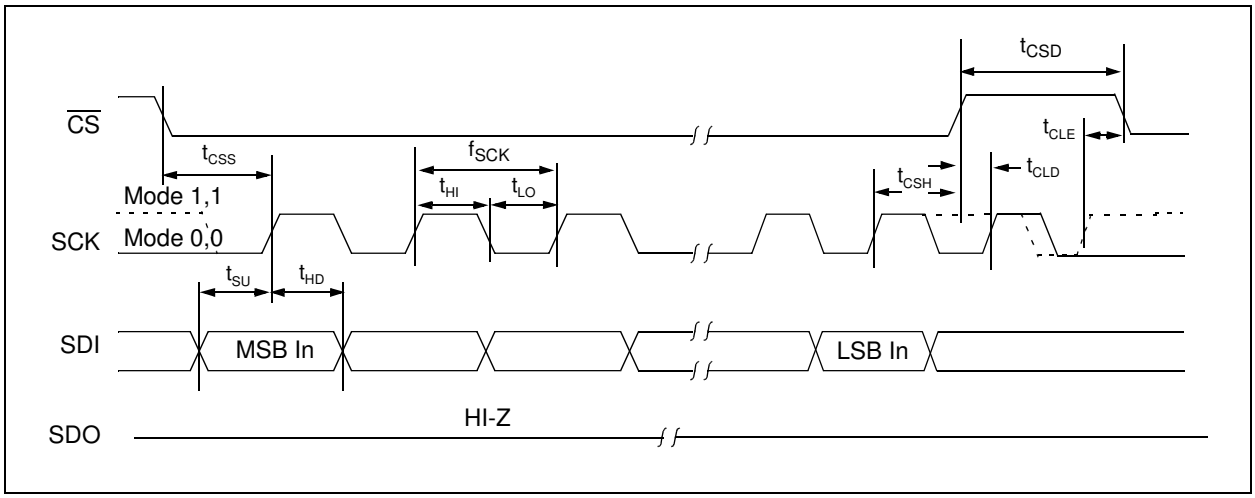



***FIGURE 1-2:*** *Serial Input Timing Diagram.*

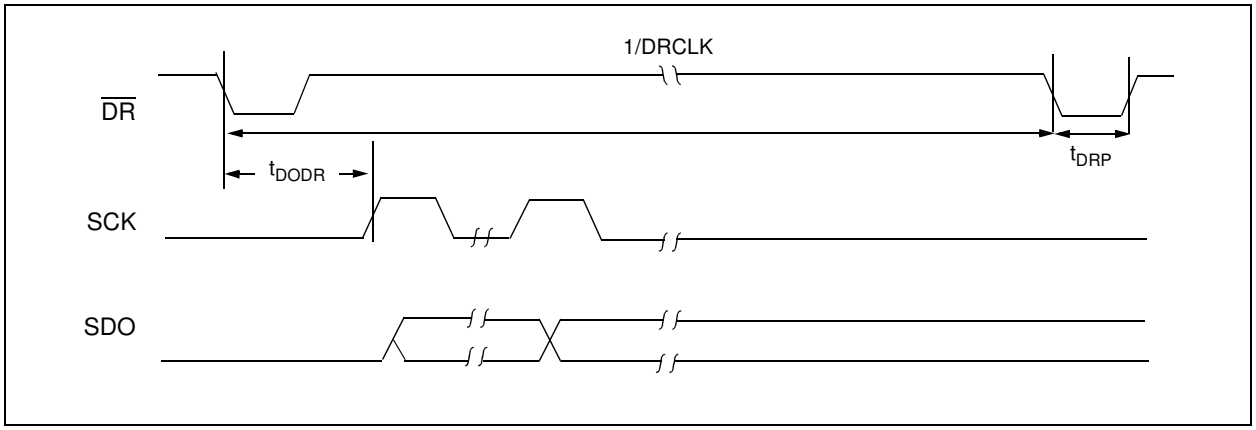



***FIGURE 1-3:*** *Data Ready Pulse Timing Diagram.*

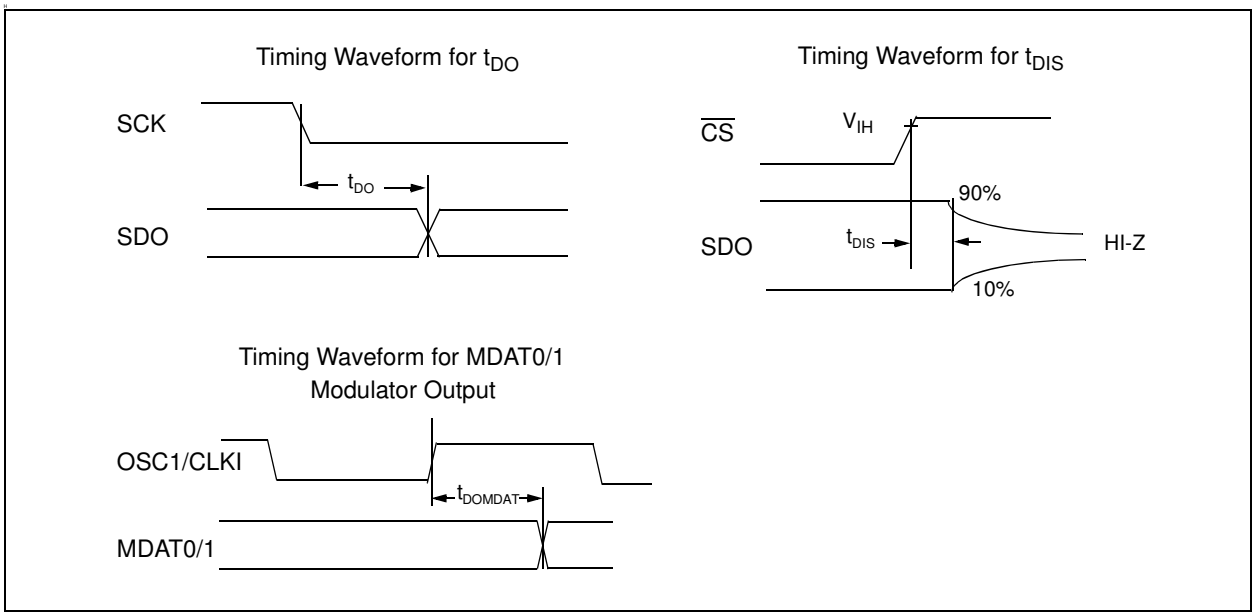



***FIGURE 1-4:*** *Specific Timing Diagrams.*

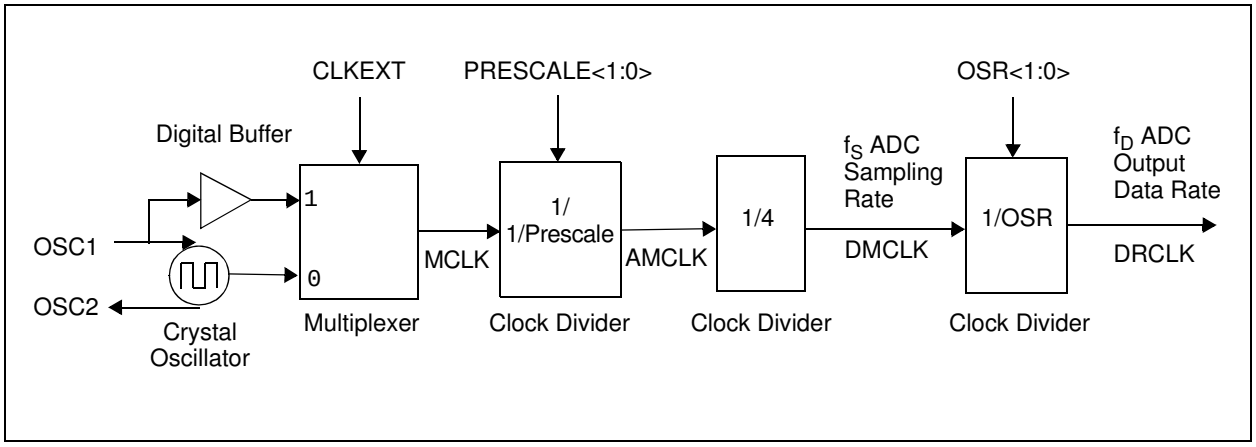



***FIGURE 1-5:*** *MCP3901 Clock Detail.*

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**Note:** Unless otherwise indicated, $AV_{DD}$ = 5.0V, $DV_{DD}$ = 5.0V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; $V_{IN}$ = -0.5 dBFS @ 60 Hz.

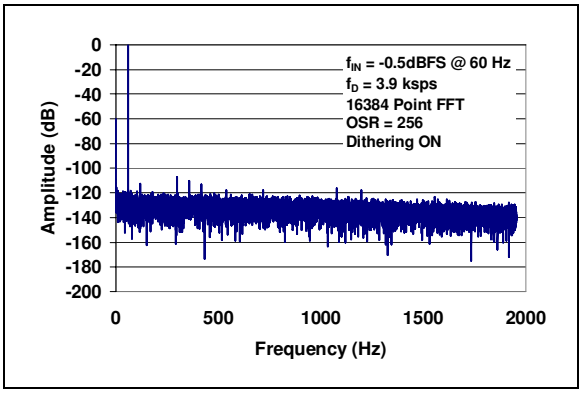



***FIGURE 2-1:*** *Spectral Response.*

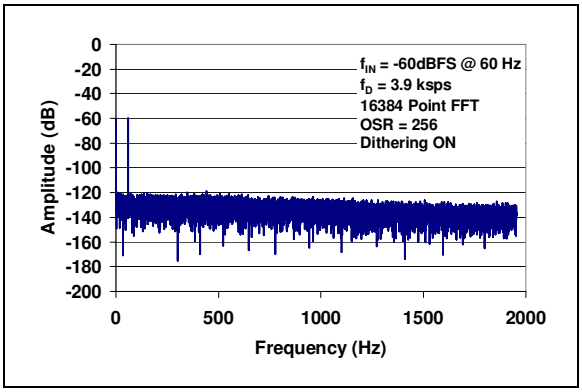



***FIGURE 2-2:*** *Spectral Response.*

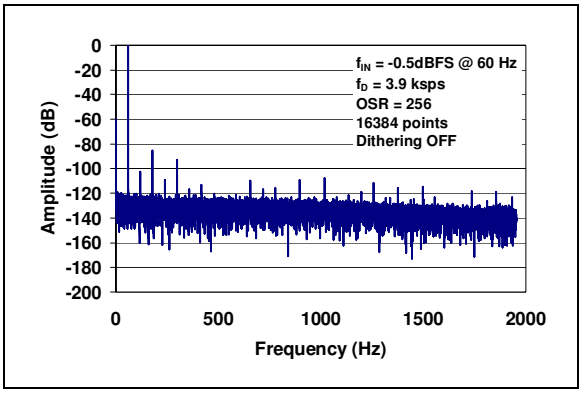



***FIGURE 2-3:*** *Spectral Response.*

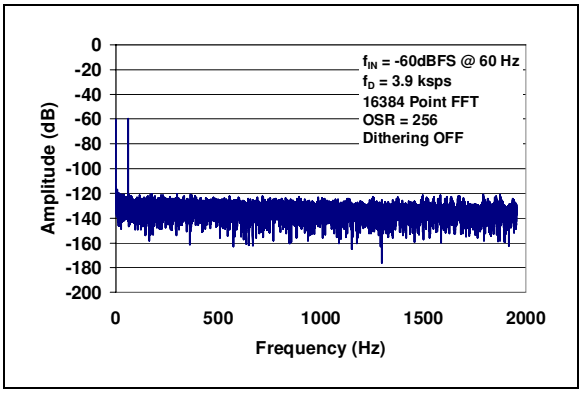



***FIGURE 2-4:*** *Spectral Response.*

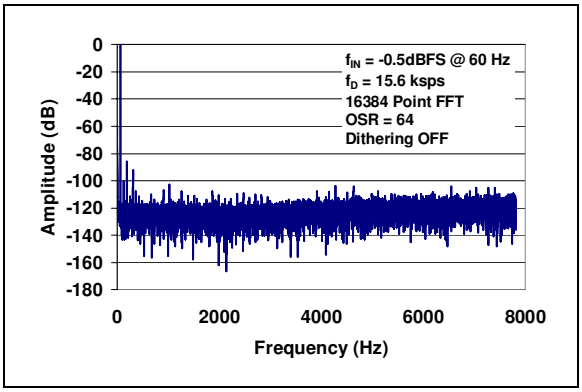



***FIGURE 2-5:*** *Spectral Response.*

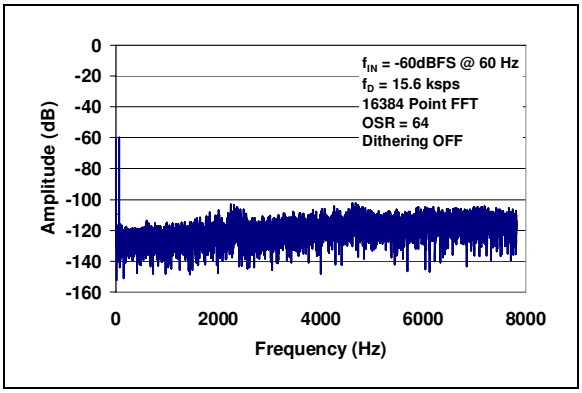



***FIGURE 2-6:*** *Spectral Response.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 5.0V, $DV_{DD}$ = 5.0V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; $V_{IN}$ = -0.5 dBFS @ 60 Hz.

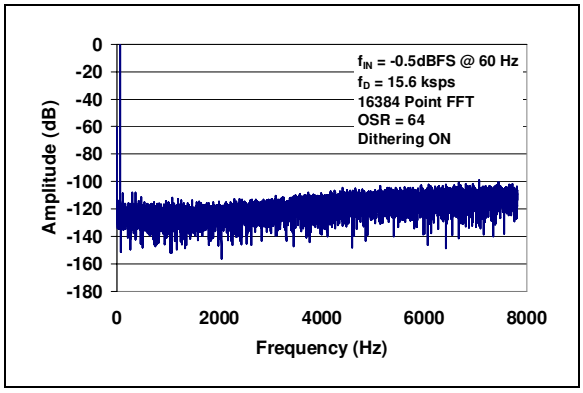



***FIGURE 2-7:*** *Spectral Response.*

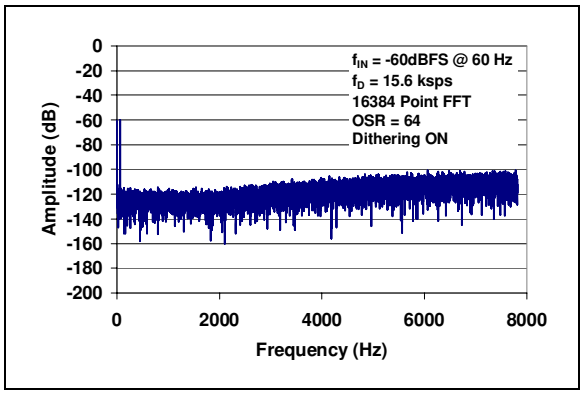



***FIGURE 2-8:*** *Spectral Response.*

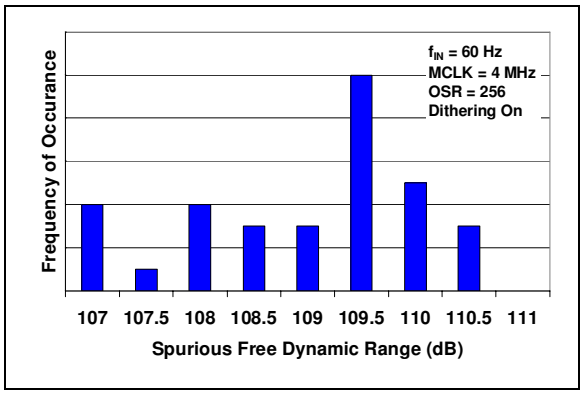



***FIGURE 2-9:*** *Spurious Free Dynamic Range Histogram.*

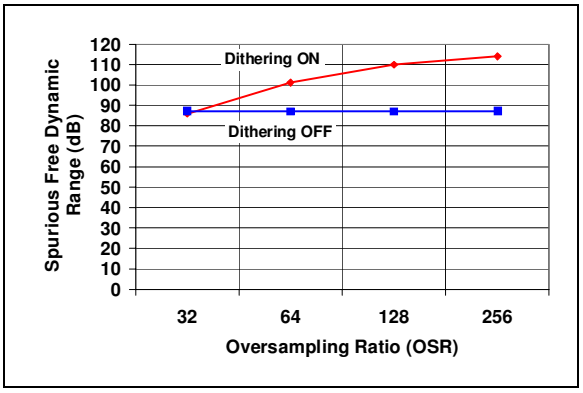



***FIGURE 2-10:*** *Spurious Free Dynamic Range vs. Oversampling Ratio.*

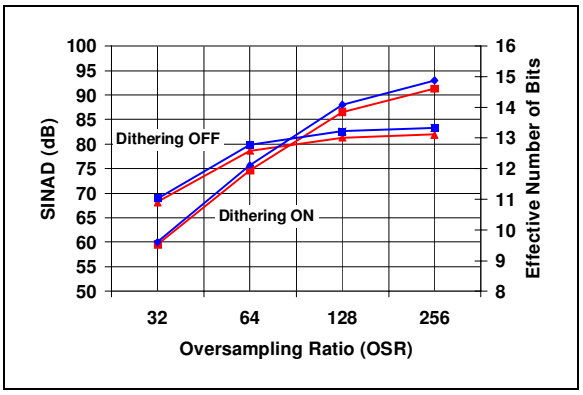



***FIGURE 2-11:*** *Signal-to-Noise and Distortion and Effective Number of Bits vs. Oversampling Ratio.*

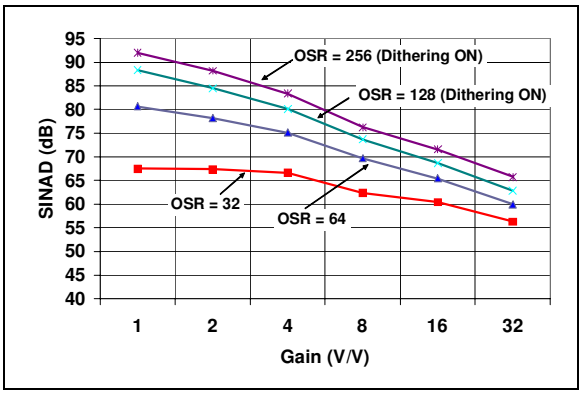



***FIGURE 2-12:*** *Signal-to-Noise and Distortion vs. Gain.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 5.0V, $DV_{DD}$ = 5.0V; $T_A$ = +25 °C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; $V_{IN}$ = -0.5 dBFS @ 60 Hz.

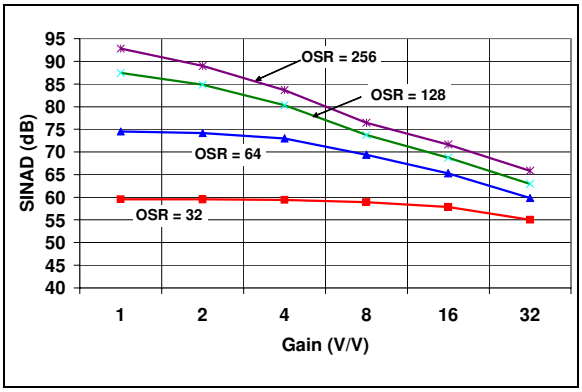



***FIGURE 2-13:*** *Signal-to-Noise and Distortion vs. Gain (Dithering On).*

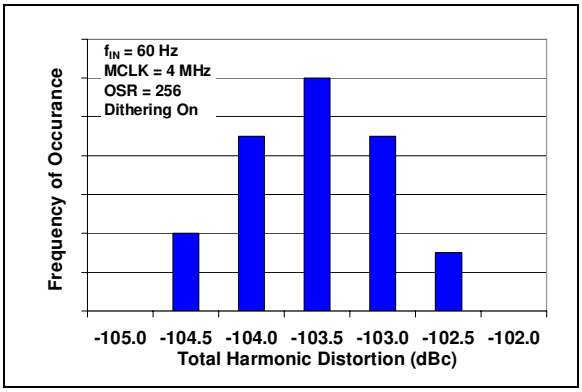



***FIGURE 2-16:*** *Total Harmonic Distortion Histogram (Dithering On).*

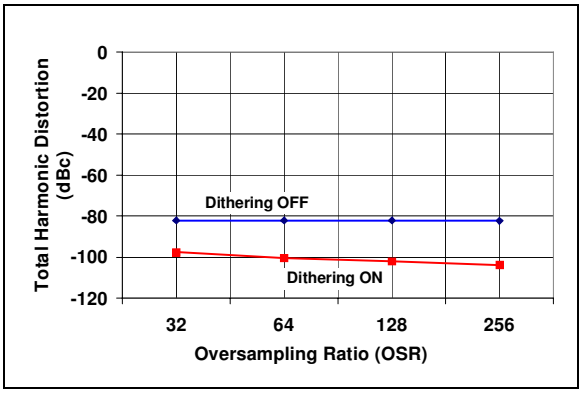



***FIGURE 2-14:*** *Total Harmonic Distortion vs. Oversampling Ratio.*

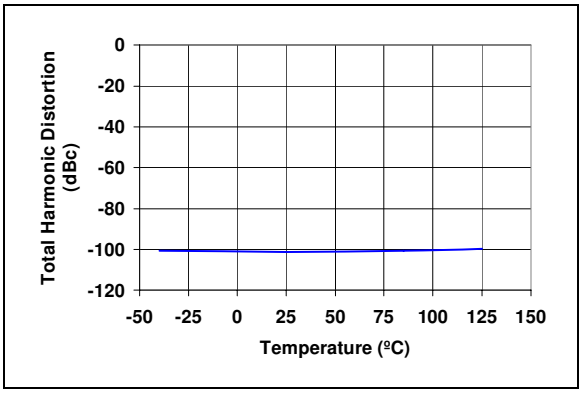



***FIGURE 2-17:*** *Total Harmonic Distortion vs. Temperature.*

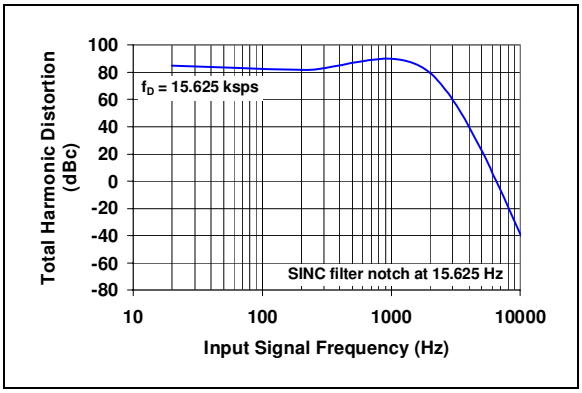



***FIGURE 2-15:*** *Total Harmonic Distortion vs. Input Signal Frequency.*

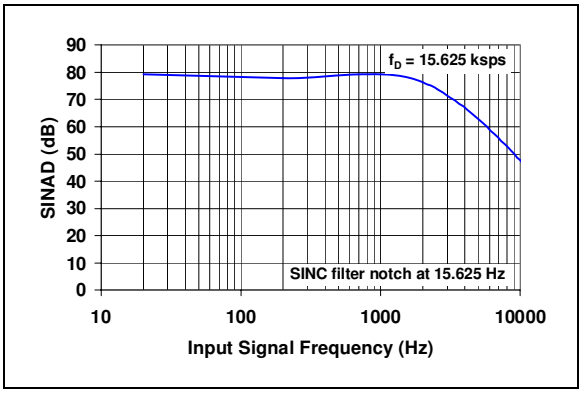



***FIGURE 2-18:*** *Signal-to-Noise and Distortion vs. Input Frequency.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 5.0V, $DV_{DD}$ = 5.0V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; $V_{IN}$ = -0.5 dBFS @ 60 Hz.

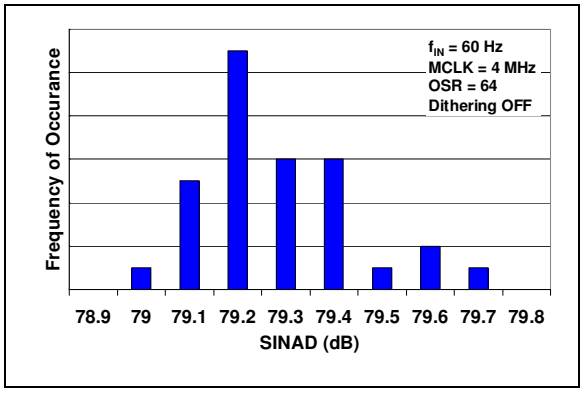



***FIGURE 2-19:*** *Signal-to-Noise and Distortion Histogram.*

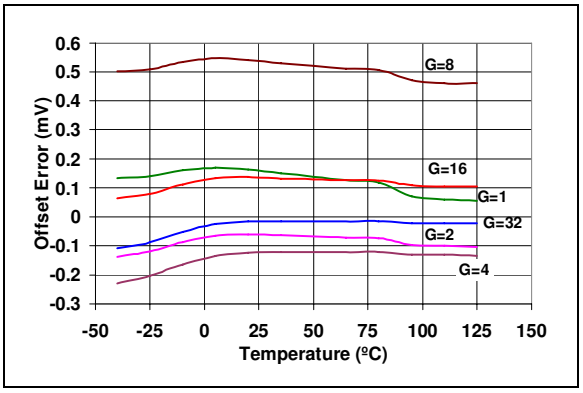



***FIGURE 2-22:*** *Channel 0 Offset vs. Temperature.*

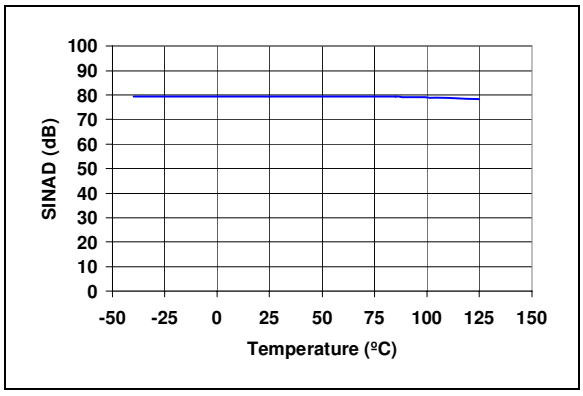



***FIGURE 2-20:*** *Signal-to-Noise and Distortion vs. Temperature.*

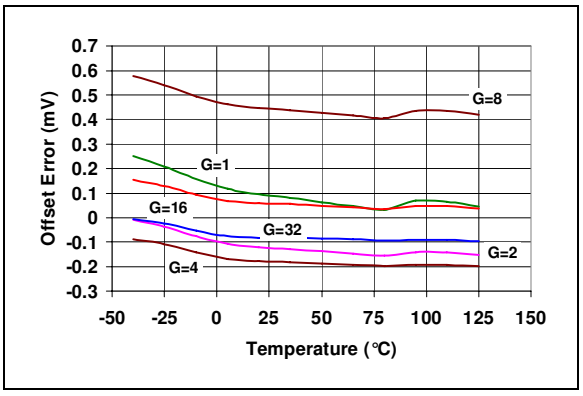



***FIGURE 2-23:*** *Channel 1 Offset vs. Temperature.*

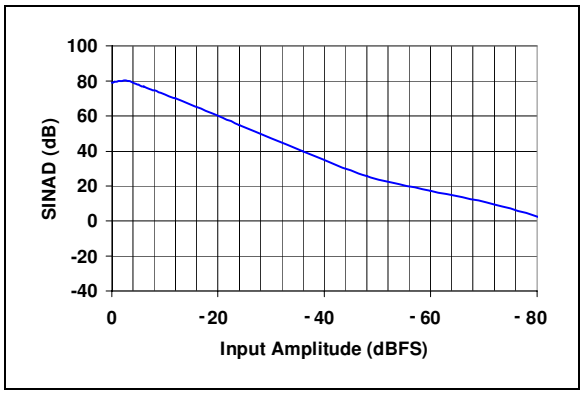



***FIGURE 2-21:*** *Signal-to-Noise and Distortion vs. Input Signal Amplitude.*

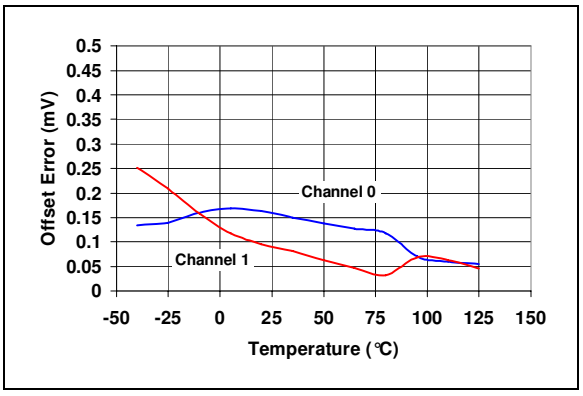



***FIGURE 2-24:*** *Channel-to-Channel Offset Match vs. Temperature.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 5.0V, $DV_{DD}$ = 5.0V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; $V_{IN}$ = -0.5 dBFS @ 60 Hz.

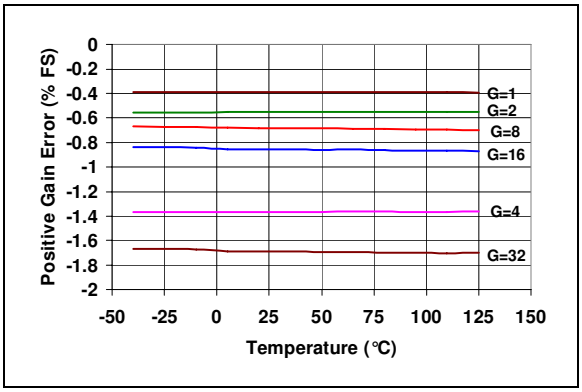



***FIGURE 2-25:*** *Positive Gain Error vs. Temperature.*

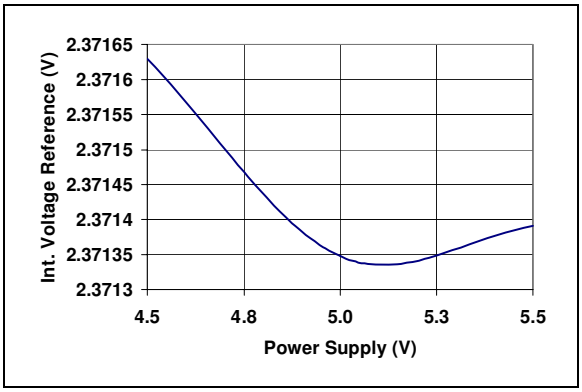



***FIGURE 2-28:*** *Internal Voltage Reference vs. Supply Voltage.*

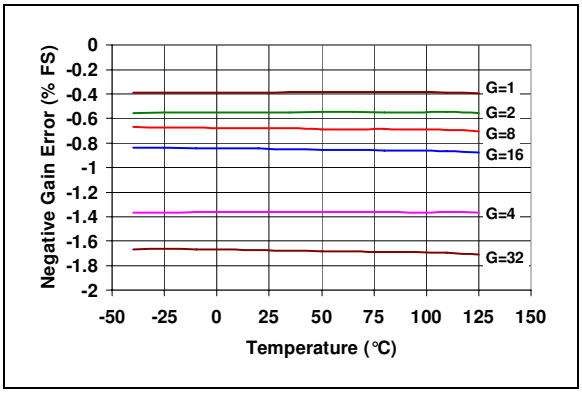



***FIGURE 2-26:*** *Negative Gain Error vs. Temperature*

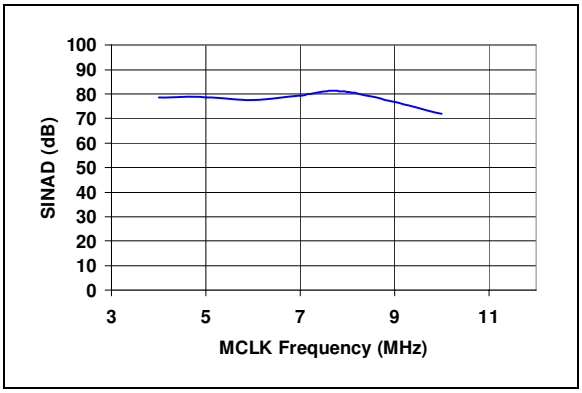



***FIGURE 2-29:*** *Signal-to-Noise and Distortion vs. Master Clock (MCLK), BOOST ON.*

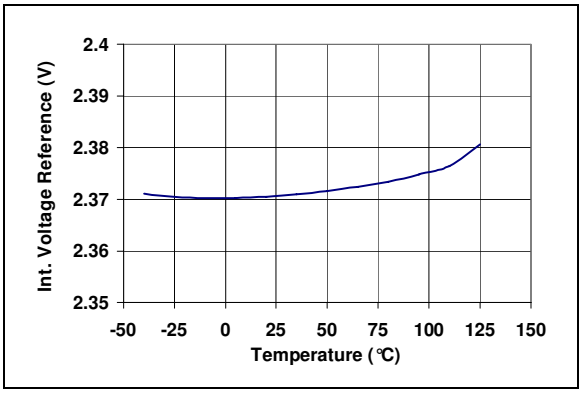



***FIGURE 2-27:*** *Internal Voltage Reference vs. Temperature.*

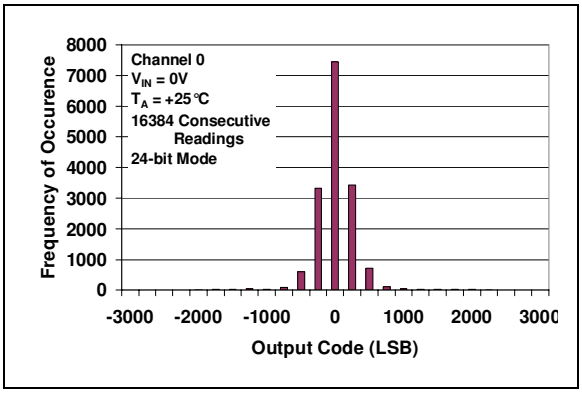



***FIGURE 2-30:*** *Noise Histogram.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 5.0V, $DV_{DD}$ = 5.0 V; $T_A$ = 25 °C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; $V_{IN}$ = -0.5 dBFS @ 60 Hz.

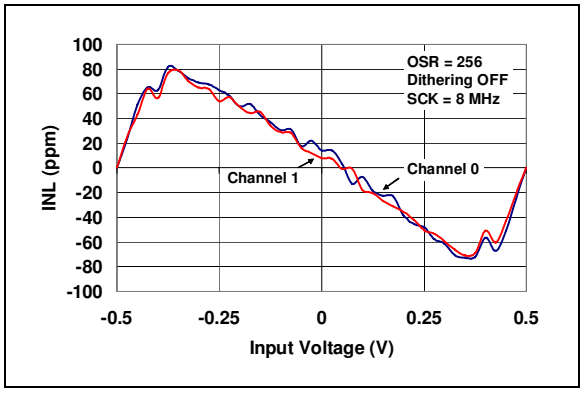



***FIGURE 2-31:*** *Integral Nonlinearity (Dithering Off).*

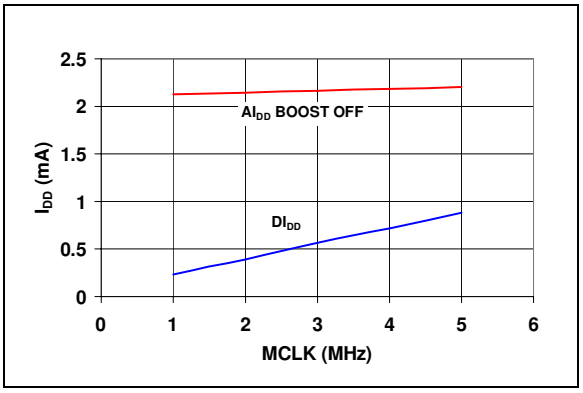



***FIGURE 2-33:*** *Operating Current vs. Master Clock (MCLK).*

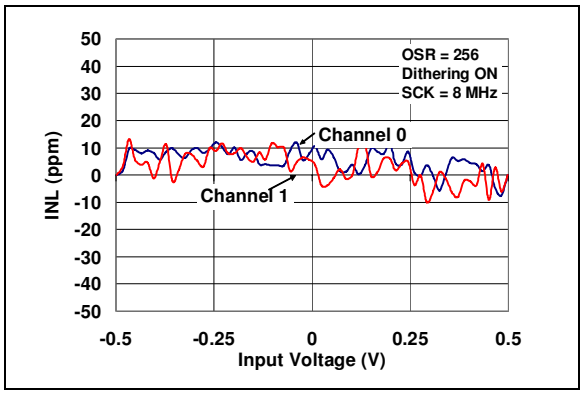



***FIGURE 2-32:*** *Integral Nonlinearity (Dithering On).*

## 3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| Symbol | Pin No. | | Function |
|---|---|---|---|
| | SSOP | QFN | |
| $\overline{\text{RESET}}$ | 1 | 18 | Master Reset Logic Input Pin |
| $DV_{DD}$ | 2 | 19 | Digital Power Supply Pin |
| $AV_{DD}$ | 3 | 20 | Analog Power Supply Pin |
| CH0+ | 4 | 1 | Non-Inverting Analog Input Pin for Channel 0 |
| CH0- | 5 | 2 | Inverting Analog Input Pin for Channel 0 |
| CH1- | 6 | 3 | Inverting Analog Input Pin for Channel 1 |
| CH1+ | 7 | 4 | Non-Inverting Analog Input Pin for Channel 1 |
| $A_{GND}$ | 8 | 5 | Analog Ground Pin, Return Path for Internal Analog Circuitry |
| REFIN+/OUT | 9 | 6 | Non-Inverting Voltage Reference Input and Internal Reference Output Pin |
| REFIN- | 10 | 7 | Inverting Voltage Reference Input Pin |
| $D_{GND}$ | 11 | 8 | Digital Ground Pin, Return Path for Internal Digital Circuitry |
| MDAT1 | 12 | 9 | Modulator Data Output Pin for Channel 1 |
| MDAT0 | 13 | 10 | Modulator Data Output Pin for Channel 0 |
| $\overline{\text{DR}}$ | 14 | 11 | Data Ready Signal Output Pin |
| OSC1/CLKI | 15 | 12 | Oscillator Crystal Connection Pin or External Clock Input Pin |
| OSC2 | 16 | 13 | Oscillator Crystal Connection Pin |
| $\overline{\text{CS}}$ | 17 | 14 | Serial Interface Chip Select Pin |
| SCK | 18 | 15 | Serial Interface Clock Pin |
| SDO | 19 | 16 | Serial Interface Data Output Pin |
| SDI | 20 | 17 | Serial Interface Data Input Pin |
| EP | — | 21 | Exposed Thermal Pad. Must be connected to AGND. |

### 3.1 $\overline{\text{RESET}}$

This pin is active low and places the entire chip in a Reset state when active.

When $\overline{\text{RESET}}$ = 0, all registers are reset to their default value, no communication can take place and no clock is distributed inside the part. This state is equivalent to a POR state.

Since the default state of the ADCs is on, the analog power consumption when $\overline{\text{RESET}}$ = 0 is equivalent to when $\overline{\text{RESET}}$ = 1. Only the digital power consumption is largely reduced because this current consumption is essentially dynamic and is reduced drastically when there is no clock running.

All the analog biases are enabled during a Reset so that the part is fully operational just after a $\overline{\text{RESET}}$ rising edge.

This input is Schmitt triggered.

### 3.2 Digital $V_{DD}$ ($DV_{DD}$)

$DV_{DD}$ is the power supply pin for the digital circuitry within the MCP3901. This pin requires appropriate bypass capacitors and should be maintained between 2.7V and 5.5V for specified operation.

### 3.3 Analog $V_{DD}$ ($AV_{DD}$)

$AV_{DD}$ is the power supply pin for the analog circuitry within the MCP3901.

This pin requires appropriate bypass capacitors and should be maintained to 5V ±10% for specified operation.

## 3.4 ADC Differential Analog inputs (CHn+/CHn-)

CH0- and CH0+, and CH1- and CH1+, are the two fully differential analog voltage inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±500 mV/GAIN with $V_{REF}$ = 2.4V.

The maximum absolute voltage, with respect to AGND, for each CHn+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

## 3.5 Analog Ground (AGND)

AGND is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). To ensure accuracy and noise cancellation, this pin must be connected to the same ground as DGND, preferably with a star connection. If an analog ground plane is available, it is recommended that this pin be tied to this plane of the PCB. This plane should also reference all other analog circuitry in the system.

## 3.6 Non-Inverting Reference Input, Internal Reference Output (REFIN+/OUT)

This pin is the non-inverting side of the differential voltage reference input for both ADCs or the internal voltage reference output.

When VREFEXT = 1, and an external voltage reference source can be used, the internal voltage reference is disabled. When using an external differential voltage reference, it should be connected to its $V_{REF}$+ pin. When using an external single-ended reference, it should be connected to this pin.

When VREFEXT = 0, the internal voltage reference is enabled and connected to this pin through a switch. This voltage reference has minimal drive capability, and thus, needs proper buffering and bypass capacitances (10 µF tantalum in parallel with 0.1 µF ceramic) if used as a voltage source.

For optimal performance, bypass capacitances should be connected between this pin and AGND at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

## 3.7 Inverting Reference Input (REFIN-)

This pin is the inverting side of the differential voltage reference input for both ADCs. When using an external differential voltage reference, it should be connected to its $V_{REF-}$ pin. When using an external, single-ended voltage reference, or when VREFEXT = 0 (default) and using the internal voltage reference, this pin should be directly connected to AGND.

## 3.8 Digital Ground Connection (DGND)

DGND is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). To ensure accuracy and noise cancellation, DGND must be connected to the same ground as AGND, preferably with a star connection. If a digital ground plane is available, it is recommended that this pin be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other digital circuitry in the system.

## 3.9 Modulator Data Output Pin for Channel 1 and Channel 0 (MDAT1/MDAT0)

MDAT0 and MDAT1 are the output pins for the modulator serial bitstreams of ADC Channels 0 and 1, respectively. These pins are high-impedance by default. When the MODOUT<1:0> are enabled, the modulator bitstream of the corresponding channel is present on the pin and updated at the AMCLK frequency. (See **Section 5.4 "Modulator Output Block"** for a complete description of the modulator outputs.) These pins can be directly connected to a MCU or DSP when a specific digital filtering is needed.

## 3.10 $\overline{DR}$ (Data Ready Pin)

The data ready pin indicates if a new conversion result is ready to be read. The default state of this pin is high when DR_HIZN = 1 and is high-impedance when DR_HIZN = 0 (default). After each conversion is finished, a low pulse will take place on the data ready pin to indicate the conversion result is ready as an interrupt. This pulse is synchronous with the master clock and has a defined and constant width.

The data ready pin is independent of the SPI interface and acts like an interrupt output. The data ready pin state is not latched and the pulse width (and period) are both determined by the MCLK frequency, over-sampling rate and internal clock prescale settings. The $\overline{DR}$ pulse width is equal to one DMCLK period and the frequency of the pulses is equal to DRCLK (see Figure 1-3).

| **Note:** | This pin should not be left floating when the DR_HIZN bit is low; a 100 kΩ pull-up resistor connected to $D_{VDD}$ is recommended. |
|---|---|

### 3.11 Oscillator and Master Clock Input Pins (OSC1/CLKI, OSC2)

OSC1/CLKI and OSC2 provide the master clock for the device. When CLKEXT = 0 (default), a resonant crystal or clock source with a similar sinusoidal waveform must be placed across these pins to ensure proper operation. The typical clock frequency specified is 4 MHz. However, the clock frequency can be 1 MHz to 5 MHz without disturbing ADC accuracy. With the current boost circuit enabled, the master clock can be used up to 8.192 MHz without disturbing ADC accuracy. Appropriate load capacitance should be connected to these pins for proper operation.

| | |
|---|---|
| **Note:** | When CLKEXT = 1, the crystal oscillator is disabled, as well as the OSC2 input. The OSC1 becomes the master clock input, CLKI, the direct path for an external clock source; for example, a clock source generated by an MCU. |

### 3.12 $\overline{CS}$ (Chip Select)

This pin is the SPI chip select that enables the serial communication. When this pin is high, no communication can take place. A chip select falling edge initiates the serial communication and a chip select rising edge terminates the communication. No communication can take place, even when $\overline{CS}$ is low and when $\overline{RESET}$ is low.

This input is Schmitt triggered.

### 3.13 SCK (Serial Data Clock)

This is the serial clock pin for SPI communication.

Data is clocked into the device on the rising edge of SCK. Data is clocked out of the device on the falling edge of SCK.

The MCP3901 interface is compatible with both SPI 0,0 and 1,1 modes. SPI modes can only be changed during a Reset.

The maximum clock speed specified is 20 MHz when $DV_{DD}$ > 4.5V and 10 MHz otherwise.

This input is Schmitt triggered.

### 3.14 SDO (Serial Data Output)

This is the SPI data output pin. Data is clocked out of the device on the falling edge of SCK.

This pin stays high-impedance during the first command byte. It also stays high-impedance during the whole communication for write commands, and when the $\overline{CS}$ pin is high or when the $\overline{RESET}$ pin is low. This pin is active only when a read command is processed. Each read is processed by a packet of 8 bits.

### 3.15 SDI (Serial Data Input)

This is the SPI data input pin. Data is clocked into the device on the rising edge of SCK.

When $\overline{CS}$ is low, this pin is used to communicate with a series of 8-bit commands.

The interface is half-duplex (inputs and outputs do not happen at the same time).

Each communication starts with a chip select falling edge, followed by an 8-bit command word entered through the SDI pin. Each command is either a read or a write command. Toggling SDI during a read command has no effect.

This input is Schmitt triggered.

**NOTES:**

## 4.0 TERMINOLOGY AND FORMULAS

This section defines the terms and formulas used throughout this data sheet. The following terms are defined:

MCLK – Master Clock

AMCLK – Analog Master Clock

DMCLK – Digital Master Clock

DRCLK – Data Rate Clock

Oversampling Ratio (OSR)

Offset Error

Gain Error

Integral Nonlinearity Error

Signal-to-Noise Ratio (SNR)

Signal-to-Noise Ratio And Distortion (SINAD)

Total Harmonic Distortion (THD)

Spurious-Free Dynamic Range (SFDR)

MCP3901 Delta-Sigma Architecture

Idle Tones

Dithering

Crosstalk

PSRR

CMRR

ADC Reset Mode

Hardware Reset Mode ($\overline{\text{RESET}}$ = 0)

ADC Shutdown Mode

Full Shutdown Mode

### 4.1 MCLK – Master Clock

This is the fastest clock present in the device. This is the frequency of the crystal placed at the OSC1/OSC2 inputs when CLKEXT = 0 or the frequency of the clock input at the OSC1/CLKI when CLKEXT = 1 (see Figure 1-5).

### 4.2 AMCLK – Analog Master Clock

This is the clock frequency that is present on the analog portion of the device, after prescaling has occurred via the CONFIG1 PRESCALE<1:0> register bits. The analog portion includes the PGAs and the two Sigma-Delta modulators.

**EQUATION 4-1:**

$$AMCLK = \frac{MCLK}{PRESCALE}$$

**TABLE 4-1: MCP3901 OVERSAMPLING RATIO SETTINGS**

| Config PRE<1:0> | | Analog Master Clock Prescale |
|---|---|---|
| 0 | 0 | AMCLK = MCLK/1 (default) |
| 0 | 1 | AMCLK = MCLK/2 |
| 1 | 0 | AMCLK = MCLK/4 |
| 1 | 1 | AMCLK = MCLK/8 |

### 4.3 DMCLK – Digital Master Clock

This is the clock frequency that is present on the digital portion of the device, after prescaling and division by 4. This is also the sampling frequency, which is the rate when the modulator outputs are refreshed. Each period of this clock corresponds to one sample and one modulator output (see Figure 1-5).

**EQUATION 4-2:**

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times PRESCALE}$$

### 4.4 DRCLK – Data Rate Clock

This is the output data rate (i.e., the rate at which the ADCs output new data). Each new data is signaled by a Data Ready pulse on the $\overline{\text{DR}}$ pin.

This data rate is depending on the OSR and the prescaler with the following formula:

**EQUATION 4-3:**

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$

Since this is the output data rate, and since the decimation filter is a SINC (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

The following table describes the various combinations of OSR and PRESCALE, and their associated AMCLK, DMCLK and DRCLK rates.

**TABLE 4-2: DEVICE DATA RATES IN FUNCTION OF MCLK, OSR AND PRESCALE**

| PRE <1:0> | | OSR <1:0> | | OSR | AMCLK | DMCLK | DRCLK | DRCLK (ksps) | SINAD (dB) | ENOB (bits) |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 256 | MCLK/8 | MCLK/32 | MCLK/8192 | 0.4882 | 91.4 | 14.89 |
| 1 | 1 | 1 | 0 | 128 | MCLK/8 | MCLK/32 | MCLK/4096 | 0.976 | 86.6 | 14.10 |
| 1 | 1 | 0 | 1 | 64 | MCLK/8 | MCLK/32 | MCLK/2048 | 1.95 | **78.7** | **12.78** |
| 1 | 1 | 0 | 0 | 32 | MCLK/8 | MCLK/32 | MCLK/1024 | 3.9 | 68.2 | 11.04 |
| 1 | 0 | 1 | 1 | 256 | MCLK/4 | MCLK/16 | MCLK/4096 | 0.976 | 91.4 | 14.89 |
| 1 | 0 | 1 | 0 | 128 | MCLK/4 | MCLK/16 | MCLK/2048 | 1.95 | 86.6 | 14.10 |
| 1 | 0 | 0 | 1 | 64 | MCLK/4 | MCLK/16 | MCLK/1024 | 3.9 | **78.7** | **12.78** |
| 1 | 0 | 0 | 0 | 32 | MCLK/4 | MCLK/16 | MCLK/512 | 7.8125 | 68.2 | 11.04 |
| 0 | 1 | 1 | 1 | 256 | MCLK/2 | MCLK/8 | MCLK/2048 | 1.95 | 91.4 | 14.89 |
| 0 | 1 | 1 | 0 | 128 | MCLK/2 | MCLK/8 | MCLK/1024 | 3.9 | 86.6 | 14.10 |
| 0 | 1 | 0 | 1 | 64 | MCLK/2 | MCLK/8 | MCLK/512 | 7.8125 | **78.7** | **12.78** |
| 0 | 1 | 0 | 0 | 32 | MCLK/2 | MCLK/8 | MCLK/256 | 15.625 | 68.2 | 11.04 |
| 0 | 0 | 1 | 1 | 256 | MCLK | MCLK/4 | MCLK/1024 | 3.9 | 91.4 | 14.89 |
| 0 | 0 | 1 | 0 | 128 | MCLK | MCLK/4 | MCLK/512 | 7.8125 | 86.6 | 14.10 |
| **0** | **0** | **0** | **1** | **64** | **MCLK** | MCLK/4 | MCLK/256 | **15.625** | **78.7** | **12.78** |
| 0 | 0 | 0 | 0 | 32 | MCLK | MCLK/4 | MCLK/128 | 31.25 | 68.2 | 11.04 |

**Note:** For OSR = 32 and 64, DITHER = 0. For OSR = 128 and 256, DITHER = 1.

## 4.5 Oversampling Ratio (OSR)

The ratio of the sampling frequency to the output data rate is OSR = DMCLK/DRCLK. The default OSR is 64 or with MCLK = 4 MHz and PRESCALE = 1, AMCLK = 4 MHz, $f_S$ = 1 MHz, $f_D$ = 15.625 ksps. The following bits in the CONFIG1 register are used to change the Oversampling Ratio (OSR).

**TABLE 4-3: MCP3901 OVERSAMPLING RATIO SETTINGS**

| CONFIG OSR<1:0> | | OVERSAMPLING RATIO OSR |
|---|---|---|
| 0 | 0 | 32 |
| 0 | 1 | 64 (default) |
| 1 | 0 | 128 |
| 1 | 1 | 256 |

## 4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together ($V_{IN}$ = 0V). The specification incorporates both PGA and ADC offset contributions. This error varies with PGA and OSR settings. The offset is different on each channel and varies from chip to chip. This offset error can easily be calibrated out by a MCU with a subtraction. The offset is specified in mV.

The offset on the MCP3901 has a low temperature coefficient; see **Section 2.0 "Typical Performance Curves"**.

## 4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in percent (%) compared to the ideal transfer function defined by Equation 5-3. The specification incorporates both PGA and ADC gain error contributions, but not the $V_{REF}$ contribution (it is measured with an external $V_{REF}$). This error varies with PGA and OSR settings.

The gain error on the MCP3901 has a low temperature coefficient; see the typical performance curves for more information, Figure 2-24 and Figure 2-25.

## 4.8 Integral Nonlinearity Error

Integral nonlinearity error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed, or with the end points equal to zero.

It is the maximum remaining error after calibration of offset and gain errors for a DC input signal.

## 4.9 Signal-to-Noise Ratio (SNR)

For the MCP3901 ADC, the Signal-to-Noise ratio is a ratio of the output fundamental signal power to the noise power (not including the harmonics of the signal), when the input is a sinewave at a predetermined frequency. It is measured in dB. Usually, only the maximum Signal-to-Noise ratio is specified. The SNR calculation mainly depends on the OSR and DITHER settings of the device.

**EQUATION 4-4: SIGNAL-TO-NOISE RATIO**

$$SNR(dB) = 10log\left(\frac{SignalPower}{NoisePower}\right)$$

## 4.10 Signal-to-Noise Ratio And Distortion (SINAD)

The most important figure of merit, for the analog performance of the ADCs present on the MCP3901, is the Signal-to-Noise and Distortion (SINAD) specification.

Signal-to-Noise and distortion ratio are similar to the Signal-to-Noise ratio, with the exception that you must include the harmonics power in the noise power calculation. The SINAD specification mainly depends on the OSR and DITHER settings.

**EQUATION 4-5: SINAD EQUATION**

$$SINAD(dB) = 10log\left(\frac{SignalPower}{Noise + HarmonicsPower}\right)$$

The calculated combination of SNR and THD per the following formula also yields SINAD:

**EQUATION 4-6: SINAD, THD AND SNR RELATIONSHIP**

$$SINAD(dB) = 10log\left[10^{\left(\frac{SNR}{10}\right)} + 10^{\left(\frac{-THD}{10}\right)}\right]$$

## 4.11 Total Harmonic Distortion (THD)

The total harmonic distortion is the ratio of the output harmonic's power to the fundamental signal power for a sinewave input and is defined by Equation 4-7:

**EQUATION 4-7:**

$$THD(dB) = 10log\left(\frac{HarmonicsPower}{FundamentalPower}\right)$$

The THD calculation includes the first 35 harmonics for the MCP3901 specifications. The THD is usually only measured with respect to the 10 first harmonics. THD is sometimes expressed in %. For converting the THD in %, here is the formula:

**EQUATION 4-8:**

$$THD(\%) = 100 \times 10^{\frac{THD(dB)}{20}}$$

This specification depends mainly on the DITHER setting.

## 4.12 Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio between the output power of the fundamental and the highest spur in the frequency spectrum. The spur frequency is not necessarily a harmonic of the fundamental, even though it is usually the case. This figure represents the dynamic range of the ADC when a full-scale signal is used at the input. This specification depends mainly on the DITHER setting.

**EQUATION 4-9:**

$$SFDR(dB) = 10log\left(\frac{FundamentalPower}{HighestSpurPower}\right)$$

## 4.13 MCP3901 Delta-Sigma Architecture

The MCP3901 incorporates two Delta-Sigma ADCs with a multi-bit architecture. A Delta-Sigma ADC is an oversampling converter that incorporates a built-in modulator, which is digitizing the quantity of charge integrated by the modulator loop (see Figure 5-1). The quantizer is the block that is performing the Analog-to-Digital conversion. The quantizer is typically 1 bit, or a simple comparator which helps to maintain the linearity performance of the ADC (the DAC structure, is in this case, inherently linear).

Multi-bit quantizers help to lower the quantization error (the error fed back in the loop can be very large with 1-bit quantizers) without changing the order of the modulator or the OSR, which leads to better SNR figures. Typically, however, the linearity of such architectures is more difficult to achieve, since the DAC is no more simple to realize, and its linearity limits the THD of such ADCs.

The MCP3901's 5-level quantizer is a Flash ADC, composed of 4 comparators arranged with equally spaced thresholds and a thermometer coding. The MCP3901 also includes proprietary 5-level DAC architecture that is inherently linear for improved THD figures.

## 4.14 Idle Tones

A Delta-Sigma Converter is an integrating converter. It also has a finite quantization step (LSB) which can be detected by its quantizer. A DC input voltage that is below the quantization step should only provide an all zeros result, since the input is not large enough to be detected. As an integrating device, any Delta-Sigma will show, in this case, Idle tones. This means that the output will have spurs in the frequency content that are depending on the ratio between quantization step voltage and the input voltage. These spurs are the result of the integrated sub-quantization step inputs that will eventually cross the quantization steps after a long enough integration. This will induce an AC frequency at the output of the ADC and can be shown in the ADC output spectrum.

These Idle tones are residues that are inherent to the quantization process and the fact that the converter is integrating at all times without being reset. They are residues of the finite resolution of the conversion process. They are very difficult to attenuate and they are heavily signal dependent. They can degrade both the SFDR and THD of the converter, even for DC inputs. They can be localized in the baseband of the converter, and thus, difficult to filter from the actual input signal.

For power metering applications, Idle tones can be very disturbing because energy can be detected even at the 50 or 60 Hz frequency, depending on the DC offset of the ADCs, while no power is really present at the inputs. The only practical way to suppress or attenuate the Idle tones phenomenon is to apply dithering to the ADC. The Idle tone amplitudes are a function of the order of the modulator, the OSR and the number of levels in the quantizer of the modulator. A higher order, a higher OSR or a higher number of levels for the quantizer will attenuate the Idle tones amplitude.

## 4.15 Dithering

In order to suppress or attenuate the Idle tones present in any Delta-Sigma ADCs, dithering can be applied to the ADC. Dithering is the process of adding an error to the ADC feedback loop in order to "decorrelate" the outputs and "break" the Idle tones behavior. Usually, a random or pseudo-random generator adds an analog or digital error to the feedback loop of the Delta-Sigma ADC in order to ensure that no tonal behavior can happen at its outputs. This error is filtered by the feedback loop, and typically, has a zero average value so that the converter static transfer function is not disturbed by the dithering process. However, the dithering process slightly increases the noise floor (it adds noise to the part) while reducing its tonal behavior, and thus, improving SFDR and THD (see Figure 2-10 and Figure 2-14). The dithering process scrambles the Idle tones into baseband white noise and ensures that dynamic specs (SNR, SINAD, THD, SFDR) are less signal dependent. The MCP3901 incorporates a proprietary dithering algorithm on both ADCs in order to remove Idle tones and improve THD, which is crucial for power metering applications.

## 4.16 Crosstalk

The crosstalk is defined as the perturbation caused by one ADC channel on the other ADC channel. It is a measurement of the isolation between the two ADCs present in the chip.

This measurement is a two-step procedure:

1. Measure one ADC input with no perturbation on the other ADC (ADC inputs shorted).
2. Measure the same ADC input with a perturbation sine wave signal on the other ADC at a certain predefined frequency.

The crosstalk is then the ratio between the output power of the ADC when the perturbation is present and when it is not divided by the power of the perturbation signal.

A lower crosstalk value implies more independence and isolation between the two channels.

The measurement of this signal is performed under the following conditions:

- GAIN = 1,
- PRESCALE = 1,
- OSR = 256,
- MCLK = 4 MHz

### Step 1

- CH0+ = CH0- = AGND
- CH1+ = CH1- = AGND

### Step 2

- CH0+ = CH0- = AGND
- CH1+ – CH1- = 1 $V_{P-P}$ @ 50/60 Hz (full-scale sine wave)

The crosstalk is then calculated with the following formula:

**EQUATION 4-10:**

$$CTalk(dB) = 10log\left(\frac{\Delta CH0Power}{\Delta CH1Power}\right)$$

## 4.17 PSRR

This is the ratio between a change in the power supply voltage and the ADC output codes. It measures the influence of the power supply voltage on the ADC outputs.

The PSRR specification can be DC (the power supply is taking multiple DC values) or AC (the power supply is a sinewave at a certain frequency with a certain common-mode). In AC, the amplitude of the sinewave is representing the change in the power supply.

It is defined as:

**EQUATION 4-11:**

$$PSRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta AV_{DD}}\right)$$

Where $V_{OUT}$ is the equivalent input voltage that the output code translates to with the ADC transfer function. In the MCP3901 specification, $AV_{DD}$ varies from 4.5V to 5.5V, and for AC PSRR, a 50/60 Hz sinewave is chosen, centered around 5V with a maximum 500 mV amplitude. The PSRR specification is measured with $AV_{DD} = DV_{DD}$.

## 4.18 CMRR

This is the ratio between a change in the common-mode input voltage and the ADC output codes. It measures the influence of the common-mode input voltage on the ADC outputs.

The CMRR specification can be DC (the common-mode input voltage is taking multiple DC values) or AC (the common-mode input voltage is a sinewave at a certain frequency with a certain common-mode). In AC, the amplitude of the sinewave is representing the change in the power supply.

It is defined as:

**EQUATION 4-12:**

$$CMRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta V_{CM}}\right)$$

Where $V_{CM}$ = (CHn+ + CHn-)/2 is the common-mode input voltage and $V_{OUT}$ is the equivalent input voltage, the output code is translated to the ADC transfer function. In the MCP3901 specification, VCM varies from -1V to +1V, and for the AC specification, a 50/60 Hz sinewave is chosen, centered around 0V, with a 500 mV amplitude.

## 4.19 ADC Reset Mode

ADC Reset mode (also called Soft Reset mode) can only be entered through setting the RESET<1:0> bits high in the Configuration register. This mode is defined as the condition where the converters are active, but their output is forced to '0'.

The registers are not affected in this Reset mode and retain their values.

The ADCs can immediately output meaningful codes after leaving Reset mode (and after the sinc filter settling time of 3/DRCLK). This mode is both entered and exited through the setting of bits in the Configuration register.

Each converter can be placed in Soft Reset mode independently. The Configuration registers are not modified by the Soft Reset mode.

A data ready pulse will not be generated by any ADC while in Reset mode.

Reset mode also effects the modulator output block (i.e., the MDAT pin, corresponding to the channel in Reset). If enabled, it provides a bitstream corresponding to a zero output (a series of '0011' bits continuously repeated).

When an ADC exits ADC Reset mode, any phase delay present, before Reset was entered, will still be present. If one ADC was not in Reset, the ADC leaving Reset mode will automatically resynchronize the phase delay. The resynchronization is relative to the other ADC channel per the Phase Delay register block and gives $\overline{DR}$ pulses accordingly.

If an ADC is placed in Reset mode while the other is converting, it is not shutting down the internal clock. When going back out of Reset, it will be resynchronized automatically with the clock that did not stop during Reset.

If both ADCs are in Soft Reset or Shutdown modes, the clock is no longer distributed to the digital core for low-power operation. Once any of the ADC is back to normal operation, the clock is automatically distributed again.

## 4.20 Hard Reset Mode ($\overline{RESET}$ = 0)

This mode is only available during a Power-on-Reset (POR) or when the $\overline{RESET}$ pin is pulled low. The $\overline{RESET}$ pin low state places the device in a Hard Reset mode.

In this mode, all internal registers are reset to their default state.

The DC biases for the analog blocks are still active (i.e., the MCP3901 is ready to convert). However, this pin clears all conversion data in the ADCs. In this mode, the MDAT outputs are in high-impedance. The comparator outputs of both ADCs are forced to their Reset state ('0011'). The SINC filters are all reset, as well as their double output buffers. See serial timing for minimum pulse low time in **Section 1.0 "Electrical Characteristics"**.

During a Hard Reset, no communication with the part is possible. The digital interface is maintained in a Reset state.

## 4.21 ADC Shutdown Mode

ADC Shutdown mode is defined as a state where the converters and their biases are off, consuming only leakage current. After this is removed, start-up delay time (SINC filter settling time) will occur before outputting meaningful codes. The start-up delay is needed to power-up all DC biases in the channel that was in shutdown. This delay is the same as $t_{POR}$ and any $\overline{DR}$ pulse coming within this delay should be discarded.

Each converter can be placed in Shutdown mode, independently. The CONFIG registers are not modified by the Shutdown mode. This mode is only available through programming the SHUTDOWN<1:0> bits in the CONFIG2 register.

The output data is flushed to all zeros while in ADC shutdown. No data ready pulses are generated by any ADC while in ADC Shutdown mode.

ADC Shutdown mode also effects the modulator output block (i.e., if MDAT of the channel in Shutdown mode is enabled). This pin will provide a bitstream corresponding to a zero output (series of '0011' bits continuously repeated).

When an ADC exits ADC Shutdown mode, any phase delay present before shutdown was entered will still be present. If one ADC was not in shutdown, the ADC leaving Shutdown mode will automatically resynchronize the phase delay relative to the other ADC channel, per the Phase Delay register block, and give $\overline{DR}$ pulses accordingly.

If an ADC is placed in Shutdown mode while the other is converting, it is not shutting down the internal clock. When going back out of shutdown, it will be resynchronized automatically with the clock that did not stop during Reset.

If both ADCs are in ADC Reset or ADC Shutdown modes, there is no more distribution of the clock to the digital core for low-power operation. Once any of the ADC is back to normal operation, the clock is automatically distributed again.

## 4.22 Full Shutdown Mode

The lowest power consumption can be achieved when SHUTDOWN<1:0> = 11 and VREFEXT = CLKEXT = 1. This mode is called "Full Shutdown mode" and no analog circuitry is enabled. In this mode, the POR $AV_{DD}$ monitoring circuit is also disabled. When the clock is Idle (CLKI = 0 or 1 continuously), no clock is propagated throughout the chip. Both ADCs are in shutdown, the internal voltage reference is disabled and the internal oscillator is disabled.

The only circuit that remains active is the SPI interface, but this circuit does not induce any static power consumption. If SCK is Idle, the only current consumption comes from the leakage currents induced by the transistors and is less than 1 µA on each power supply.

This mode can be used to power down the chip completely and avoid power consumption when there is no data to convert at the analog inputs. Any SCK or MCLK edge coming while on this mode, will induce dynamic power consumption.

Once any of the SHUTDOWN, CLKEXT and VREFEXT bits returns to '0', the POR $AV_{DD}$ monitoring block is back to operation and $AV_{DD}$ monitoring can take place.

# 5.0 DEVICE OVERVIEW

## 5.1 Analog Inputs (CHn+/-)

The MCP3901 analog inputs can be connected directly to current and voltage transducers (such as shunts, current transformers, or Rogowski coils). Each input pin is protected by specialized ESD structures that are certified to pass 7 kV HBM and 400V MM contact charge. These structures allow bipolar ±6V continuous voltage, with respect to AGND, to be present at their inputs without the risk of permanent damage.

Both channels have fully differential voltage inputs for better noise performance. The absolute voltage at each pin, relative to AGND, should be maintained in the ±1V range during operation in order to ensure the specified ADC accuracy. The common-mode signals should be adapted to respect both the previous conditions and the differential input voltage range. For best performance, the common-mode signals should be maintained to AGND.

## 5.2 Programmable Gain Amplifiers (PGA)

The two Programmable Gain Amplifiers (PGAs) reside at the front end of each Delta-Sigma ADC. They have two functions: translate the common-mode of the input from AGND to an internal level between AGND and $AV_{DD}$, and amplify the input differential signal. The translation of the common-mode does not change the differential signal, but recenters the common-mode so that the input signal can be properly amplified.

The PGA block can be used to amplify very low signals, but the differential input range of the Delta-Sigma modulator must not be exceeded. The PGA is controlled by the PGA_CHn<2:0> bits in the GAIN register. The following table represents the gain settings for the PGA:

**TABLE 5-1: PGA CONFIGURATION SETTING**

| Gain PGA_CHn<2:0> | | | Gain (V/V) | Gain (dB) | $V_{IN}$ Range (V) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | ±0.5 |
| 0 | 0 | 1 | 2 | 6 | ±0.25 |
| 0 | 1 | 0 | 4 | 12 | ±0.125 |
| 0 | 1 | 1 | 8 | 18 | ±0.0625 |
| 1 | 0 | 0 | 16 | 24 | ±0.03125 |
| 1 | 0 | 1 | 32 | 30 | ±0.015625 |

## 5.3 Delta-Sigma Modulator

### 5.3.1 ARCHITECTURE

Both ADCs are identical in the MCP3901 and they include a second-order modulator with a multi-bit DAC architecture (see Figure 5-1). The quantizer is a Flash ADC composed of 4 comparators with equally spaced thresholds and a thermometer output coding. The proprietary 5-level architecture ensures minimum quantization noise at the outputs of the modulators without disturbing linearity or inducing additional distortion. The sampling frequency is DMCLK (typically 1 MHz with MCLK = 4 MHz) so the modulator outputs are refreshed at a DMCLK rate. The modulator outputs are available in the MOD register or serially transferred on each MDAT pin.

Both modulators also include a dithering algorithm that can be enabled through the DITHER<1:0> bits in the Configuration register. This dithering process improves THD and SFDR (for high OSR settings) while slightly increasing the noise floor of the ADCs. For power metering applications and applications that are distortion-sensitive, it is recommended to keep DITHER enabled for both ADCs. In the case of power metering applications, THD and SFDR are critical specifications to optimize SNR (noise floor). This is not really problematic due to a large averaging factor at the output of the ADCs; therefore, even for low OSR settings, the dithering algorithm will show a positive impact on the performance of the application.

Figure 5-1 represents a simplified block diagram of the Delta-Sigma ADC present on MCP3901.

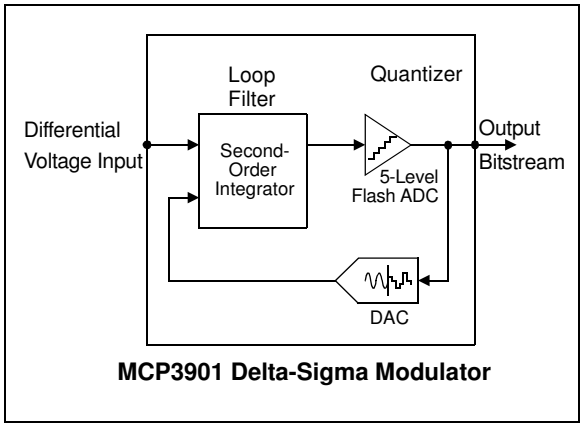



***FIGURE 5-1:*** *Simplified Delta-Sigma ADC Block Diagram.*

### 5.3.2 MODULATOR INPUT RANGE AND SATURATION POINT

For a specified voltage reference value of 2.4V, the modulators' specified differential input range is ±500 mV. The input range is proportional to $V_{REF}$ and scales according to the $V_{REF}$ voltage. This range ensures the stability of the modulator over amplitude and frequency. Outside of this range, the modulator is still functional, however, its stability is no longer ensured, and therefore, it is not recommended to exceed this limit. The saturation point for the modulator is $V_{REF}/3$, since the transfer function of the ADC includes a gain of 3 by default (independent from the PGA setting). See **Section 5.6 "ADC Output Coding"**.

### 5.3.3 BOOST MODE

The Delta-Sigma modulators also include an independent BOOST mode for each channel. If the corresponding BOOST<1:0> bits are enabled, the power consumption of the modulator is multiplied by 2. Its bandwidth is increased to be able to sustain AMCLK clock frequencies up to 8.192 MHz, while keeping the ADC accuracy. When disabled, the power consumption is back to normal and the AMCLK clock frequencies can only reach up to 5 MHz without affecting ADC accuracy.

## 5.4 Modulator Output Block

If the user wishes to use the modulator output of the device, the appropriate bits to enable the modulator output must be set in the Configuration register.

When MODOUT<1:0> are enabled, the modulator output of the corresponding channel is present at the corresponding MDAT output pin as soon as the command is placed.

Since the Delta-Sigma modulators have a 5-level output given by the state of 4 comparators with thermometer coding, their outputs can be represented on 4 bits. Each bit gives the state of the corresponding comparator (see Table 5-2). These bits are present on the MOD register and are updated at the DMCLK rate.

In order to output the comparators result on a separate pin (MDAT0 and MDAT1), these comparator output bits have been arranged to be serially output at the AMCLK rate (see Figure 5-2).

This 1-bit serial bitstream is the same as what would be produced by a 1-bit DAC modulator with a sampling frequency of AMCLK. The modulator can either be considered as a 5 level-output at DMCLK rate or a 1-bit output at AMCLK rate. These two representations are interchangeable. The MDAT outputs can, therefore, be used in any application that requires 1-bit modulator outputs. These applications will often integrate and filter the 1-bit output with SINC or more complex decimation filters computed by an MCU or a DSP.

**TABLE 5-2: DELTA-SIGMA MODULATOR CODING**

| Comp<3:0> Code | Modulator Output Code | MDAT Serial Stream |
|---|---|---|
| 1111 | +2 | 1111 |
| 0111 | +1 | 0111 |
| 0011 | 0 | 0011 |
| 0001 | -1 | 0001 |
| 0000 | -2 | 0000 |

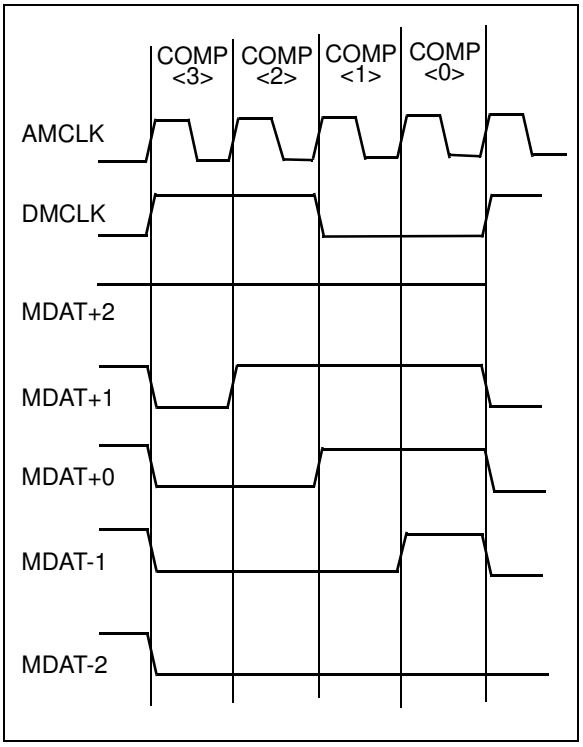



***FIGURE 5-2:*** *MDAT Serial Outputs in Function of the Modulator Output Code.*

Since the Reset and shutdown SPI commands are asynchronous, the MDAT pins are resynchronized with DMCLK after each time the part goes out of Reset and shutdown.

This means that the first output of MDAT after Reset is always '0011' after the first DMCLK rising edge.

## 5.5 SINC$^3$ Filter

Both ADCs present in the MCP3901 include a decimation filter that is a third-order sinc (or notch) filter. This filter processes the multi-bit bitstream into 16 or 24-bit words (depending on the WIDTH Configuration bit). The settling time of the filter is 3 DMCLK periods. It is recommended that unsettled data be discarded to avoid data corruption, which can be done easily by setting the DR_LTY bit high in the STATUS/COM register.

The resolution achievable at the output of the sinc filter (the output of the ADC) is dependant on the OSR and is summarized with the following table:

**TABLE 5-3: ADC RESOLUTION vs. OSR**

| OSR<1:0> | | OSR | ADC Resolution (bits) No Missing Codes |
|---|---|---|---|
| 0 | 0 | 32 | 17 |
| 0 | 1 | 64 | 20 |
| 1 | 0 | 128 | 23 |
| 1 | 1 | 256 | 24 |

For 24-Bit Output mode (WIDTH = 1), the output of the sinc filter is padded with least significant zeros for any resolution less than 24 bits.

For 16-Bit Output modes, the output of the sinc filter is rounded to the closest 16-bit number in order to conserve only 16-bit words and to minimize truncation error.

The gain of the transfer function of this filter is 1 at each multiple of DMCLK (typically 1 MHz) so a proper anti-aliasing filter must be placed at the inputs. This will attenuate the frequency content around DMCLK and keep the desired accuracy over the baseband of the converter. This anti-aliasing filter can be a simple, first-order RC network with a sufficiently low time constant to generate high rejection at DMCLK frequency.

**EQUATION 5-1: SINC FILTER TRANSFER FUNCTION H(Z)**

$$H(z) = \left(\frac{1 - z^{-OSR}}{OSR(1 - z^{-1})}\right)^3$$

Where:

$$z = \exp\left(\frac{2\pi f j}{DMCLK}\right)$$

The Normal Mode Rejection Ratio (NMRR) or gain of the transfer function is given by the following equation:

**EQUATION 5-2: MAGNITUDE OF FREQUENCY RESPONSE H(f)**

$$NMRR(f) = \left|\frac{sinc\left(\pi \cdot \frac{f}{DMCLK}\right)}{sinc\left(\pi \cdot \frac{f}{DRCLK}\right)}\right|^3$$

or:

$$NMRR(f) = \left|\frac{sinc\left(\pi \cdot \frac{f}{f_S}\right)}{sinc\left(\pi \cdot \frac{f}{f_D}\right)}\right|^3$$

where:

$$sinc(x) = \frac{sin(x)}{x}$$

Figure 5-3 shows the sinc filter frequency response:

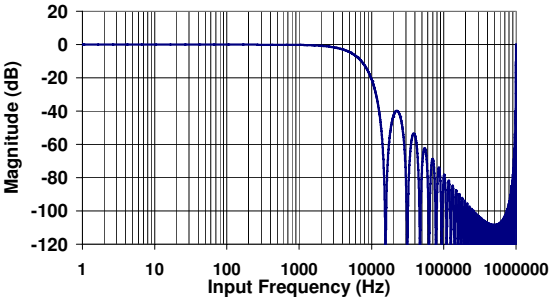



***FIGURE 5-3:*** *SINC Filter Response with MCLK = 4 MHz, OSR = 64, PRESCALE = 1.*

## 5.6 ADC Output Coding

The second-order modulator, SINC$^3$ filter, PGA, $V_{REF}$ and analog input structure all work together to produce the device transfer function for the Analog-to-Digital conversion (see Equation 5-3).

The channel data is either a 16-bit or 24-bit word, presented in a 23-bit or 15-bit plus sign, two's complement format, and is MSB (left) justified.

The ADC data is two or three bytes wide depending on the WIDTH bit of the associated channel. The 16-bit mode includes a round to the closest 16-bit word (instead of truncation) in order to improve the accuracy of the ADC data.

In case of positive saturation (CHn+ – CHn- > $V_{REF}$/3), the output is locked to 7FFFFF for 24-bit mode (7FFF for 16-bit mode). In case of negative saturation (CHn+ – CHn- < -$V_{REF}$/3), the output code is locked to 800000 for 24-bit mode (8000 for 16-bit mode).

Equation 5-3 is only true for DC inputs. For AC inputs, this transfer function needs to be multiplied by the transfer function of the SINC$^3$ filter (see Equation 5-1 and Equation 5-2).

**EQUATION 5-3:**

$$DATA\_CHn = \left(\frac{(CH_{n+} - CH_{n-})}{V_{REF+} - V_{REF-}}\right) \times 8{,}388{,}608 \times G \times 3 \quad \textbf{(For 24-Bit Mode or WIDTH = 1)}$$

$$DATA\_CHn = \left(\frac{(CH_{n+} - CH_{n-})}{V_{REF+} - V_{REF-}}\right) \times 32{,}768 \times G \times 3 \quad \textbf{(For 16-Bit Mode or WIDTH = 0)}$$

### 5.6.1 ADC RESOLUTION AS A FUNCTION OF OSR

The ADC resolution is a function of the OSR (**Section 5.5 "SINC3 Filter"**). The resolution is the same for both channels. No matter what the resolution is, the ADC output data is always presented in 24-bit words, with added zeros at the end if the OSR is not large enough to produce 24-bit resolution (left justification).

**TABLE 5-4: OSR = 256 OUTPUT CODE EXAMPLES**

| ADC Output Code (MSB First) | Hexadecimal | Decimal |
|---|---|---|
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | 0x7FFFFF | + 8,388,607 |
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 | 0x7FFFFE | + 8,388,606 |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0x000000 | 0 |
| 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | 0xFFFFFF | -1 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 | 0x800001 | - 8,388,607 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0x800000 | - 8,388,608 |

**TABLE 5-5: OSR = 128 OUTPUT CODE EXAMPLES**

| ADC Output Code (MSB First) | Hexadecimal | Decimal 23-Bit Resolution |
|---|---|---|
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 | 0x7FFFFE | + 4,194,303 |
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 0 0 | 0x7FFFFC | + 4,194,302 |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0x000000 | 0 |
| 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 | 0xFFFFFE | -1 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 | 0x800002 | - 4,194,303 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0x800000 | - 4,194,304 |

**TABLE 5-6: OSR = 64 OUTPUT CODE EXAMPLES**

| ADC Output code (MSB First) | Hexadecimal | Decimal 20-Bit Resolution |
|---|---|---|
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 | 0x7FFFF0 | + 524, 287 |
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 | 0x7FFFE0 | + 524, 286 |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0x000000 | 0 |
| 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 | 0xFFFFF0 | -1 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 | 0x800010 | - 524,287 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0x800000 | - 524, 288 |

**TABLE 5-7: OSR = 32 OUTPUT CODE EXAMPLES**

| ADC Output code (MSB First) | Hexadecimal | Decimal 17-Bit Resolution |
|---|---|---|
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 | 0x7FFF80 | + 65, 535 |
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 | 0x7FFF00 | + 65, 534 |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0x000000 | 0 |
| 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 | 0xFFFF80 | -1 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 | 0x800080 | - 65,535 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0x800000 | - 65, 536 |

## 5.7 Voltage Reference

### 5.7.1 INTERNAL VOLTAGE REFERENCE

The MCP3901 contains an internal voltage reference source, specially designed to minimize drift over temperature. In order to enable the internal voltage reference, the VREFEXT bit in the Configuration register must be set to '0' (Default mode). This internal $V_{REF}$ supplies reference voltage to both channels. The typical value of this voltage reference is 2.37V ±2%. The internal reference has a very low typical temperature coefficient of ±12 ppm/°C, allowing the output codes to have minimal variation with respect to temperature, since they are proportional to ($1/V_{REF}$).

The noise of the internal voltage reference is low enough not to significantly degrade the SNR of the ADC if compared to a precision, external low noise voltage reference.

The output pin for the internal voltage reference is REFIN+/OUT.

When the internal voltage reference is enabled, the REFIN- pin should always be connected to AGND.

For optimal ADC accuracy, appropriate bypass capacitors should be placed between REFIN+/OUT and AGND. Decoupling at the sampling frequency, around 1 MHz, is important for any noise around this frequency will be aliased back into the conversion data (0.1 µF ceramic and 10 µF tantalum capacitors are recommended).

These bypass capacitors are not mandatory for correct ADC operation, but removing these capacitors may degrade the accuracy of the ADC. The bypass capacitors also help the applications where the voltage reference output is connected to other circuits. In this case, additional buffering may be needed as the output drive capability of this output is low.

### 5.7.2 DIFFERENTIAL EXTERNAL VOLTAGE INPUTS

When the VREFEXT bit is high, the two reference pins (REFIN+/OUT, REFIN-) become a differential voltage reference input. The voltage at the REFIN+/OUT pin is noted as $V_{REF}+$ and the voltage at the REFIN- pin is noted as $V_{REF}-$. The differential voltage input value is given by the following equation:

**EQUATION 5-4:**

$$V_{REF} = V_{REF}+ - V_{REF}-$$

The specified $V_{REF}$ range is from 2.2V to 2.6V. The REFIN- pin voltage ($V_{REF}-$) should be limited to ±0.3V. Typically, for single-ended reference applications, the REFIN- pin should be directly connected to AGND.

## 5.8 Power-on Reset

The MCP3901 contains an internal POR circuit that monitors analog supply voltage $AV_{DD}$ during operation. The typical threshold for a power-up event detection is 4.2V ±5%. The POR circuit has a built-in hysteresis for improved transient spikes immunity that has a typical value of 200 mV. Proper decoupling capacitors (0.1 µF ceramic and 10 µF tantalum) should be mounted as close as possible to the $AV_{DD}$ pin, providing additional transient immunity.

Figure 5-4 illustrates the different conditions at power-up and a power-down event in the typical conditions. All internal DC biases are not settled until at least 50 µs after system POR. Any $\overline{DR}$ pulses during this time, after a system Reset, should be ignored. After POR, $\overline{DR}$ pulses are present at the pin with all the default conditions in the Configuration registers.

Both $AV_{DD}$ and $DV_{DD}$ power supplies are independent. Since $AV_{DD}$ is the only power supply that is monitored, it is highly recommended to power up $DV_{DD}$ first as a power-up sequence. If $AV_{DD}$ is powered up first, it is highly recommended to keep the $\overline{RESET}$ pin low during the whole power-up sequence.

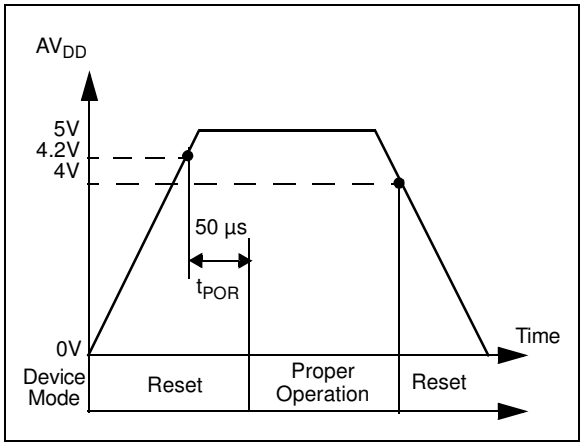



***FIGURE 5-4:*** *Power-on Reset Operation.*

## 5.9 $\overline{RESET}$ Effect on Delta-Sigma Modulator/SINC Filter

When the $\overline{RESET}$ pin is low, both ADCs will be in Reset and output code, 0x0000h. The $\overline{RESET}$ pin performs a Hard Reset (DC biases still on, part ready to convert) and clears all charges contained in the Delta-Sigma modulators. The comparators' output is '0011' for each ADC.

The SINC filters are all reset, as well as their double output buffers. This pin is independent of the serial interface. It brings the CONFIG registers to the default state. When $\overline{RESET}$ is low, any write with the SPI interface will be disabled and will have no effect. All output pins (SDO, $\overline{DR}$, MDAT0/1) are high-impedance, and no clock is propagated through the chip.

## 5.10 Phase Delay Block

The MCP3901 incorporates a phase delay generator which ensures that the two ADCs are converting the inputs with a fixed delay between them. The two ADCs are synchronously sampling but the averaging of modulator outputs is delayed. Therefore, the SINC filter outputs (thus, the ADC outputs) show a fixed phase delay, as determined by the PHASE register setting.

The PHASE register (PHASE<7:0>) is a 7 bit + sign, MSB first, two's complement register that indicates how much phase delay there is to be between Channel 0 and Channel 1. The reference channel for the delay is Channel 1 (typically the voltage channel for power metering applications). When PHASE<7:0> are positive, Channel 0 is lagging versus Channel 1. When PHASE<7:0> are negative, Channel 0 is leading versus Channel 1. The amount of delay between two ADC conversions is given by the following formula:

**EQUATION 5-5:**

$$Delay = \frac{Phase\ Register\ Code}{DMCLK}$$

The timing resolution of the phase delay is 1/DMCLK or 1 µs in the default configuration with MCLK = 4 MHz.

The data ready signals are affected by the phase delay settings. Typically, the time difference between the data ready pulses of Channel 0 and Channel 1 is equal to the phase delay setting.

**Note:** A detailed explanation of the Data Ready pin ($\overline{DR}$) with phase delay is present in **Section 6.10 "Data Ready Latches and Data Ready Modes (DRMODE<1:0>)"**.

### 5.10.1 PHASE DELAY LIMITS

The phase delay can only go from -OSR/2 to +OSR/2 – 1. This sets the fine phase resolution. The PHASE register is coded with two's complement.

If larger delays between the two channels are needed, they can be implemented externally to the chip with an MCU. A FIFO in the MCU can save incoming data from the leading channel for a number N of DRCLK clocks. In this case, DRCLK would represent the coarse timing resolution, and DMCLK, the fine timing resolution. The total delay will then be equal to:

Delay = N/DRCLK + PHASE/DMCLK

The Phase Delay register can be programmed once with the OSR = 256 setting and will adjust to the OSR automatically afterwards, without the need to change the value of the PHASE register.

- **OSR = 256**: The delay can go from -128 to +127. PHASE<7> is the sign bit, PHASE<6> is the MSB and PHASE<0> is the LSB.
- **OSR = 128:** The delay can go from -64 to +63. PHASE<6> is the sign bit, PHASE<5> is the MSB and PHASE<0> is the LSB.
- **OSR = 64**: The delay can go from -32 to +31. PHASE<5> is the sign bit, PHASE<4> is the MSB and PHASE<0> is the LSB.
- **OSR = 32:** The delay can go from -16 to +15. PHASE<4> is the sign bit, PHASE<3> is the MSB and PHASE<0> is the LSB.

**TABLE 5-8: PHASE VALUES WITH MCLK = 4 MHZ, OSR = 256**

| PHASE Register Value | Hex | Delay (CH0 relative to CH1) |
|---|---|---|
| 0 1 1 1 1 1 1 1 | 0x7F | +127 µs |
| 0 1 1 1 1 1 1 0 | 0x7E | +126 µs |
| 0 0 0 0 0 0 0 1 | 0x01 | +1 µs |
| 0 0 0 0 0 0 0 0 | 0x00 | 0 µs |
| 1 1 1 1 1 1 1 1 | 0xFF | -1 µs |
| 1 0 0 0 0 0 0 1 | 0x81 | -127 µs |
| 1 0 0 0 0 0 0 0 | 0x80 | -128 µs |

## 5.11 Crystal Oscillator

The MCP3901 includes a Pierce-type crystal oscillator with very high stability and ensures very low temperature and jitter for the clock generation. This oscillator can handle up to 16.384 MHz crystal frequencies provided that proper load capacitances and the quartz quality factor are used.

For keeping specified ADC accuracy, AMCLK should be kept between 1 and 5 MHz with BOOST off or 1 and 8.192 MHz with BOOST on. Larger MCLK frequencies can be used provided the prescaler clock settings allow the AMCLK to respect these ranges.

For a proper start-up, the load capacitors of the crystal should be connected between OSC1 and DGND, and between OSC2 and DGND. They should also respect the following equation:

**EQUATION 5-6:**

$$R_M < 1.6 \times 10^6 \times \left(\frac{1}{f \times C_{LOAD}}\right)^2$$

Where:

| | | |
|---|---|---|
| f | = | Crystal frequency in MHz |
| $C_{LOAD}$ | = | Load capacitance in pF including parasitics from the PCB |
| $R_M$ | = | Motional resistance in ohms of the quartz |

When CLKEXT = 1, the crystal oscillator is bypassed by a digital buffer to allow direct clock input for an external clock (see Figure 1-5).

**NOTES:**

# 6.0 SERIAL INTERFACE DESCRIPTION

## 6.1 Overview

The MCP3901 device is compatible with SPI Modes 0,0 and 1,1. Data is clocked *out* of the MCP3901 on the *falling* edge of SCK and data is clocked *into* the MCP3901 on the *rising* edge of SCK. In these modes, SCK can Idle either high or low.

Each SPI communication starts with a $\overline{CS}$ falling edge and stops with the $\overline{CS}$ rising edge. Each SPI communication is independent. When $\overline{CS}$ is high, SDO is in high-impedance, and transitions on SCK and SDI have no effect. Additional controls: $\overline{RESET}$, $\overline{DR}$ and MDAT0/1 are also provided on separate pins for advanced communication.

The MCP3901 interface has a simple command structure. The first byte transmitted is always the CONTROL byte and is followed by data bytes that are 8-bit wide. Both ADCs are continuously converting data by default and can be reset or shut down through a CONFIG2 register setting.

Since each ADC data is either 16 or 24 bits (depending on the WIDTH bits), the internal registers can be grouped together with various configurations (through the READ bits) in order to allow easy data retrieval within only one communication. For device reads, the internal address counter can be automatically incremented in order to loop through groups of data within the register map. The SDO will then output the data located at the ADDRESS (A<4:0>) defined in the control byte and then ADDRESS + 1 depending on the READ<1:0> bits, which select the groups of registers. These groups are defined in **Section 7.1 "ADC Channel Data Output Registers"** (Register Map).

The Data Ready pin ($\overline{DR}$) can be used as an interrupt for an MCU and outputs pulses when new ADC channel data is available. The $\overline{RESET}$ pin acts like a Hard Reset and can reset the part to its default power-up configuration. The MDAT0/1 pins give the modulator outputs (see **Section 5.4 "Modulator Output Block"**).

## 6.2 Control Byte

The control byte of the MCP3901 contains two device Address bits, A<6:5>, 5 register Address bits, A<4:0>, and a Read/Write bit (R/$\overline{W}$). The first byte transmitted to the MCP3901 is always the control byte.

The MCP3901 interface is device addressable (through A<6:5>) so that multiple MCP3901 chips can be present on the same SPI bus with no data bus contention. This functionality enables three-phase power metering systems, containing three MCP3901 chips, controlled by a single SPI bus (single $\overline{CS}$, SCK, SDI and SDO pins).

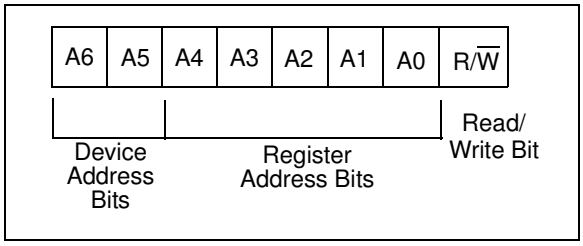



***FIGURE 6-1:*** *Control Byte.*

The default device address bits are '00'. Contact the Microchip factory for additional device address bits. For more information, please see the Product Identification System section.

A read on undefined addresses will give an all zeros output on the first, and all subsequent transmitted bytes. A write on an undefined address will have no effect and also, will not increment the address counter.

The register map is defined in **Section 7.1 "ADC Channel Data Output Registers"**.

## 6.3 Reading from the Device

The first data byte read is the one defined by the address given in the CONTROL byte. After this first byte is transmitted, if the $\overline{CS}$ pin is maintained low, the communication continues and the address of the next transmitted byte is determined by the status of the READ bits in the STATUS/COM register. Multiple looping configurations can be defined through the READ<1:0> bits for the address increment (see **Section 6.6 "SPI MODE 0,0 – Clock Idle Low, Read/ Write Examples"**).

## 6.4 Writing to the Device

The first data byte written is the one defined by the address given in the control byte. The write communication automatically increments the address for subsequent bytes.

The address of the next transmitted byte within the same communication ($\overline{CS}$ stays low) is the next address defined on the register map. At the end of the register map, the address loops to the beginning of the register map. Writing a non-writable register has no effect.

The SDO pin stays in high-impedance during a write communication.

## 6.5 SPI MODE 1,1 – Clock Idle High, Read/Write Examples

In this SPI mode, the clock Idles high. For the MCP3901, this means that there will be a falling edge before there is a rising edge.

| **Note:** | Changing from an SPI Mode 1,1 to an SPI Mode 0,0 is possible, but needs a Reset pulse in-between to ensure correct communication. |
|---|---|

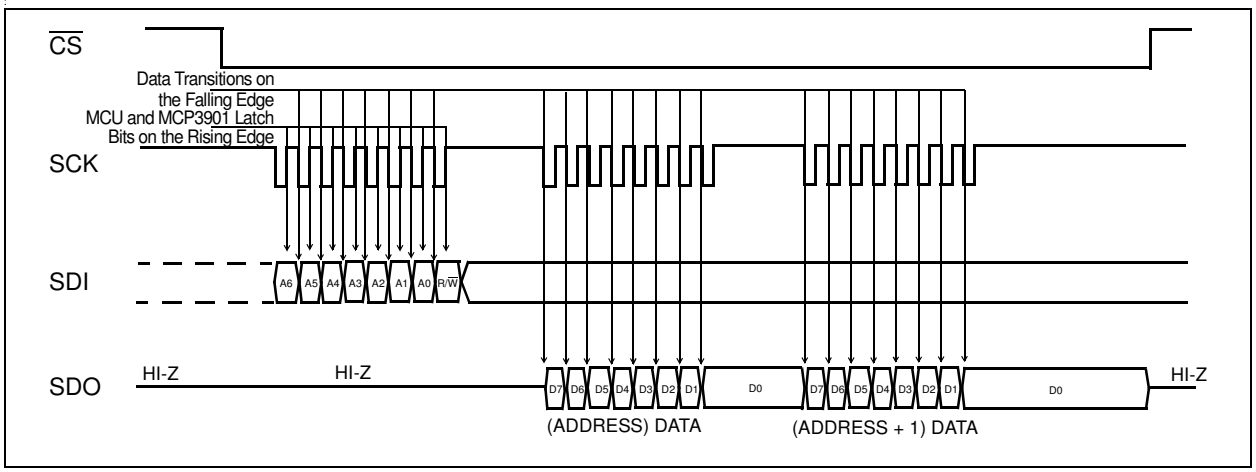



***FIGURE 6-2:*** *Device Read (SPI Mode 1,1 – Clock Idles High).*

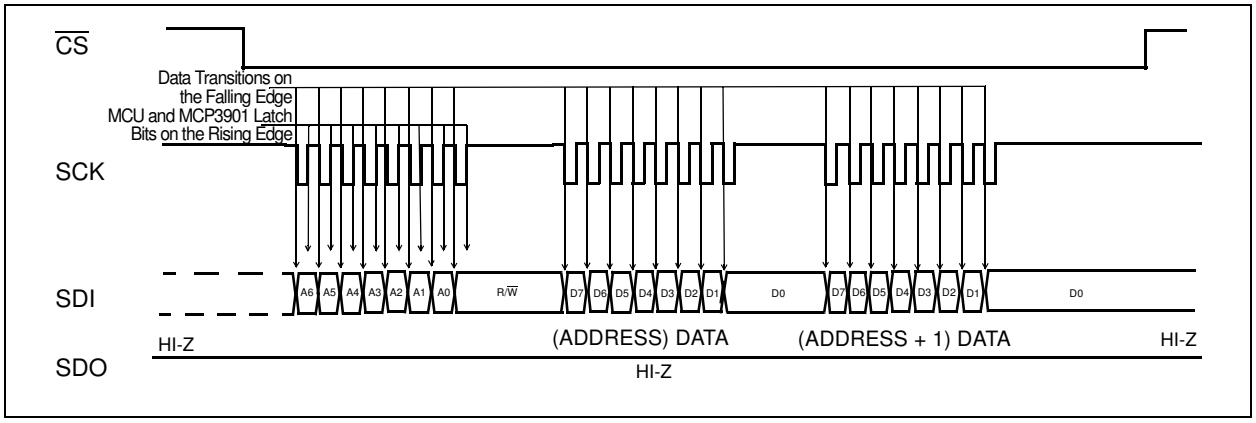



***FIGURE 6-3:*** *Device Write (SPI Mode 1,1 – Clock Idles High).*

## 6.6 SPI MODE 0,0 – Clock Idle Low, Read/Write Examples

In this SPI mode, the clock Idles low. For the MCP3901, this means that there will be a rising edge before there is a falling edge.

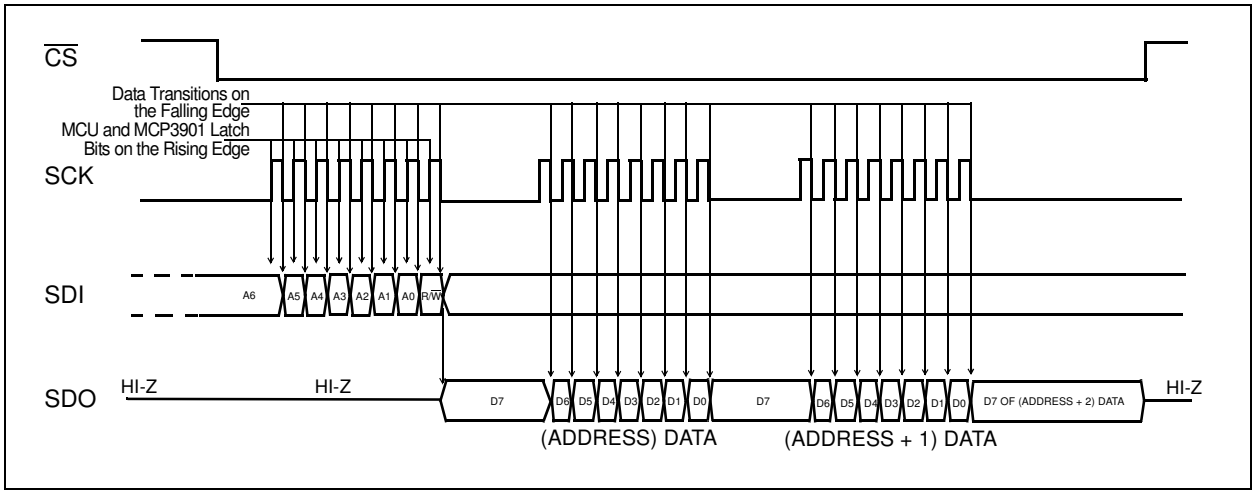



***FIGURE 6-4:*** *Device Read (SPI Mode 0,0 – Clock Idles Low).*

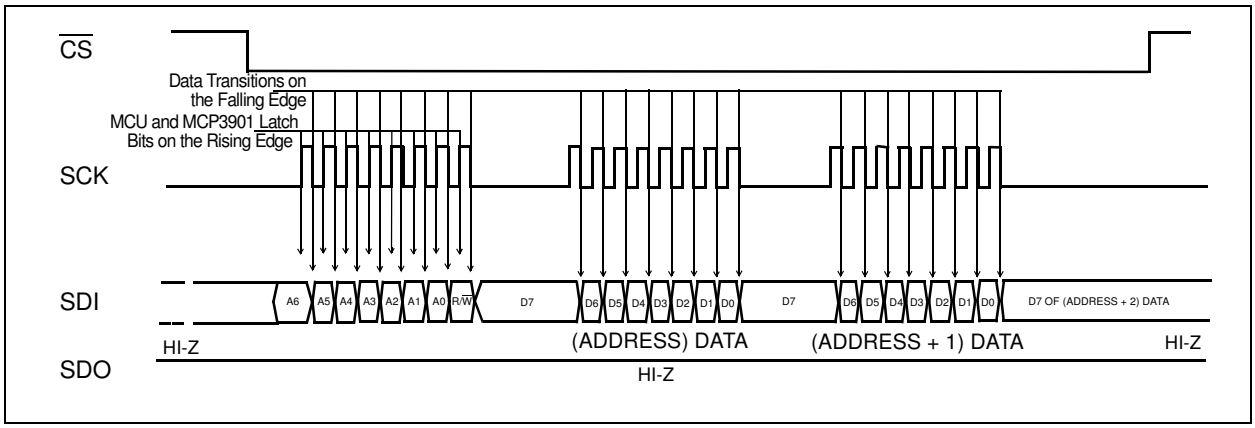



***FIGURE 6-5:*** *Device Write (SPI Mode 0,0 – Clock Idles Low).*

## 6.7 Continuous Communication, Looping on Address Sets

If the user wishes to read back either of the ADC channels continuously, or both channels continuously, the internal address counter of the MCP3901 can be set to loop on specific register sets. In this case, there is only one control byte on SDI to start the communication. The part stays within the same loop until $\overline{CS}$ returns high.

This internal address counter allows the following functionality:

- Read one ADC channel's data continuously
- Read both ADC channel's data continuously (both ADC data can be independent or linked with DRMODE settings)
- Continuously read the entire register map
- Continuously read each separate register
- Continuously read all Configuration registers
- Write all Configuration registers in one communication (see Figure 6-7)

The STATUS/COM register contains the loop settings for the internal address counter (READ<1:0>). The internal address counter can either stay constant (READ<1:0> = 00) and continuously read the same byte, or it can auto-increment and loop through the register groups defined below (READ<1:0> = 01), register types (READ<1:0> = 10) or the entire register map (READ<1:0> = 11).

Each channel is configured independently as either a 16-bit or 24-bit data word, depending on the setting of the corresponding WIDTH bit in the CONFIG1 register.

For continuous reading, in the case of WIDTH = 0 (16-bit), the lower byte of the ADC data is not accessed and the part jumps automatically to the following address (the user does not have to clock out the lower byte since it becomes undefined for WIDTH = 0).

Figure 6-6 represents a typical, continuous read communication with the default settings (DRMODE<1:0> = 00, READ<1:0> = 10) for both WIDTH settings. This configuration is typically used for power metering applications.

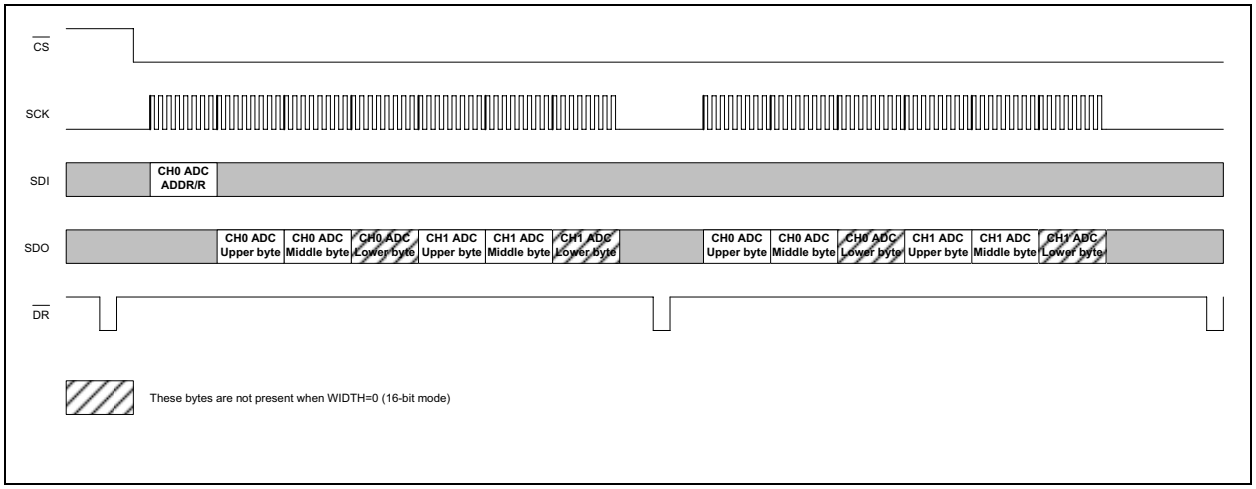



***FIGURE 6-6:*** *Typical Continuous Read Communication.*

### 6.7.1 CONTINUOUS WRITE

Both ADCs are powered up with their default configurations, and begin to output $\overline{DR}$ pulses immediately (RESET<1:0> and SHUTDOWN<1:0> bits are off by default).

The default output codes for both ADCs are all zeros. The default modulator output for both ADCs is '0011' (corresponding to a theoretical zero voltage at the inputs). The default phase is zero between the two channels.

It is recommended to enter into ADC Reset mode for both ADCs, just after power-up, because the desired MCP3901 register configuration may not be the default one, and in this case, the ADC would output undesired data. Within the ADC Reset mode (RESET<1:0> = 11), the user can configure the whole part with a single communication. The write commands automatically increment the address so that the user can start writing the PHASE register and finish with the CONFIG2 register in only one communication (see Figure 6-7). The RESET<1:0> bits are in the CONFIG2 register to allow exiting the Soft Reset mode, and have the whole part configured and ready to run in only one command.

The following register sets are defined as groups:

**TABLE 6-1: REGISTER GROUPS**

| Group | Addresses |
|---|---|
| ADC DATA CH0 | 0x00-0x02 |
| ADC DATA CH1 | 0x03-0x05 |
| MOD, PHASE, GAIN | 0x06-0x08 |
| CONFIG, STATUS | 0x09-0x0B |

The following register sets are defined as types:

**TABLE 6-2: REGISTER TYPES**

| Type | Addresses |
|---|---|
| ADC DATA (both channels) | 0x00-0x05 |
| CONFIGURATION | 0x06-0x0B |

## 6.8 Situations that Reset ADC Data

Immediately after the following actions, the ADCs are temporarily reset in order to provide proper operation:

1. Change in PHASE register.
2. Change in the OSR setting.
3. Change in the PRESCALE setting.
4. Overwrite of the same PHASE register value.
5. Change in the CLKEXT bit in the CONFIG2 register, modifying internal oscillator state.

After these temporary Resets, the ADCs go back to the normal operation with no need for an additional command. These are also the settings where the $\overline{DR}$ position is affected. The PHASE register can be used to serially Soft Reset the ADCs, without using the RESET bits in the Configuration register, if the same value is written in the PHASE register.

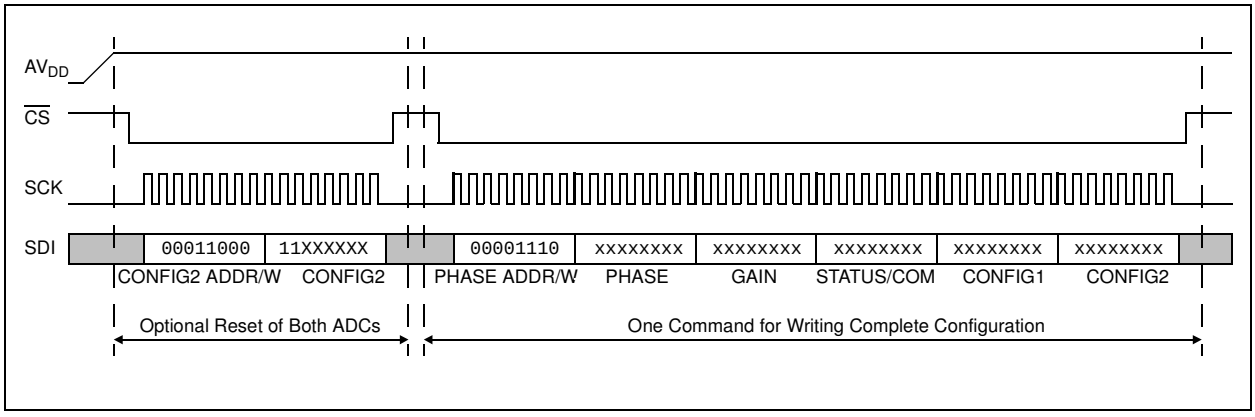



***FIGURE 6-7:*** *Recommended Configuration Sequence at Power-up.*

## 6.9 Data Ready Pin ($\overline{DR}$)

To signify when channel data is ready for transmission, the data ready signal is available on the Data Ready pin ($\overline{DR}$) through an active-low pulse at the end of a channel conversion.

The data ready pin outputs an active-low pulse with a period that is equal to the DRCLK clock period, and with a width equal to one DMCLK period.

When not active-low, this pin can either be in high-impedance (when DR_HIZN = 0) or in a defined logic high state (when DR_HIZN = 1). This is controlled through the Configuration registers. This allows multiple devices to share the same data ready pin (with a pull-up resistor connected between $\overline{DR}$ and $DV_{DD}$) in 3-phase, energy meter designs to reduce pin count. A single device on the bus does not require a pull-up resistor.

After a data ready pulse has occurred, the ADC output data can be read through SPI communication. Two sets of latches at the output of the ADC prevent the communication from outputting corrupted data (see **Section 6.10 "Data Ready Latches and Data Ready Modes (DRMODE<1:0>)"**).

The $\overline{CS}$ pin has no effect on the $\overline{DR}$ pin, which means even if $\overline{CS}$ is high, data ready pulses will be provided (except when the configuration prevents them from outputting data ready pulses). The $\overline{DR}$ pin can be used as an interrupt when connected to an MCU or DSP. While the $\overline{RESET}$ pin is low, the $\overline{DR}$ pin is not active.

## 6.10 Data Ready Latches and Data Ready Modes (DRMODE<1:0>)

To ensure that both channels' ADC data is present at the same time for SPI read, regardless of phase delay settings for either or both channels, there are two sets of latches in series with both the data ready and the 'read start' triggers.

The first set of latches holds each output when the data is ready and latches both outputs together when DRMODE<1:0> = 00. When this mode is on, both ADCs work together and produce one set of available data after each data ready pulse (that corresponds to the lagging ADC data ready). The second set of latches ensures that when reading starts on an ADC output, the corresponding data is latched so that no data corruption can occur.

If an ADC read has started, in order to read the following ADC output, the current reading needs to be completed (all bits must be read from the ADC Output Data registers).

### 6.10.1 DATA READY PIN ($\overline{DR}$) CONTROL USING DRMODE BITS

There are four modes that control the data ready pulses and these modes are set with the DRMODE<1:0> bits in the STATUS/COM register. For power metering applications, DRMODE<1:0> = 00 is recommended (Default mode).

The position of the $\overline{DR}$ pulses vary, with respect to this mode, to the OSR and to the PHASE settings:

- **DRMODE<1:0> = 11:** Both data ready pulses from ADC Channel 0 and ADC Channel 1 are output on the $\overline{DR}$ pin.
- **DRMODE<1:0> = 10:** Data ready pulses from ADC Channel 1 are output on the $\overline{DR}$ pin. The $\overline{DR}$ from ADC Channel 0 is not present on the pin.
- **DRMODE<1:0> = 01:** Data ready pulses from ADC Channel 0 are output on the $\overline{DR}$ pin. The $\overline{DR}$ from ADC Channel 1 is not present on the pin.
- **DRMODE<1:0> = 00 (Recommended and Default mode):** Data ready pulses from the lagging ADC between the two are output on the $\overline{DR}$ pin. The lagging ADC depends on the PHASE register and on the OSR. In this mode, the two ADCs are linked together so their data is latched together when the lagging ADC output is ready.

### 6.10.2 $\overline{DR}$ PULSES WITH SHUTDOWN OR RESET CONDITIONS

There will be no $\overline{DR}$ pulses if DRMODE<1:0> = 00 when either one or both of the ADCs are in Reset or shutdown. In Mode 0,0, a $\overline{DR}$ pulse only happens when both ADCs are ready. Any $\overline{DR}$ pulse will correspond to one data on both ADCs. The two ADCs are linked together and act as if there was only one channel with the combined data of both ADCs. This mode is very practical when both ADC channels' data retrieval and processing need to be synchronized, as in power metering applications.

| | |
|---|---|
| **Note:** | If DRMODE<1:0> = 11, the user will still be able to retrieve the $\overline{DR}$ pulse for the ADC not in shutdown or Reset (i.e., only 1 ADC channel needs to be awake). |

Figure 6-8 represents the behavior of the data ready pin with the different DRMODE and DR_LTY configurations, while shutdown or Resets are applied.

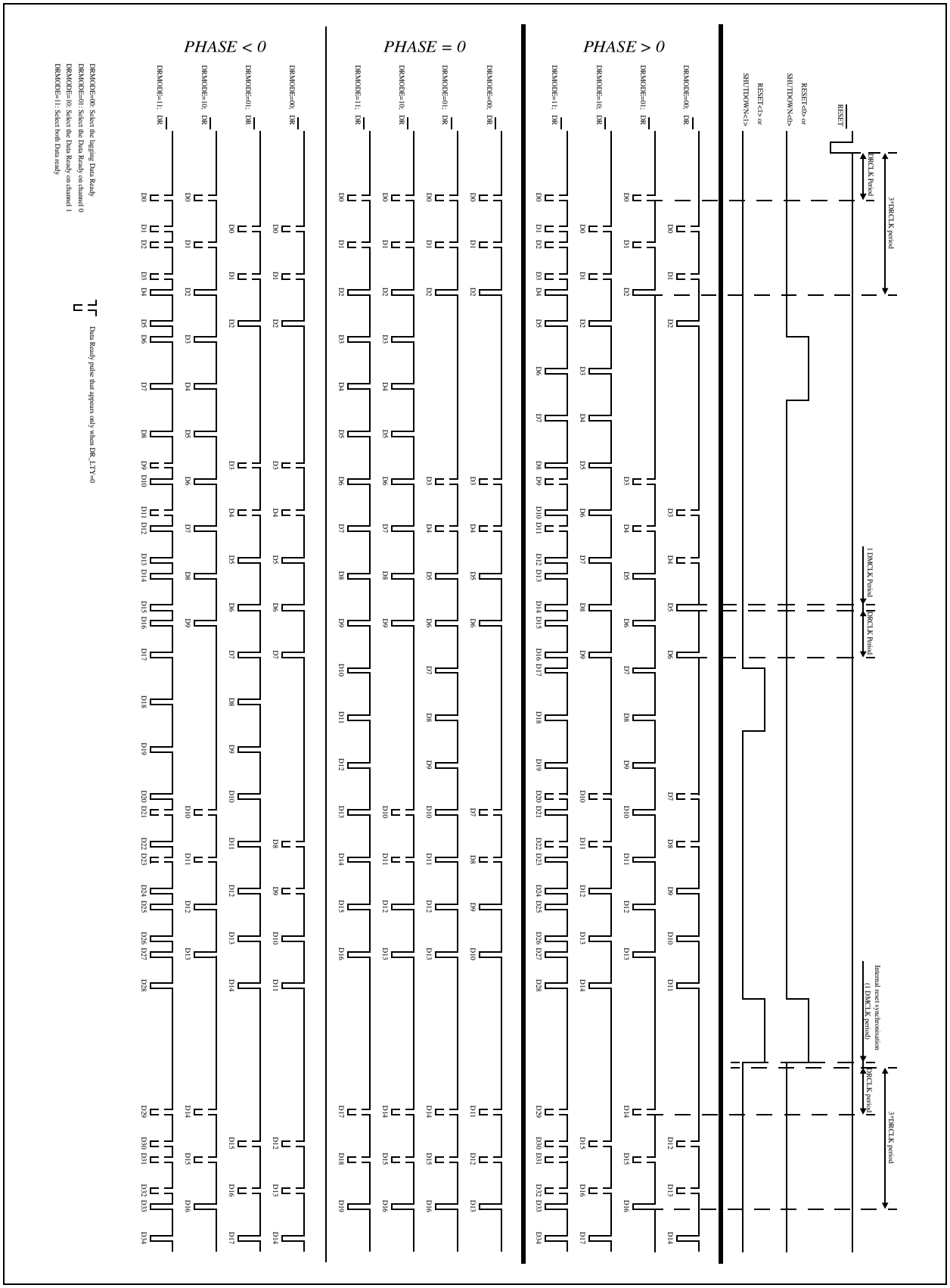



***FIGURE 6-8:*** *Data Ready Behavior.*

## 7.0 INTERNAL REGISTERS

The addresses associated with the internal registers are listed below. A detailed description of the registers follows. All registers are 8-bit long and can be addressed separately. Read modes define the groups and types of registers for continuous read communication or looping on address sets.

**TABLE 7-1: REGISTER MAP**

| Address | Name | Bits | R/W | Description |
|---|---|---|---|---|
| 0x00 | DATA_CH0 | 24 | R | Channel 0 ADC Data <23:0>, MSB First |
| 0x03 | DATA_CH1 | 24 | R | Channel 1 ADC Data <23:0>, MSB First |
| 0x06 | MOD | 8 | R/W | Delta-Sigma Modulators Output Register |
| 0x07 | PHASE | 8 | R/W | Phase Delay Configuration Register |
| 0x08 | GAIN | 8 | R/W | Gain Configuration Register |
| 0x09 | STATUS/COM | 8 | R/W | Status/Communication Register |
| 0x0A | CONFIG1 | 8 | R/W | Configuration Register 1 |
| 0x0B | CONFIG2 | 8 | R/W | Configuration Register 2 |

**TABLE 7-2: REGISTER MAP GROUPING FOR CONTINUOUS READ MODES**

| Function | Address | READ<1:0> | | |
|---|---|---|---|---|
| | | = 01 | = 10 | = 11 |
| DATA_CH0 | 0x00 | GROUP | TYPE | LOOP ENTIRE REGISTER MAP |
| | 0x01 | | | |
| | 0x02 | | | |
| DATA_CH1 | 0x03 | GROUP | | |
| | 0x04 | | | |
| | 0x05 | | | |
| MOD | 0x06 | GROUP | TYPE | |
| PHASE | 0x07 | | | |
| GAIN | 0x08 | | | |
| STATUS/ COM | 0x09 | GROUP | | |
| CONFIG1 | 0x0A | | | |
| CONFIG2 | 0x0B | | | |

## 7.1 ADC Channel Data Output Registers

The ADC Channel Data Output registers always contain the most recent A/D conversion data for each channel. These registers are read-only. They can be accessed independently or linked together (with READ<1:0> bits). These registers are latched when an ADC read communication occurs. When a data ready event occurs during a read communication, the most current ADC data is also latched to avoid data corruption issues. The three bytes of each channel are updated synchronously at a DRCLK rate. The three bytes can be accessed separately, if needed, but are refreshed synchronously.

**REGISTER 7-1: CHANNEL OUTPUT REGISTERS: ADDRESS 0x00-0x02: CH0; 0x03-0x05; CH1**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DATA_CHn <23> | DATA_CHn <22> | DATA_CHn <21> | DATA_CHn <20> | DATA_CHn <19> | DATA_CHn <18> | DATA_CHn <17> | DATA_CHn <16> |
| bit 23 | | | | | | | bit 16 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DATA_CHn <15> | DATA_CHn <14> | DATA_CHn <13> | DATA_CHn <12> | DATA_CHn <11> | DATA_CHn <10> | DATA_CHn <9> | DATA_CHn <8> |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DATA_CHn <7> | DATA_CHn <6> | DATA_CHn <5> | DATA_CHn <4> | DATA_CHn <3> | DATA_CHn <2> | DATA_CHn <1> | DATA_CHn <0> |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-0 **DATA_CHn<23:0>**

## 7.2 Modulator Output Register

The MOD register contains the most recent modulator data output. The default value corresponds to an equivalent input of 0V on both ADCs. Each bit in this register corresponds to one comparator output on one of the channels.

This register should be used as a read-only register. **(Note 1)**.

This register is updated at the refresh rate of DMCLK (typically, 1 MHz with MCLK = 4 MHz).

See **Section 5.4 "Modulator Output Block"** for more details.

**REGISTER 7-2: MODULATOR OUTPUT REGISTER (MOD): ADDRESS 0x06**

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| COMP3_CH1 | COMP2_CH1 | COMP1_CH1 | COMP0_CH1 | COMP3_CH0 | COMP2_CH0 | COMP1_CH0 | COMP0_CH0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-4 **COMPn_CH1:** Comparator Outputs from Channel 1 Modulator bits

bit 3-0 **COMPn_CH0:** Comparator Outputs from Channel 0 Modulator bits

**Note 1:** This register can be written in order to overwrite modulator output data, but any writing here will corrupt the ADC_DATA on the next three data ready pulses.

## 7.3 PHASE Register

The PHASE register (PHASE<7:0>) is a 7 bits + sign, MSB first, two's complement register that indicates how much phase delay there should be between Channel 0 and Channel 1.

The reference channel for the delay is Channel 1, which typically, is the voltage channel when used in energy metering applications (i.e., when PHASE register code is positive, Channel 0 is lagging Channel 1).

When PHASE register code is negative, Channel 0 is leading versus Channel 1.

The delay is given by the following formula:

**EQUATION 7-1:**

$$Delay = \frac{Phase\ Register\ Code}{DMCLK}$$

### 7.3.1 PHASE RESOLUTION FROM OSR

The timing resolution of the phase delay is 1/DMCLK, or 1 µs, in the default configuration (MCLK = 4 MHz). The PHASE register coding depends on the OSR setting:

- **OSR = 256:** The delay can go from -128 to +127. PHASE<7> is the sign bit. Phase<6> is the MSB and PHASE<0> the LSB.
- **OSR = 128:** The delay can go from -64 to +63. PHASE<6> is the sign bit. Phase<5> is the MSB and PHASE<0> the LSB.
- **OSR = 64:** The delay can go from -32 to +31. PHASE<5> is the sign bit. Phase<4> is the MSB and PHASE<0> the LSB.
- **OSR = 32:** The delay can go from -16 to +15. PHASE<4> is the sign bit. Phase<3> is the MSB and PHASE<0> the LSB.

**REGISTER 7-3: PHASE REGISTER (PHASE): ADDRESS 0x07**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASE<7> | PHASE<6> | PHASE<5> | PHASE<4> | PHASE<3> | PHASE<2> | PHASE<1> | PHASE<0> |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0 **PHASE<7:0>:** CH0 Relative to CH1 Phase Delay bits

Delay = PHASE Register's two's complement code/DMCLK (Default PHASE = 0).

## 7.4 Gain Configuration Register

This register contains the settings for the PGA gains for each channel as well as the BOOST options for each channel.

**REGISTER 7-4: GAIN CONFIGURATION REGISTER (GAIN): ADDRESS 0x08**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PGA_CH1 <2> | PGA_CH1 <1> | PGA_CH1 <0> | BOOST_ CH1 | BOOST_ CH0 | PGA_CH0 <2> | PGA_CH0 <1> | PGA_CH0 <0> |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **PGA_CH1<2:0>:** PGA Setting for Channel 1 bits
- 111 = Reserved (Gain = 1)
- 110 = Reserved (Gain = 1)
- 101 = Gain is 32
- 100 = Gain is 16
- 011 = Gain is 8
- 010 = Gain is 4
- 001 = Gain is 2
- 000 = Gain is 1

bit 4-3 **BOOST_CH<1:0>** Current Scaling for High-Speed Operation bits
- 11 = Both channels have current x 2
- 10 = Channel 1 has current x 2
- 01 = Channel 0 has current x 2
- 00 = Neither channel has current x 2

bit 2-0 **PGA_CH0<2:0>:** PGA Setting for Channel 0 bits
- 111 = Reserved (Gain = 1)
- 110 = Reserved (Gain = 1)
- 101 = Gain is 32
- 100 = Gain is 16
- 011 = Gain is 8
- 010 = Gain is 4
- 001 = Gain is 2
- 000 = Gain is 1

## 7.5 Status and Communication Register

This register contains all settings related to the communication, including data ready settings and status, and Read mode settings.

### 7.5.1 DATA READY ($\overline{DR}$) LATENCY CONTROL – DR_LTY

This bit determines if the first data ready pulses correspond to settled data or unsettled data from each $SINC^3$ filter. Unsettled data will provide $\overline{DR}$ pulses every DRCLK period. If this bit is set, unsettled data will wait for 3 DRCLK periods before giving $\overline{DR}$ pulses and will then give $\overline{DR}$ pulses every DRCLK period.

### 7.5.2 DATA READY ($\overline{DR}$) PIN HIGH Z – DR_HIZN

This bit defines the non-active state of the data ready pin (logic 1 or high-impedance). Using this bit, the user can connect multiple chips with the same $\overline{DR}$ pin with a pull-up resistor (DR_HIZN = 0) or a single chip with no external component (DR_HIZN = 1).

### 7.5.3 DATA READY MODE – DRMODE<1:0>

If one of the channels is in Reset or shutdown, only one of the data ready pulses is present and the situation is similar to DRMODE = 01 or 10. In the '01', '10' and '11' modes, the ADC channel data to be read is latched at the beginning of a reading in order to prevent the case of erroneous data when a $\overline{DR}$ pulse happens during a read. In these modes, the two channels are independent.

When these bits are equal to '11','10' or '01', they control which ADC's data ready is present on the $\overline{DR}$ pin. When DRMODE = 00, the data ready pin output is synchronized with the lagging ADC channel (defined by the PHASE register) and the ADCs are linked together. In this mode, the output of the two ADCs is latched synchronously at the moment of the $\overline{DR}$ event. This prevents bad synchronization between the two ADCs. The output is also latched at the beginning of a reading in order not to be updated during a read and not to give erroneous data.

This mode is very useful for power metering applications because the data from both ADCs can be retrieved, using this single data ready event, and processed synchronously even in case of a large phase difference. This mode works as if there was one ADC channel and its data would be 48 bits long and contain both channel data. As a consequence, if one channel is in Reset or shutdown when DRMODE = 00, no data ready pulse will be present at the outputs (if both channels are not ready in this mode, the data is not considered ready).

See **Section 6.9 "Data Ready Pin (DR)"** for more details about data ready pin behavior.

### 7.5.4 DR STATUS FLAG – DRSTATUS<1:0>

These bits indicate the $\overline{DR}$ status of both channels, respectively. These flags are set to logic high after each read of the STATUS/COM register. These bits are cleared when a $\overline{DR}$ event has happened on its respective ADC channel. Writing these bits has no effect.

| | |
|---|---|
| **Note:** | These bits are useful if multiple devices share the same $\overline{DR}$ output pin (DR_HIZN = 0), in order to understand what $\overline{DR}$ event happened. This configuration can be used for three-phase power metering systems, where all three phases share the same data ready pin. In case the DRMODE = 00 (linked ADCs), these data ready status bits will be updated synchronously upon the same event (lagging ADC is ready). These bits are also useful in systems where the $\overline{DR}$ pin is not used to save MCU I/O. |

**REGISTER 7-5: STATUS AND COMMUNICATION REGISTER: ADDRESS 0x09**

| R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| READ<1> | READ<0> | DR_LTY | DR_HIZN | DRMODE<1> | DRMODE<0> | DRSTATUS_CH1 | DRSTATUS_CH0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **READ<1:0>:** Address Loop Setting bits

11 = Address counter loops on entire register map
10 = Address counter loops on register types (default)
01 = Address counter loops on register groups
00 = Address not incremented, continually read same single register

bit 5 **DR_LTY:** Data Ready Latency Control bit

1 = "No Latency" Conversion, $\overline{DR}$ pulses after 3 DRCLK periods (default)
0 = Unsettled Data is available after every DRCLK period

bit 4 **DR_HIZN:** Data Ready Pin Inactive State Control bit

1 = The data ready pin default state is a logic high when data is NOT ready
0 = The data ready pin default state is high-impedance when data is NOT ready (default)

bit 3-2 **DRMODE<1:0>:** Data Ready Pin (DR) Control bits

11 = Both Data Ready pulses from ADC0 and ADC Channel 1 are output on the $\overline{DR}$ pin.
10 = Data Ready pulses from ADC Channel 1 are output on the $\overline{DR}$ pin. $\overline{DR}$ from ADC Channel 0 are not present on the pin.
01 = Data Ready pulses from ADC Channel 0 are output on the $\overline{DR}$ pin. $\overline{DR}$ from ADC Channel 1 are not present on the pin.
00 = Data Ready pulses from the lagging ADC between the two are output on the $\overline{DR}$ pin. The lagging ADC selection depends on the PHASE register and on the OSR (default).

bit 1-0 **DRSTATUS_CH<1:0>:** Data Ready Status bits

11 = ADC Channel 1 and Channel 0 data is not ready (default)
10 = ADC Channel 1 data is not ready, ADC Channel 0 data is ready
01 = ADC Channel 0 data is not ready, ADC Channel 1 data is ready
00 = ADC Channel 1 and Channel 0 data is ready

## 7.6 Configuration Registers

The Configuration registers contain settings for the internal clock prescaler, the oversampling ratio, the Channel 0 and Channel 1 width settings of 16 or 24 bits, the modulator output control settings, the state of the channel Resets and shutdowns, the dithering algorithm control (for Idle tones suppression), and the control bits for the external VREF and external CLK.

**REGISTER 7-6: CONFIGURATION REGISTERS: CONFIG1: ADDRESS 0x0A, CONFIG2: ADDRESS 0x0B**

| R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PRESCALE <1> | PRESCALE <0> | OSR<1> | OSR<0> | WIDTH _CH1 | WIDTH _CH0 | MODOUT _CH1 | MODOUT _CH0 |
| bit 15 | | | | | | | bit 8 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| RESET _CH1 | RESET _CH0 | SHUTDOWN _CH1 | SHUTDOWN _CH0 | DITHER _CH1 | DITHER _CH0 | VREFEXT | CLKEXT |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **PRESCALE<1:0>:** Internal Master Clock (AMCLK) Prescaler Value bits
11 = AMCLK = MCLK/8
10 = AMCLK = MCLK/4
01 = AMCLK = MCLK/2
00 = AMCLK = MCLK (default)

bit 13-12 **OSR<1:0>:** Oversampling Ratio for Delta-Sigma A/D Conversion bits (all channels, DMCLK/DRCLK)
11 = 256
10 = 128
01 = 64 (default)
00 = 32

bit 11-10 **WIDTH_CH<1:0>:** ADC Channel Output Data Word Width bits
1 = 24-bit mode
0 = 16-bit mode (default)

bit 9-8 **MODOUT_CH<1:0>:** Modulator Output Setting for MDAT Pins bits
11 = Both CH0 and CH1 modulator outputs present on MDAT1 and MDAT0 pins
10 = CH1 ADC modulator output present on MDAT1 pin
01 = CH0 ADC modulator output present on MDAT0 pin
00 = No modulator output is enabled (default)

bit 7-6 **RESET_CH<1:0>:** Reset Mode Setting for ADCs bits
11 = Both CH0 and CH1 ADC are in Reset mode
10 = CH1 ADC in Reset mode
01 = CH0 ADC in Reset mode
00 = Neither Channel in Reset mode (default)

bit 5-4 **SHUTDOWN_CH<1:0>:** Shutdown Mode Setting for ADCs bits
11 = Both CH0 and CH1 ADC are in Shutdown
10 = CH1ADC is in shutdown
01 = CH0 ADC is in shutdown
00 = Neither Channel is in shutdown (default)

bit 3-2 **DITHER_CH<1:0>:** Control for Dithering Circuit bits
11 = Both CH0 and CH1 ADC have dithering circuit applied (default)
10 = Only CH1 ADC has dithering circuit applied
01 = Only CH0 ADC has dithering circuit applied
00 = Neither Channel has dithering circuit applied

**REGISTER 7-6: CONFIGURATION REGISTERS: CONFIG1: ADDRESS 0x0A, CONFIG2: ADDRESS 0x0B (CONTINUED)**

bit 1 **VREFEXT:** Internal Voltage Reference Shutdown Control bit

1 = Internal voltage reference disabled, an external voltage reference must be placed between REFIN+/OUT and REFIN-

0 = Internal voltage reference enabled (default)

bit 0 **CLKEXT:** Clock Mode bit

1 = External Clock mode (internal oscillator disabled and bypassed – lower power)

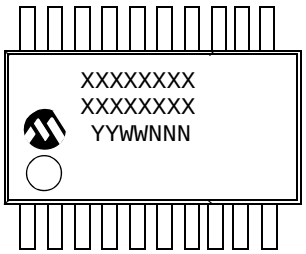
0 = XT mode – A crystal must be placed between OSC1/OSC2 (default)

**NOTES:**

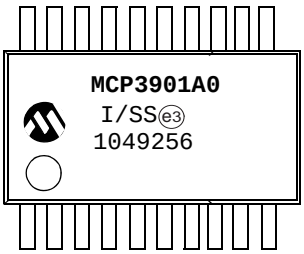
## 8.0 PACKAGING INFORMATION

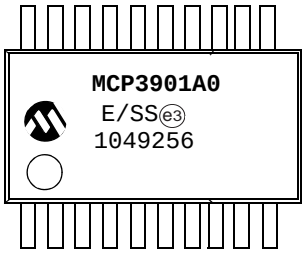
### 8.1 Package Marking Information

20-Lead SSOP (SS)

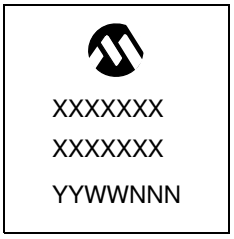



Example:

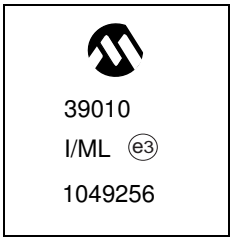


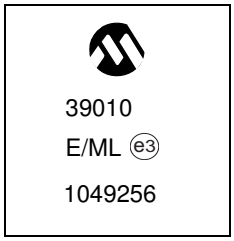




20-Lead QFN




Examples:



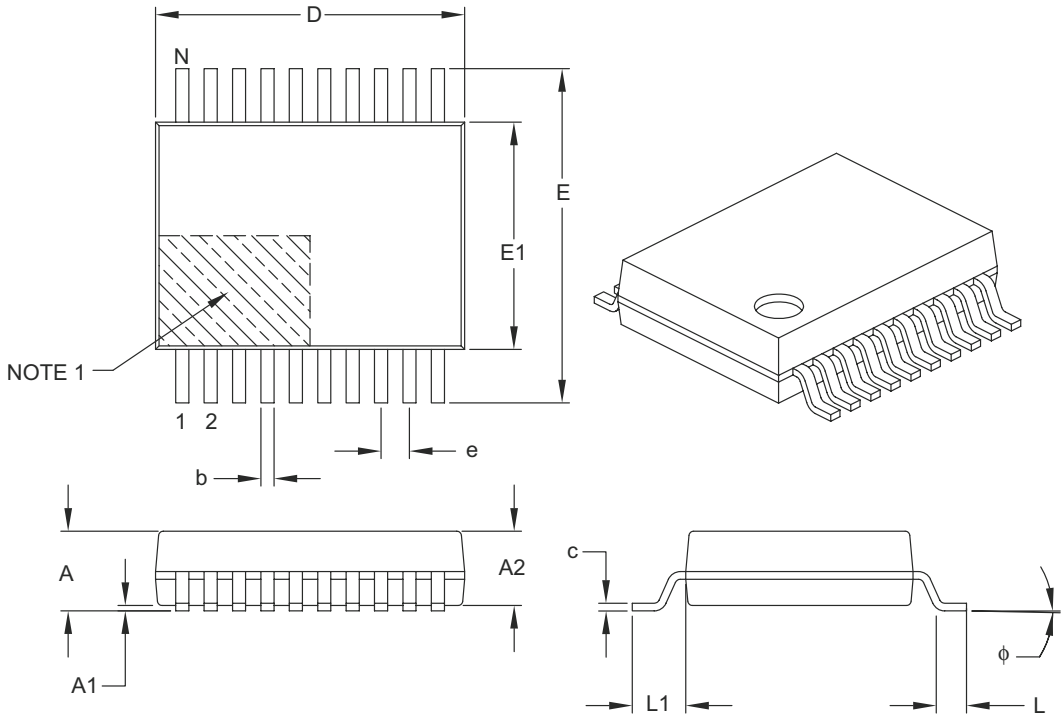




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 20 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 6.90 | 7.20 | 7.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | | 1.25 REF | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | ϕ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

**Notes:**

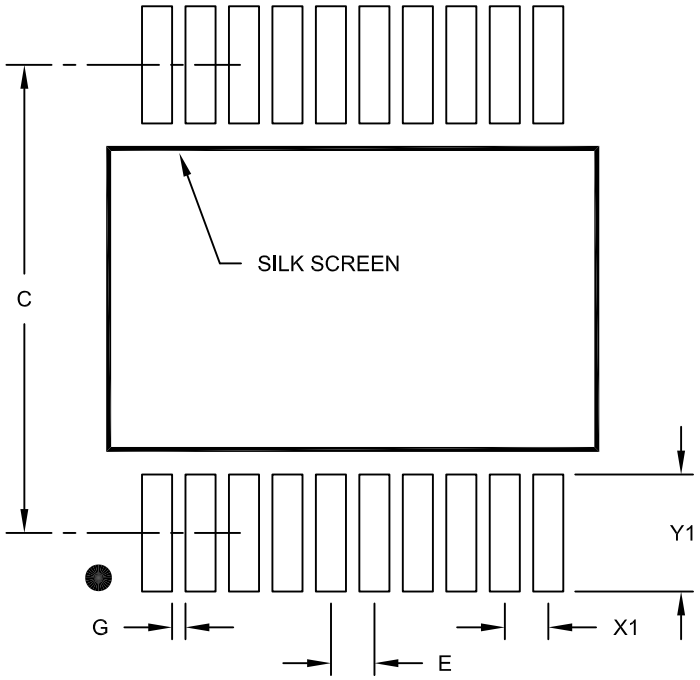
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Contact Pad Spacing | C | | 7.20 | |
| Contact Pad Width (X20) | X1 | | | 0.45 |
| Contact Pad Length (X20) | Y1 | | | 1.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

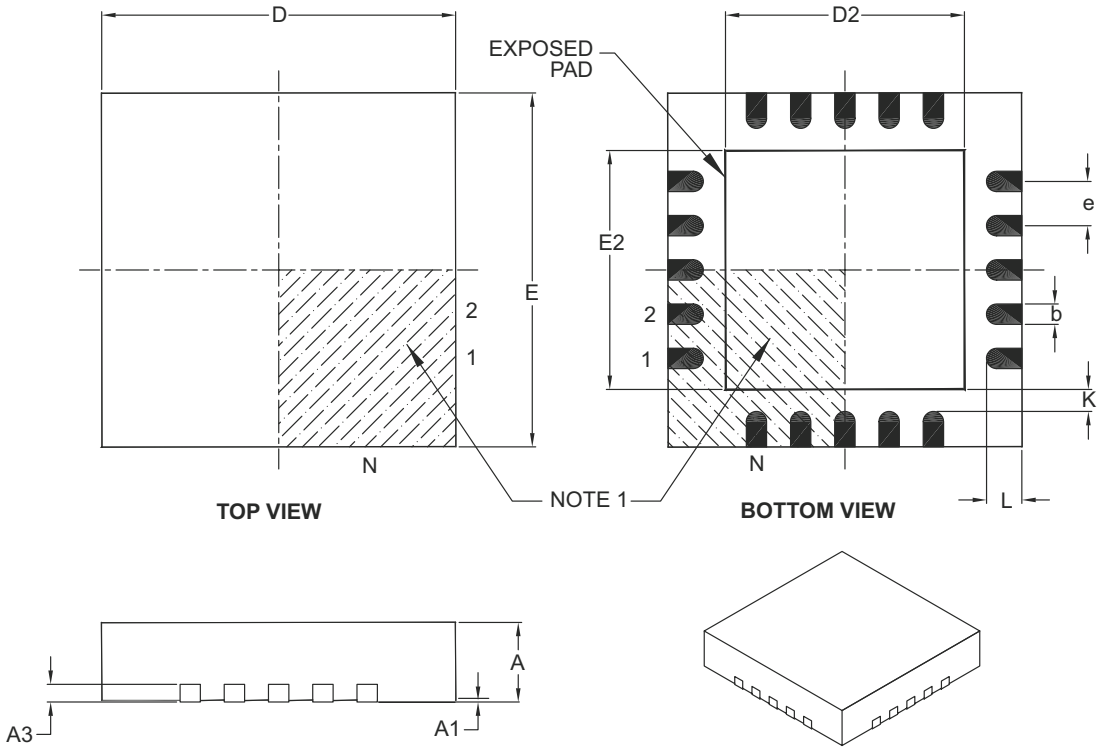
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

## 20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 20 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 4.00 BSC | |
| Exposed Pad Width | E2 | 2.60 | 2.70 | 2.80 |
| Overall Length | D | | 4.00 BSC | |
| Exposed Pad Length | D2 | 2.60 | 2.70 | 2.80 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

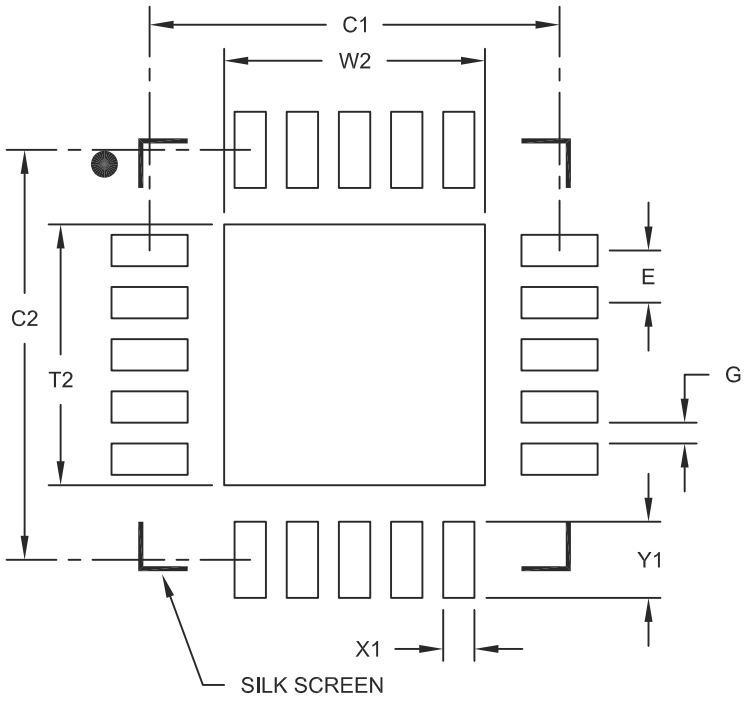
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 2.50 |
| Optional Center Pad Length | T2 | | | 2.50 |
| Contact Pad Spacing | C1 | | 3.93 | |
| Contact Pad Spacing | C2 | | 3.93 | |
| Contact Pad Width | X1 | | | 0.30 |
| Contact Pad Length | Y1 | | | 0.73 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision D (April 2011)

The following is the list of modifications:

1. Added the 20-lead QFN package and related information throughout the document.
2. Added the E Temperature package option.

## Revision C (August 2010)

The following is the list of modifications:

1. Corrected symbols inside the **Functional Block Diagram** figure.
2. Typographical revisions throughout document.

## Revision B (November 2009)

The following is the list of modifications:

1. Removed the QFN package and all references to it.

## Revision A (September 2009)

- Original Release of this Document.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | XX | X | X | /XX |
|---|---|---|---|---|
| Device | Address Options | Tape and Reel | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP3901: | Two-Channel ΔΣ A/D Converter |
| Address Options: | XX | A6 A5 |
| | A0* = | 0 0 |
| | A1 = | 0 1 |
| | A2 = | 1 0 |
| | A3 = | 1 1 |
| | * Default option. Contact Microchip factory for other address options | |
| Tape and Reel: | T = | Tape and Reel |
| Temperature Range: | I = | -40°C to +85°C |
| | E = | -40°C to +125°C |
| Package: | SS = | Plastic Shrink Small Outline (SSOP), 20-lead |
| | ML = | Plastic Quad Flat No-lead (4x4 QFN), 20-lead |

**Examples:**

a) MCP3901A0-I/SS: Two-Channel ΔΣ A/D Converter, SSOP-20 package, Address Option = A0 Industrial Temperature Range

b) MCP3901A0T-I/SS: Tape and Reel, Two-Channel ΔΣ A/D Converter, SSOP-20 package, Address Option = A0 Industrial Temperature Range

c) MCP3901A1-I/SS: Two-Channel ΔΣ A/D Converter, SSOP-20 package, Address Option = A1 Industrial Temperature Range

d) MCP3901A1T-I/SS: Tape and Reel, Two-Channel ΔΣ A/D Converter, SSOP-20 package, Address Option = A1 Industrial Temperature Range

e) MCP3901A0-E/ML: Two-Channel ΔΣ A/D Converter, QFN-20 package, Address Option = A0 Extended Temperature Range.

**NOTES:**

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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Printed on recycled paper.

ISBN: 978-1-61341-078-3

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