MCP6021/1R/2/3/4

Rail-to-Rail Input/Output, 10 MHz Op Amps

Features

- Rail-to-Rail Input/Output
- Wide Bandwidth: 10 MHz (typical)
- Low Noise: 8.7 nV/√Hz, at 10 kHz (typical)
- Low Offset Voltage:
  - Industrial Temperature: ±500 µV (maximum)
  - Extended Temperature: ±250 µV (maximum)
- Mid-Supply V_{REF}: MCP6021 and MCP6023
- Low Supply Current: 1 mA (typical)
- Total Harmonic Distortion:
  - 0.00053% (typical, G = 1 V/V)
- Unity Gain Stable
- Power Supply Range: 2.5V to 5.5V
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

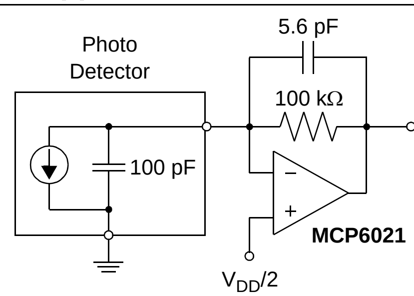
Applications

- Automotive
- Multi-Pole Active Filters
- Audio Processing
- DAC Buffer
- Test Equipment
- Medical Instrumentation

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



Transimpedance Amplifier

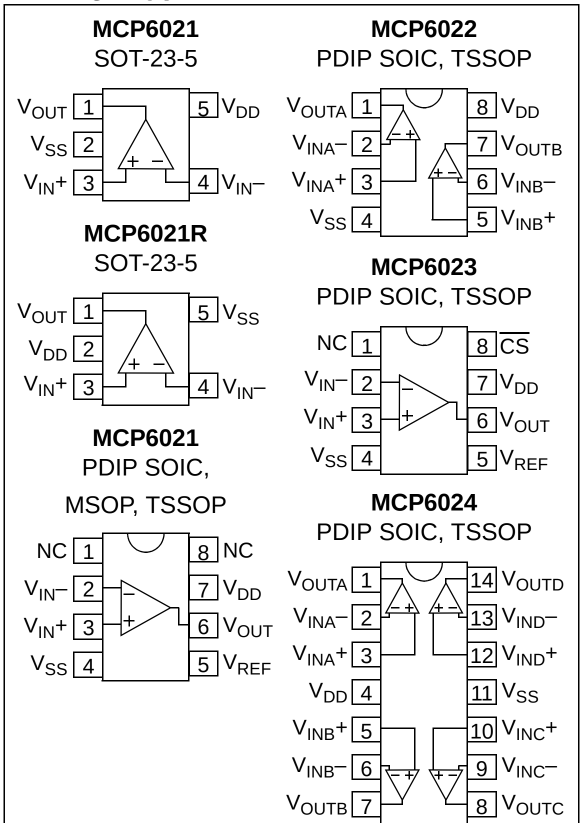
Description

The MCP6021, MCP6021R, MCP6022, MCP6023 and MCP6024 from Microchip Technology Inc. are rail-to-rail input and output op amps with high performance. Key specifications include: wide bandwidth (10 MHz), low noise (8.7 nV/√Hz), low input offset voltage and low distortion (0.00053% THD+N). The MCP6023 also offers a Chip Select pin ($\overline{CS}$) that gives power savings when the part is not in use.

The single MCP6021 and MCP6021R are available in SOT-23-5. The single MCP6021, single MCP6023 and dual MCP6022 are available in 8-lead PDIP, SOIC and TSSOP. The Extended Temperature single MCP6021 is available in 8-lead MSOP. The quad MCP6024 is offered in 14-lead PDIP, SOIC and TSSOP packages.

The MCP6021/1R/2/3/4 family is available in Industrial and Extended temperature ranges. It has a power supply range of 2.5V to 5.5V.

Package Types



NOTES:

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ 7.0V

Current at Analog Input Pins (V_{IN}+, V_{IN}–).....................±2 mA

Analog Inputs (V_{IN}+, V_{IN}–) †† .... V_{SS} – 1.0V to V_{DD} + 1.0V

All Other Inputs and Outputs .... V_{SS} – 0.3V to V_{DD} + 0.3V

Difference Input Voltage .... $|V_{DD} – V_{SS}|$

Output Short Circuit Current ....Continuous

Current at Output and Supply Pins ....±30 mA

Storage Temperature ....–65°C to +150°C

Maximum Junction Temperature (T_J)........................ .+150°C

ESD Protection On All Pins (HBM; MM)............. ≥ 2 kV; 200V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “ Input Voltage and Current Limits”**.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2 and R_L = 10 kΩ to V_{DD}/2.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage:						
Industrial Temperature Parts	V_{OS}	-500	—	+500	µV	V_{CM} = 0V
Extended Temperature Parts	V_{OS}	-250	—	+250	µV	V_{CM} = 0V, V_{DD} = 5.0V
Extended Temperature Parts	V_{OS}	-2.5	—	+2.5	mV	V_{CM} = 0V, V_{DD} = 5.0V T_A = -40°C to +125°C
Input Offset Voltage Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±3.5	—	µV/°C	T_A = -40°C to +125°C
Power Supply Rejection Ratio	PSRR	74	90	—	dB	V_{CM} = 0V
Input Current and Impedance						
Input Bias Current	I_B	—	1	—	pA	
Industrial Temperature Parts	I_B	—	30	150	pA	T_A = +85°C
Extended Temperature Parts	I_B	—	640	5,000	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common-Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common-Mode						
Common-Mode Input Range	V_{CMR}	V_{SS}-0.3	—	V_{DD}+0.3	V	
Common-Mode Rejection Ratio	CMRR	74	90	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 5.3V
	CMRR	70	85	—	dB	V_{DD} = 5V, V_{CM} = 3.0V to 5.3V
	CMRR	74	90	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 3.0V
Voltage Reference (MCP6021 and MCP6023 only)						
V_{REF} Accuracy (V_{REF} – V_{DD}/2)	V_{REF_ACC}	-50	—	+50	mV	
V_{REF} Temperature Drift	$\Delta V_{REF}/\Delta T_A$	—	±100	—	µV/°C	T_A = -40°C to +125°C
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	90	110	—	dB	V_{CM} = 0V, V_{OUT} = V_{SS}+0.3V to V_{DD}-0.3V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS}+15	—	V_{DD}-20	mV	0.5V input overdrive
Output Short Circuit Current	I_{SC}	—	±30	—	mA	V_{DD} = 2.5V
	I_{SC}	—	±22	—	mA	V_{DD} = 5.5V

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Quiescent Current per Amplifier	I_Q	0.5	1.0	1.35	mA	I_O = 0
AC Response						
Gain Bandwidth Product	GBWP	—	10	—	MHz	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Settling Time, 0.2%	t_{SETTLE}	—	250	—	ns	G = +1 V/V, V_{OUT} = 100 mV_{p-p}
Slew Rate	SR	—	7.0	—	V/µs	
Total Harmonic Distortion Plus Noise						
f = 1 kHz, G = +1 V/V	THD+N	—	0.00053	—	%	V_{OUT} = 0.25V to 3.25V (1.75V ± $1.50V_{PK}$), V_{DD} = 5.0V, BW = 22 kHz
f = 1 kHz, G = +1 V/V, R_L = 600Ω	THD+N	—	0.00064	—	%	V_{OUT} = 0.25V to 3.25V (1.75V ± $1.50V_{PK}$), V_{DD} = 5.0V, BW = 22 kHz
f = 1 kHz, G = +1 V/V	THD+N	—	0.0014	—	%	V_{OUT} = $4V_{P-P}$, V_{DD} = 5.0V, BW = 22 kHz
f = 1 kHz, G = +10 V/V	THD+N	—	0.0009	—	%	V_{OUT} = $4V_{P-P}$, V_{DD} = 5.0V, BW = 22 kHz
f = 1 kHz, G = +100 V/V	THD+N	—	0.005	—	%	V_{OUT} = $4V_{P-P}$, V_{DD} = 5.0V, BW = 22 kHz
Noise						
Input Noise Voltage	E_{ni}	—	2.9	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	8.7	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	3	—	fA/√Hz	f = 1 kHz

MCP6023 CHIP SELECT ($\overline{CS}$) ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	-1.0	0.01	—	µA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.01	2.0	µA	$\overline{CS}$ = V_{DD}
GND Current	I_{SS}	-2	-0.05	—	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage	$I_{O(LEAK)}$	—	0.01	—	µA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	2	10	µs	G = +1, V_{IN} = V_{SS}, $\overline{CS}$ = $0.2V_{DD}$ to V_{OUT} = $0.45V_{DD}$ time
$\overline{CS}$ High to Amplifier Output High-Z Time	t_{OFF}	—	0.01	—	µs	G = +1, V_{IN} = V_{SS}, $\overline{CS}$ = $0.8V_{DD}$ to V_{OUT} = $0.05V_{DD}$ time
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5.0V, Internal Switch

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TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Industrial Temperature Range	T_A	-40	—	+85	°C	
Extended Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	124	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The industrial temperature devices operate over this extended temperature range, but with reduced performance. In any case, the internal junction temperature (T_J) must not exceed the absolute maximum specification of 150°C.

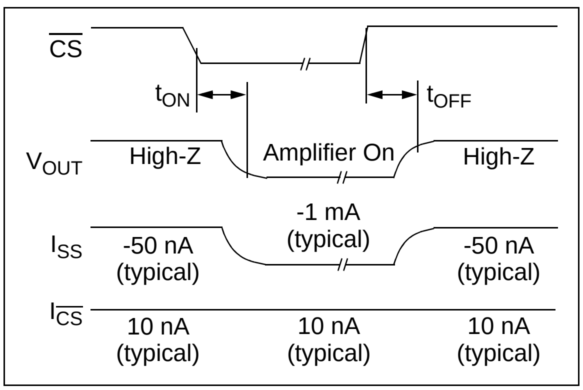

FIGURE 1-1: *Timing diagram for the $\overline{CS}$ pin on the MCP6023.*

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-3. The bypass capacitors are laid out according to the rules discussed in **Section 4.7 "Supply Bypass"**.

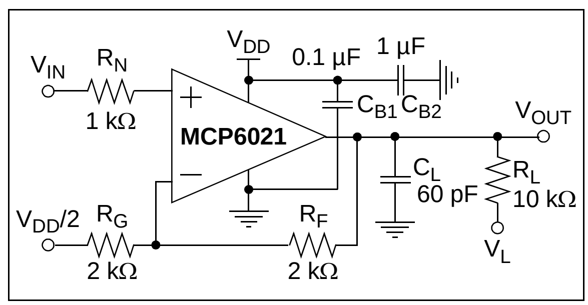

FIGURE 1-2: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

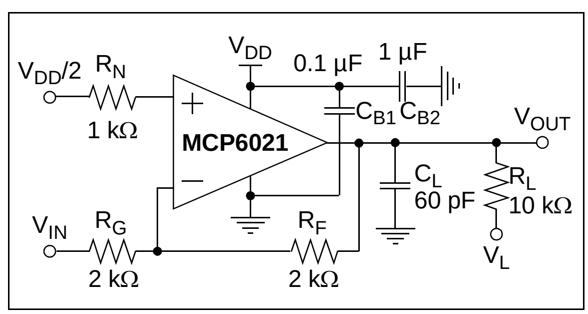

FIGURE 1-3: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

> **Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

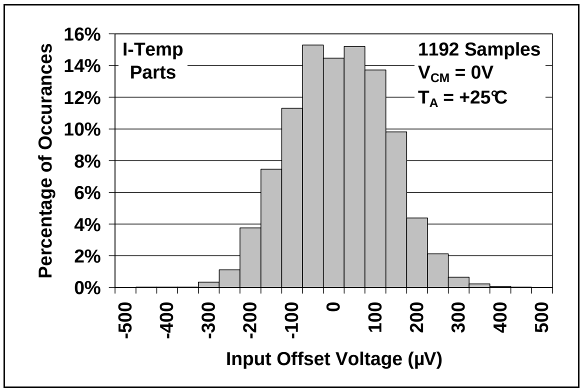

FIGURE 2-1: *Input Offset Voltage, (Industrial Temperature Parts).*

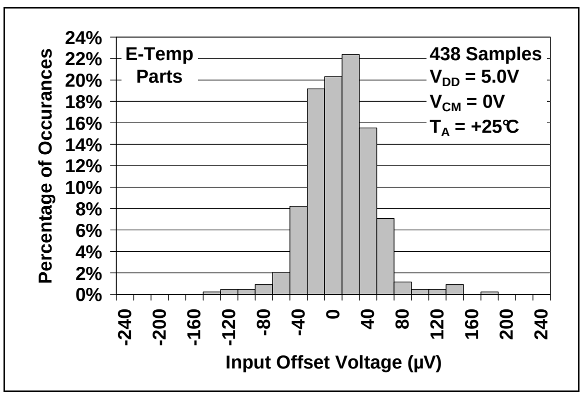

FIGURE 2-2: *Input Offset Voltage, (Extended Temperature Parts).*

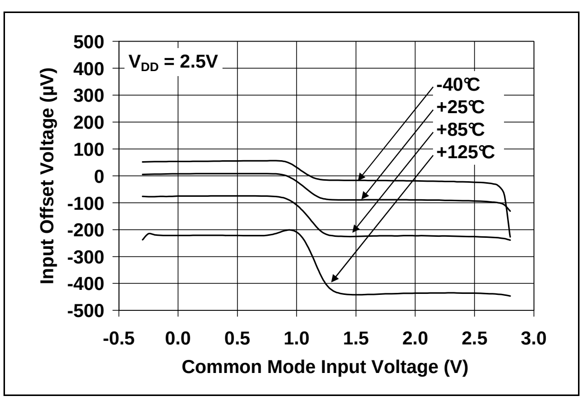

FIGURE 2-3: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 2.5V.*

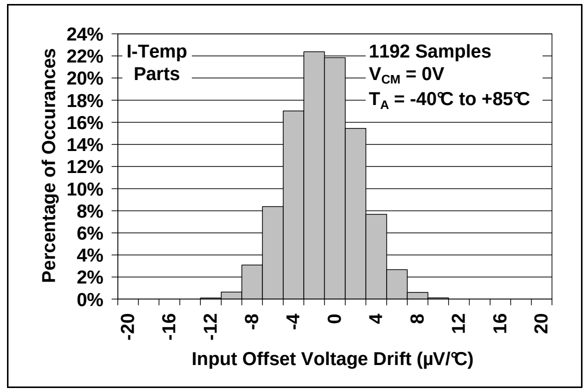

FIGURE 2-4: *Input Offset Voltage Drift, (Industrial Temperature Parts).*

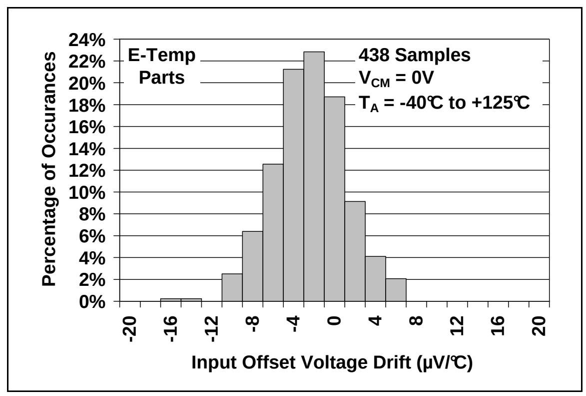

FIGURE 2-5: *Input Offset Voltage Drift, (Extended Temperature Parts).*

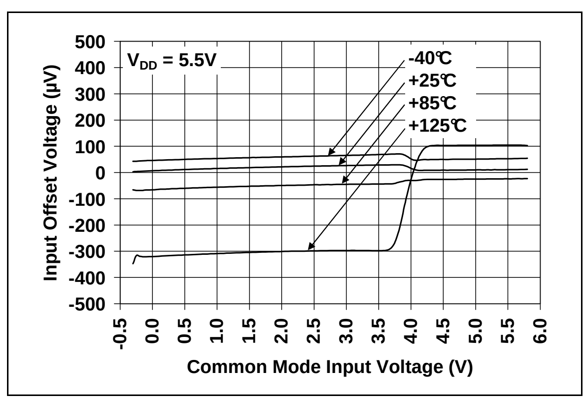

FIGURE 2-6: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

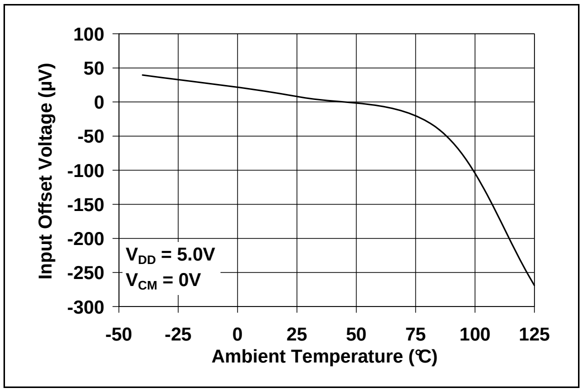

FIGURE 2-7: *Input Offset Voltage vs. Temperature.*

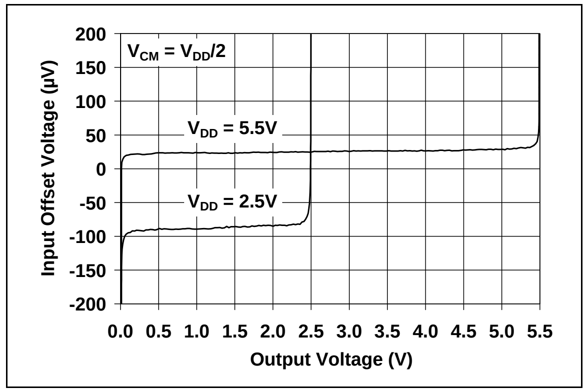

FIGURE 2-10: *Input Offset Voltage vs. Output Voltage.*

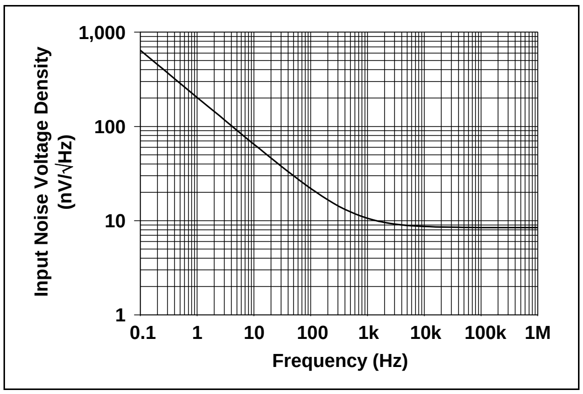

FIGURE 2-8: *Input Noise Voltage Density vs. Frequency.*

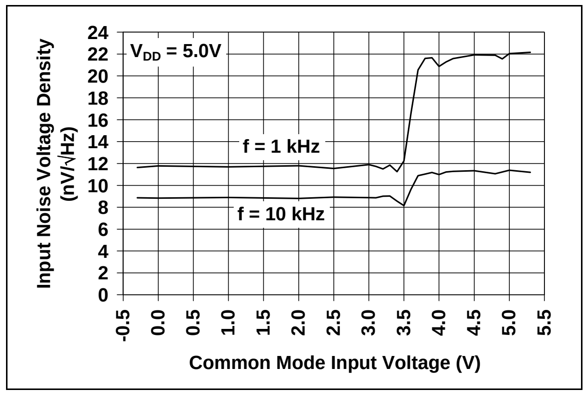

FIGURE 2-11: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

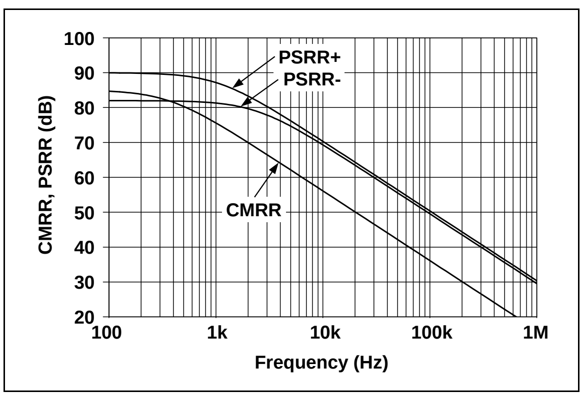

FIGURE 2-9: *CMRR, PSRR vs. Frequency.*

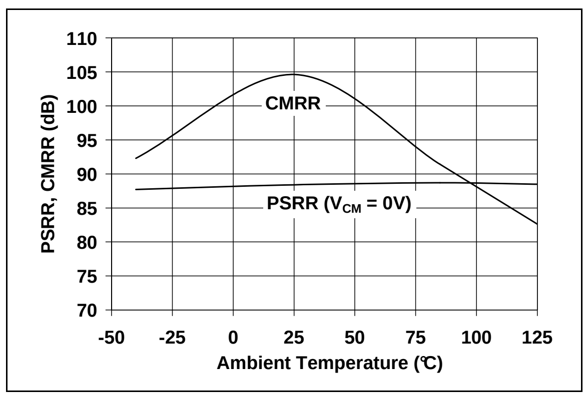

FIGURE 2-12: *CMRR, PSRR vs. Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

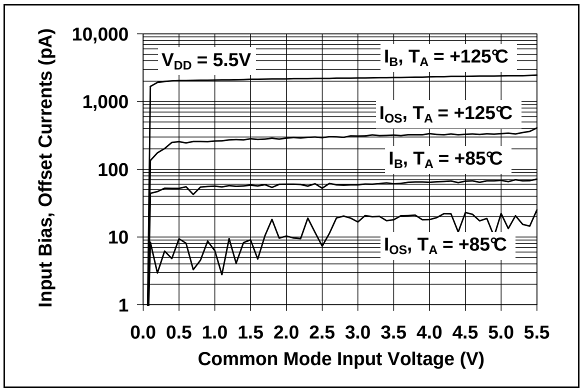

FIGURE 2-13: *Input Bias, Offset Currents vs. Common Mode Input Voltage.*

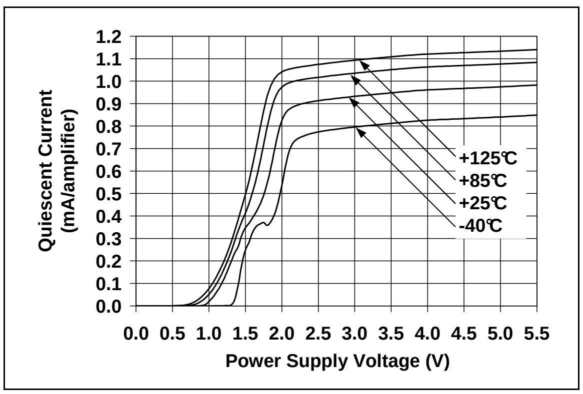

FIGURE 2-14: *Quiescent Current vs. Supply Voltage.*

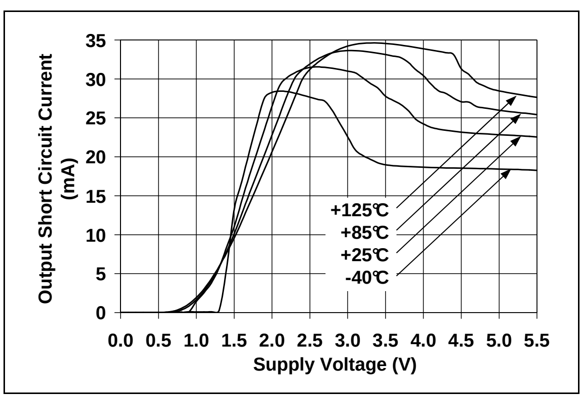

FIGURE 2-15: *Output Short-Circuit Current vs. Supply Voltage.*

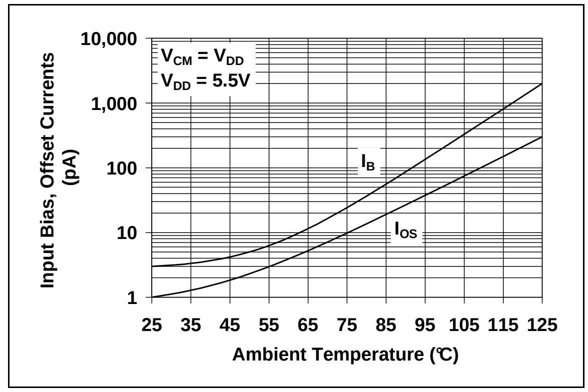

FIGURE 2-16: *Input Bias, Offset Currents vs. Temperature.*

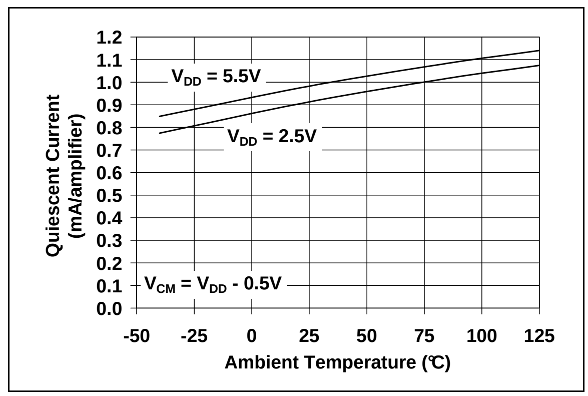

FIGURE 2-17: *Quiescent Current vs. Temperature.*

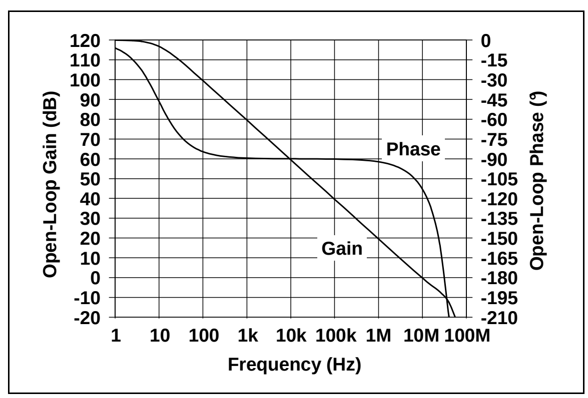

FIGURE 2-18: *Open-Loop Gain, Phase vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

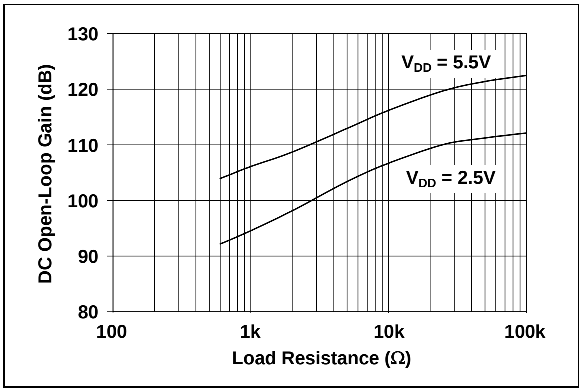

FIGURE 2-19: *DC Open-Loop Gain vs. Load Resistance.*

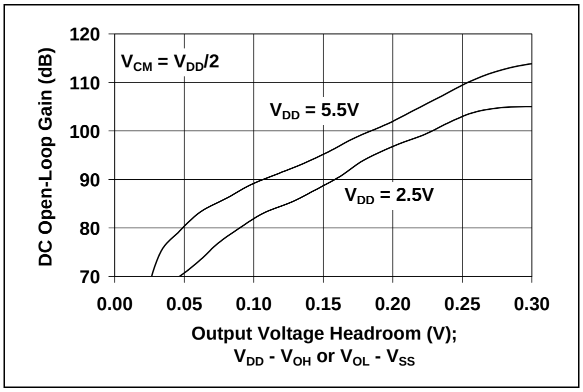

FIGURE 2-20: *Small Signal DC Open-Loop Gain vs. Output Voltage Headroom.*

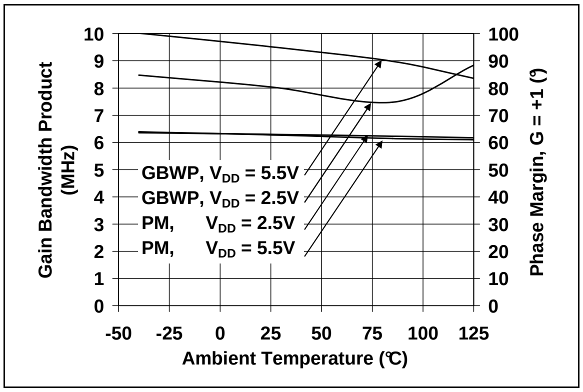

FIGURE 2-21: *Gain Bandwidth Product, Phase Margin vs. Temperature.*

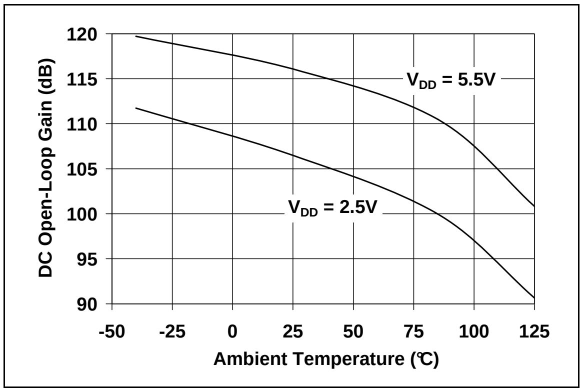

FIGURE 2-22: *DC Open-Loop Gain vs. Temperature.*

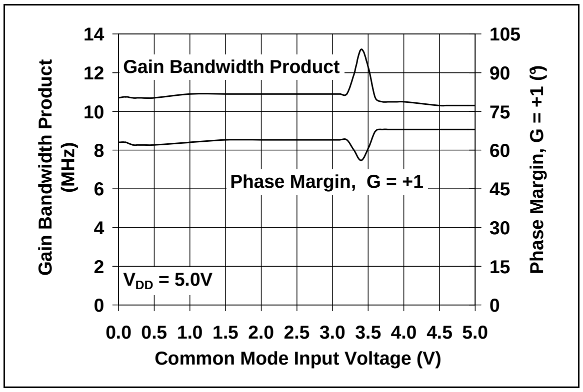

FIGURE 2-23: *Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage.*

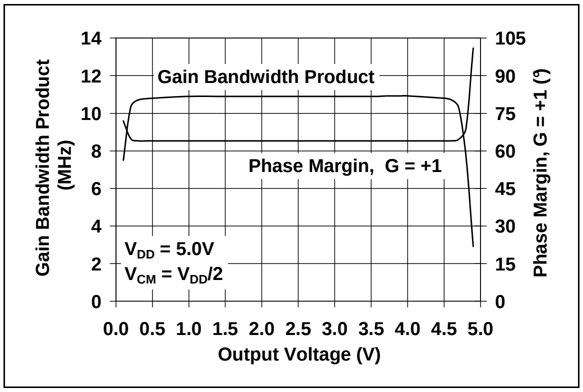

FIGURE 2-24: *Gain Bandwidth Product, Phase Margin vs. Output Voltage.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

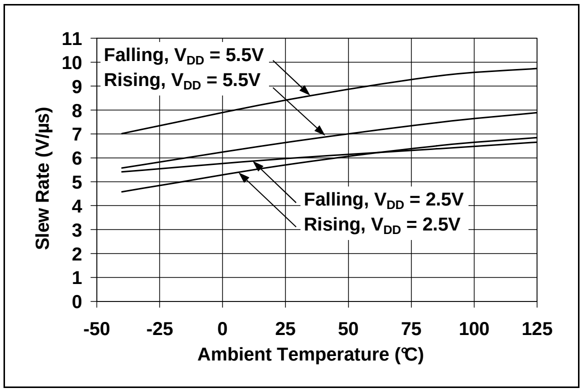

FIGURE 2-25: *Slew Rate vs. Temperature.*

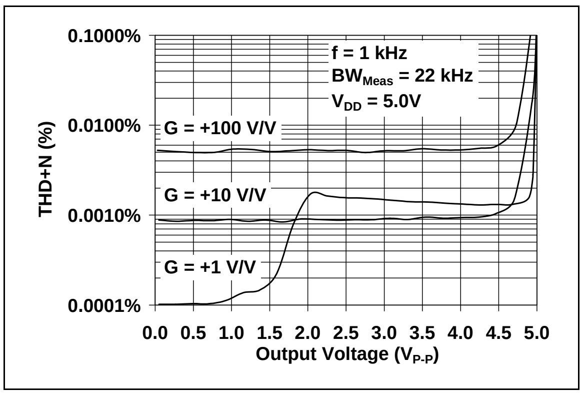

FIGURE 2-26: *Total Harmonic Distortion plus Noise vs. Output Voltage with f = 1 kHz.*

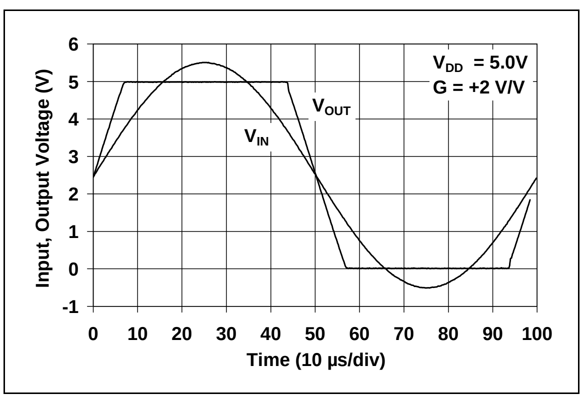

FIGURE 2-27: *The MCP6021/1R/2/3/4 family shows no phase reversal under overdrive.*

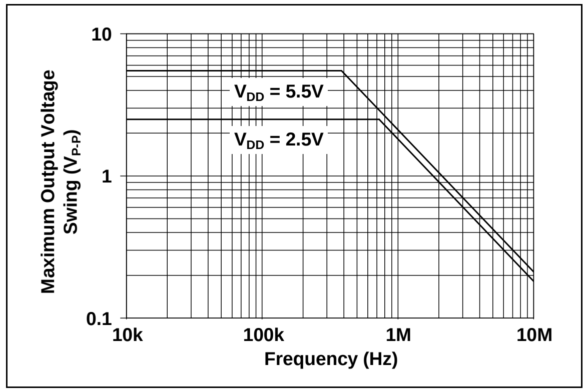

FIGURE 2-28: *Maximum Output Voltage Swing vs. Frequency.*

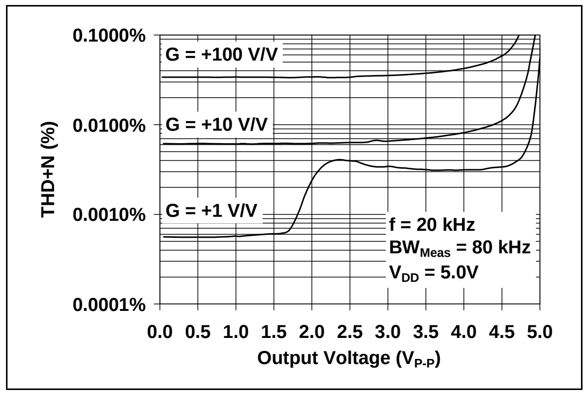

FIGURE 2-29: *Total Harmonic Distortion plus Noise vs. Output Voltage with f = 20 kHz.*

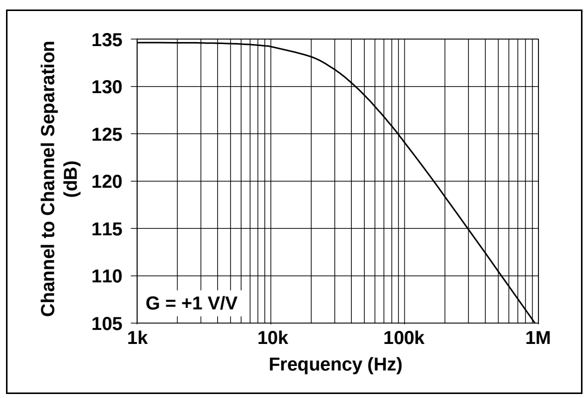

FIGURE 2-30: *Channel-to-Channel Separation vs. Frequency (MCP6022 and MCP6024 only).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

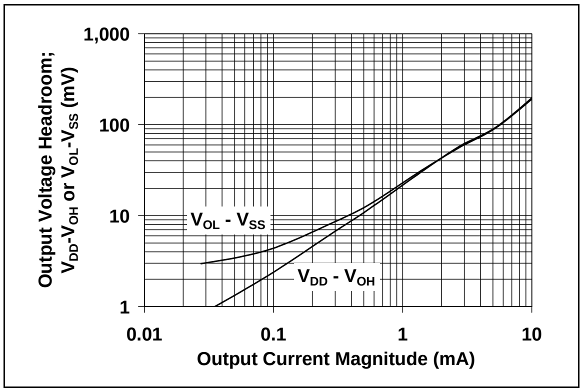

FIGURE 2-31: *Output Voltage Headroom vs. Output Current.*

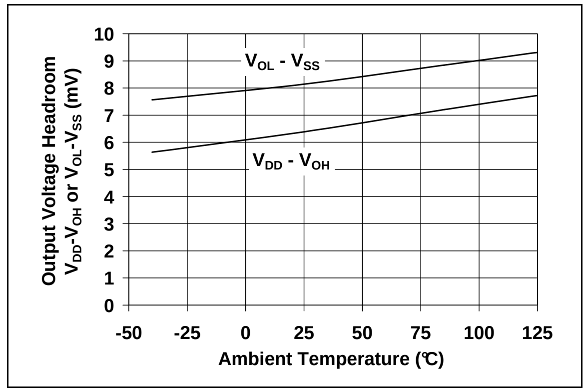

FIGURE 2-34: *Output Voltage Headroom vs. Temperature.*

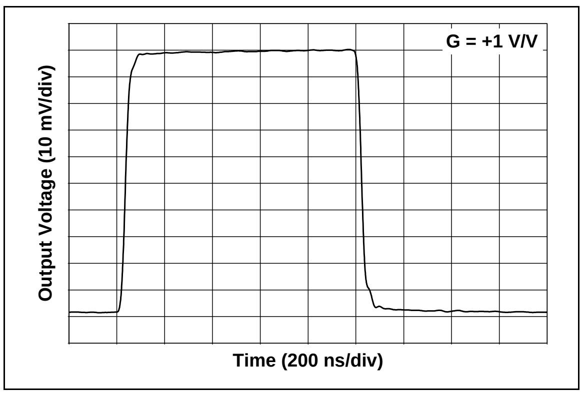

FIGURE 2-32: *Small-Signal Non-inverting Pulse Response.*

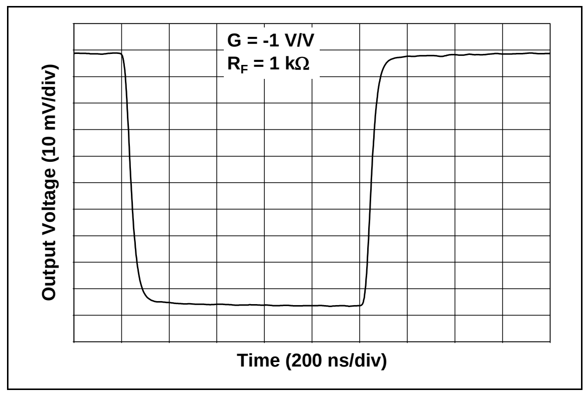

FIGURE 2-35: *Small-Signal Inverting Pulse Response.*

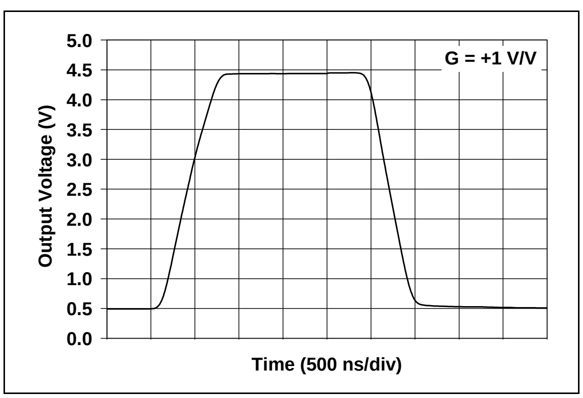

FIGURE 2-33: *Large-Signal Non-inverting Pulse Response.*

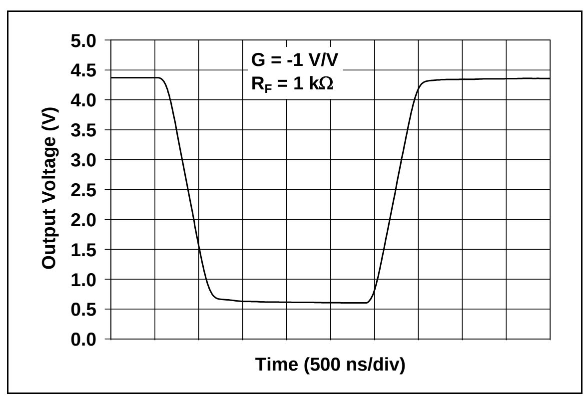

FIGURE 2-36: *Large-Signal Inverting Pulse Response.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

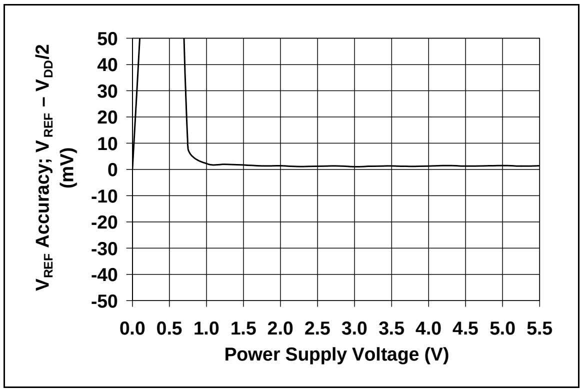

FIGURE 2-37: *V_{REF} Accuracy vs. Supply Voltage (MCP6021 and MCP6023 only).*

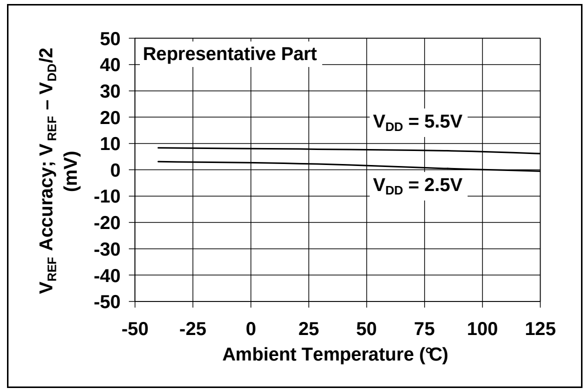

FIGURE 2-40: *V_{REF} Accuracy vs. Temperature (MCP6021 and MCP6023 only).*

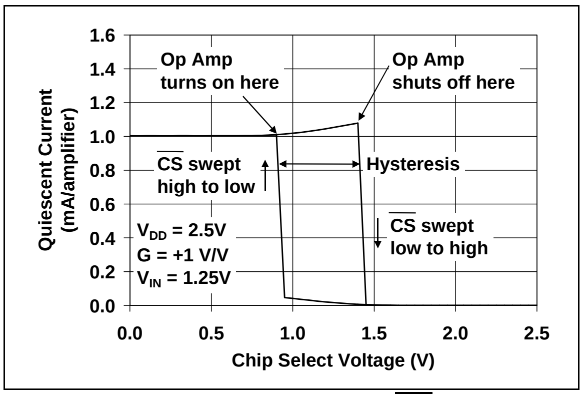

FIGURE 2-38: *Chip Select ($\overline{CS}$) Hysteresis (MCP6023 only) with V_{DD} = 2.5V.*

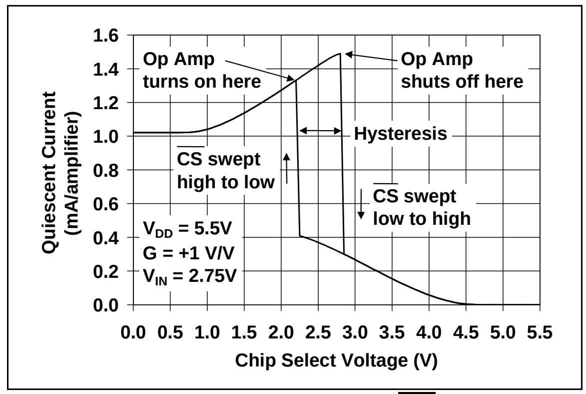

FIGURE 2-41: *Chip Select ($\overline{CS}$) Hysteresis (MCP6023 only) with V_{DD} = 5.5V.*

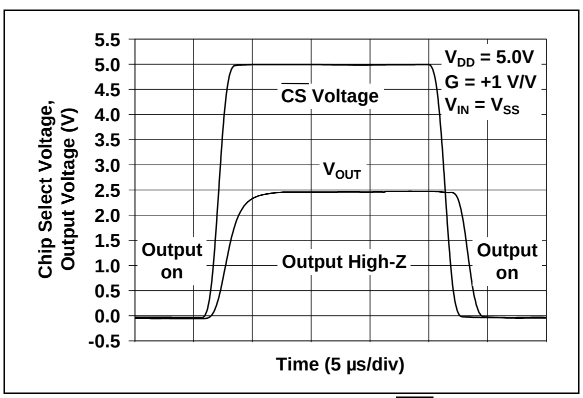

FIGURE 2-39: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time (MCP6023 only).*

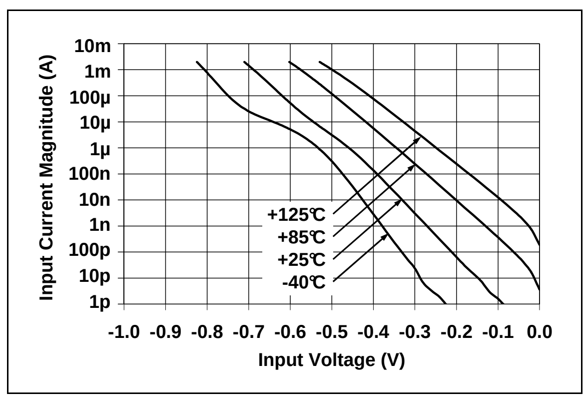

FIGURE 2-42: *Measured Input Current vs. Input Voltage (below V_{SS}).*

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3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6021		MCP6021R	MCP6022	MCP6023	MCP6024	Symbol	Description
PDIP, SOIC, MSOP, TSSOP (Note 1)	SOT-23-5	SOT-23-5 (Note 2)	PDIP, SOIC, TSSOP	PDIP, SOIC, TSSOP	PDIP, SOIC, TSSOP		
6	1	1	1	6	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
2	4	4	2	2	2	$V_{IN}–$, $V_{INA}–$	Inverting Input (op amp A)
3	3	3	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
7	5	2	8	7	4	V_{DD}	Positive Power Supply
—	—	—	5	—	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	—	6	—	6	$V_{INB}–$	Inverting Input (op amp B)
—	—	—	7	—	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	—	9	$V_{INC}–$	Inverting Input (op amp C)
—	—	—	—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
4	2	5	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	—	13	$V_{IND}–$	Inverting Input (op amp D)
—	—	—	—	—	14	V_{OUTD}	Analog Output (op amp D)
5	—	—	—	5	—	V_{REF}	Reference Voltage
—	—	—	—	8	—	$\overline{CS}$	Chip Select
1, 8	—	—	—	1	—	NC	No Internal Connection

Note 1: The MCP6021 in the 8-pin TSSOP package is only available for I-temp (Industrial Temperature) parts.
2: The MCP6021R is only available in the 5-pin SOT-23 package, and for E-temp (Extended Temperature) parts.

3.1 Analog Outputs

The op amp output pins are low-impedance voltage sources.

3.2 Analog Inputs

The op amp non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Reference Voltage ($V_{REF,}$) MCP6021 and MCP6023

Mid-supply reference voltage provided by the single op amps (except in SOT-23-5 package). This is an unbuffered, resistor voltage divider internal to the part.

3.4 Chip Select Digital Input ($\overline{CS}$)

This is a CMOS, Schmitt-triggered input that places the part into a low power mode of operation.

3.5 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 2.5V to 6.0V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a bypass capacitor.

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4.0 APPLICATIONS INFORMATION

The MCP6021/1R/2/3/4 family of operational amplifiers are fabricated on Microchip's state-of-the-art CMOS process. They are unity-gain stable and suitable for a wide range of general-purpose applications.

4.1 Rail-to-Rail Input

4.1.1 PHASE REVERSAL

The MCP6021/1R/2/3/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-42 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

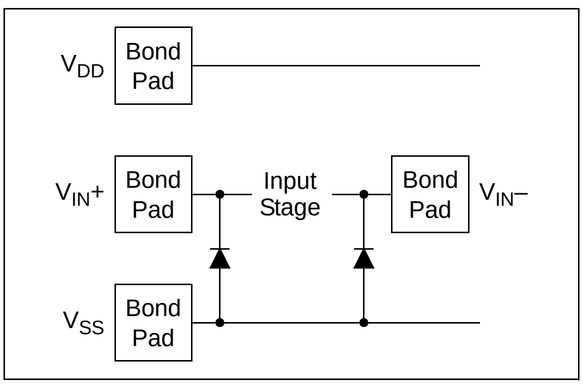

FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the V_{IN}+ and V_{IN}– pins (see **Absolute Maximum Ratings †** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}–) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN}+ and V_{IN}–) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

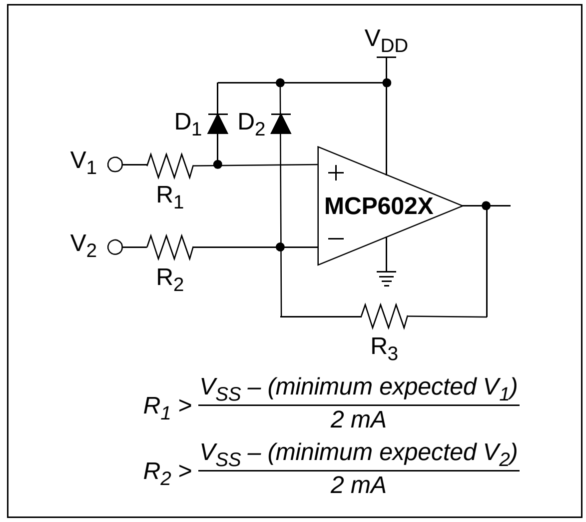

FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of resistors R_1 and R_2. In this case, current through the diodes D_1 and D_2 needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}–) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-42. Applications that are high impedance may need to limit the useable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP6021/1R/2/3/4 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (V_{CM}), while the other operates at high V_{CM}. WIth this topology, the device operates with Vcm up to 0.3V above V_{DD} and 0.3V below V_{SS}.

4.2 Rail-to-Rail Output

The Maximum Output Voltage Swing is the maximum swing possible under a particular output load. According to the specification table, the output can reach within 20 mV of either supply rail when R_L = 10 kΩ. See Figure 2-31 and Figure 2-34 for more information concerning typical performance.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed loop bandwidth is reduced. This produces gain-peaking in the frequency response, with overshoot and ringing in the step response.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

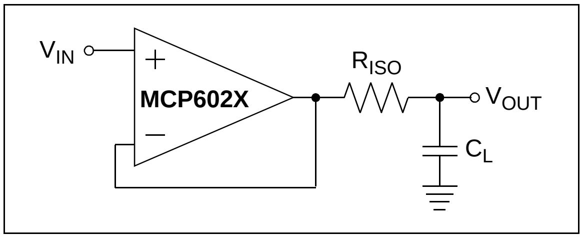

FIGURE 4-3: *Output Resistor R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

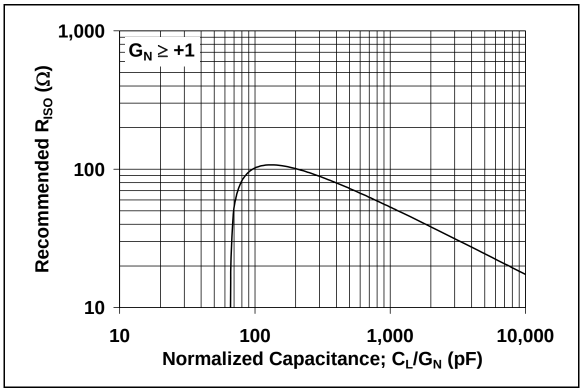

FIGURE 4-4: *Recommended R_{ISO} values for capacitive loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Evaluation on the bench and simulations with the MCP6021/1R/2/3/4 Spice macro model are helpful.

4.4 Gain Peaking

Figure 2-35 and Figure 2-36 use R_F = 1 kΩ to avoid (frequency response) gain peaking and (step response) overshoot. The capacitance to ground at the inverting input (C_G) is the op amp's common mode input capacitance plus board parasitic capacitance. C_G is in parallel with R_G, which causes an increase in gain at high frequencies for non-inverting gains greater than 1 V/V (unity gain). C_G also reduces the phase margin of the feedback loop for both non-inverting and inverting gains.

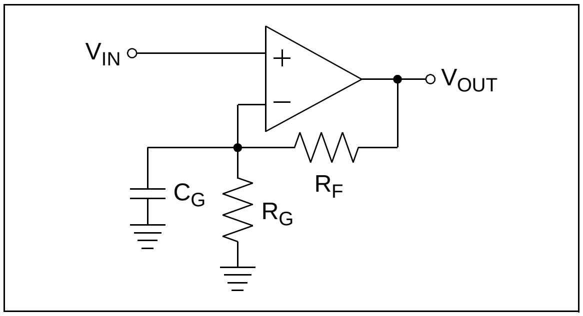

FIGURE 4-5: *Non-inverting Gain Circuit with Parasitic Capacitance.*

The largest value of R_F in Figure 4-5 that should be used is a function of noise gain (see G_N in **Section 4.3 "Capacitive Loads"**) and C_G. Figure 4-6 shows results for various conditions. Other compensation techniques may be used, but they tend to be more complicated to the design.

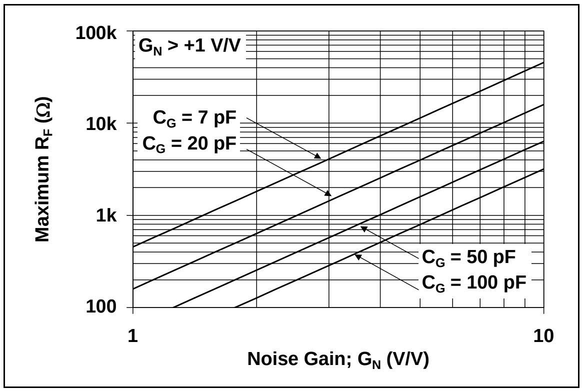

FIGURE 4-6: *Non-inverting gain circuit with parasitic capacitance.*

4.5 MCP6023 Chip Select ($\overline{CS}$)

The MCP6023 is a single amplifier with chip select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to 10 nA (typical) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. The $\overline{CS}$ pin has an internal 5 MΩ (typical) pulldown resistor connected to V_{SS}, so it will go low if the $\overline{CS}$ pin is left floating. Figure 1-1 and Figure 2-39 show the output voltage and supply current response to a $\overline{CS}$ pulse.

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4.6 MCP6021 and MCP6023 Reference Voltage

The single op amps (MCP6021 and MCP6023), not in the SOT-23-5 package, have an internal mid-supply reference voltage connected to the V_{REF} pin (see Figure 4-7). The MCP6021 has $\overline{CS}$ internally tied to V_{SS}, which always keeps the op amp on and always provides a mid-supply reference. With the MCP6023, taking the $\overline{CS}$ pin high conserves power by shutting down both the op amp and the V_{REF} circuitry. Taking the $\overline{CS}$ pin low turns on the op amp and V_{REF} circuitry.

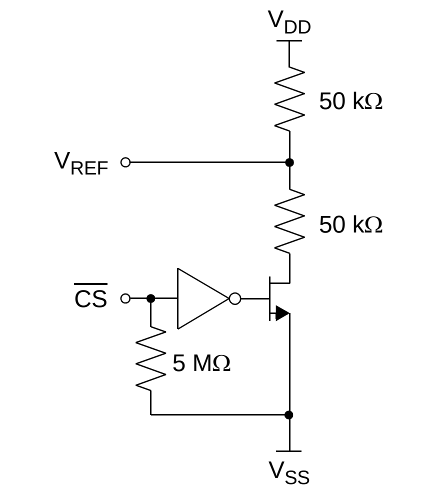


FIGURE 4-7: *Simplified internal V_{REF} circuit (MCP6021 and MCP6023 only).*

See Figure 4-8 for a non-inverting gain circuit using the internal mid-supply reference. The DC-blocking capacitor (C_B) also reduces noise by coupling the op amp input to the source.

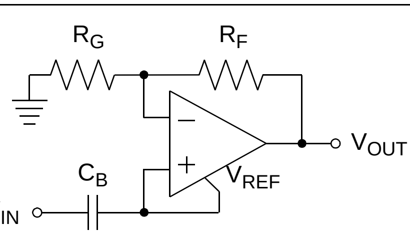


FIGURE 4-8: *Non-inverting gain circuit using V_{REF} (MCP6021 and MCP6023 only).*

To use the internal mid-supply reference for an inverting gain circuit, connect the V_{REF} pin to the non-inverting input, as shown in Figure 4-9. The capacitor C_B helps reduce power supply noise on the output.

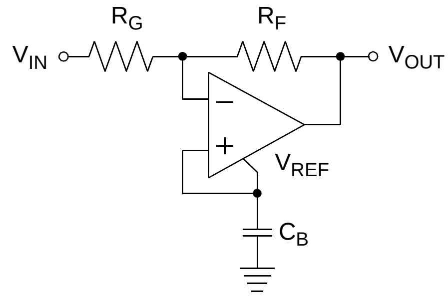


FIGURE 4-9: *Inverting gain circuit using V_{REF} (MCP6021 and MCP6023 only).*

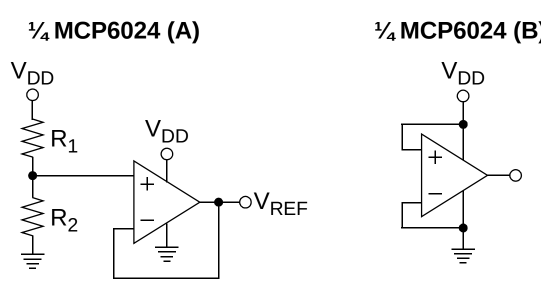
If you don't need the mid-supply reference, leave the V_{REF} pin open.

4.7 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good, high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.8 Unused Op Amps

An unused op amp in a quad package (MCP6024) should be configured as shown in Figure 4-10. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.



$$V_{REF} = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

FIGURE 4-10: *Unused Op Amps.*

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4.9 PCB Surface Leakage

In applications where low input bias current is critical, PCB (printed circuit board) surface-leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6021/1R/2/3/4 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. Figure 4-11 shows an example of this type of layout.

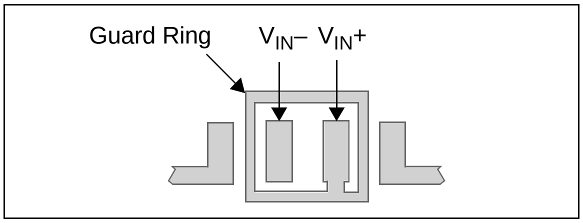

FIGURE 4-11: *Example Guard Ring Layout.*

1. Non-inverting Gain and Unity-Gain Buffer.
    a) Connect the guard ring to the inverting input pin (V_{IN}–); this biases the guard ring to the common mode input voltage.
    b) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
2. Inverting (Figure 4-11) and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors).
    a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp's input (e.g., $V_{DD}/2$ or ground).
    b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.10 High Speed PCB Layout

Due to their speed capabilities, a little extra care in the PCB (Printed Circuit Board) layout can make a significant difference in the performance of these op amps. Good PC board layout techniques will help you achieve the performance shown in **Section 1.0 "Electrical Characteristics"** and **Section 2.0 "Typical Performance Curves"**, while also helping you minimize EMC (Electro-Magnetic Compatibility) issues.

Use a solid ground plane and connect the bypass local capacitor(s) to this plane with minimal length traces. This cuts down inductive and capacitive crosstalk.

Separate digital from analog, low speed from high speed and low power from high power. This will reduce interference.

Keep sensitive traces short and straight. Separating them from interfering components and traces. This is especially important for high-frequency (low rise-time) signals.

Sometimes it helps to place guard traces next to victim traces. They should be on both sides of the victim trace, and as close as possible. Connect the guard trace to ground plane at both ends, and in the middle for long traces.

Use coax cables (or low inductance wiring) to route signal and power to and from the PCB.

4.11 Typical Applications

4.11.1 A/D CONVERTER DRIVER AND ANTI-ALIASING FILTER

Figure 4-12 shows a third-order Butterworth filter that can be used as an A/D converter driver. It has a bandwidth of 20 kHz and a reasonable step response. It will work well for conversion rates of 80 ksps and greater (it has 29 dB attenuation at 60 kHz).

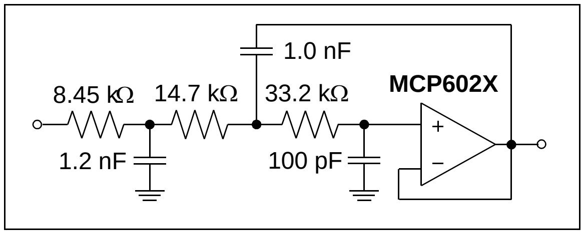

FIGURE 4-12: *A/D Converter Driver and Anti-aliasing Filter with a 20 kHz Cutoff Frequency.*

This filter can easily be adjusted to another bandwidth by multiplying all capacitors by the same factor. Alternatively, the resistors can all be scaled by another common factor to adjust the bandwidth.

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4.11.2 OPTICAL DETECTOR AMPLIFIER

Figure 4-13 shows the MCP6021 op amp used as a transimpedance amplifier in a photo detector circuit. The photo detector looks like a capacitive current source, so the 100 kΩ resistor gains the input signal to a reasonable level. The 5.6 pF capacitor stabilizes this circuit and produces a flat frequency response with a bandwidth of 370 kHz.

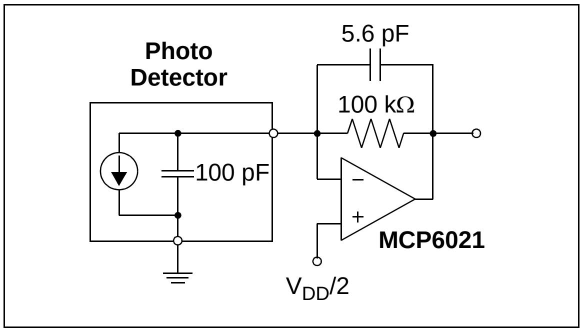

FIGURE 4-13: *Transimpedance Amplifier for an Optical Detector.*

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NOTES:

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5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6021/1R/2/3/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model available for the MCP6021/1R/2/3/4 op amps is on Microchip's web site at www.microchip.com. This model is intended as an initial design tool that works well in the op amp's linear region of operation at room temperature. Within the macro model file is information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX AmplifierEvaluation Board 1
- MCP6XXX AmplifierEvaluation Board 2
- MCP6XXX AmplifierEvaluation Board 3
- MCP6XXX AmplifierEvaluation Board 4
- Active Filter Demo Board Kit
- *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board,* P/N: SOIC8EV
- *14-Pin SOIC/TSSOP/DIP Evaluation Board,* P/N: SOIC14EV

5.6 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177:** *"Op Amp Precision Design: DC Errors"*, DS01177
- **AN1228:** "Op Amp Precision Design: Random Noise", DS01228

These application notes and others are listed in the design guide:

"Signal Chain Design Guide", DS21825

NOTES:

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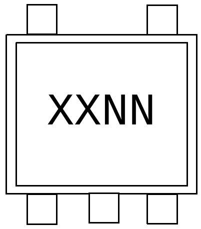
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

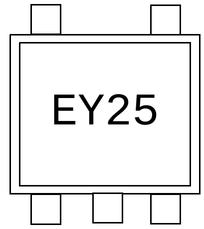
5-Lead SOT-23 (**MCP6021/MCP6021R**)



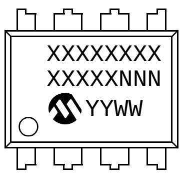
Device	E-Temp Code
MCP6021	EYNN
MCP6021R	EZNN

Note: Applies to 5-Lead SOT-23

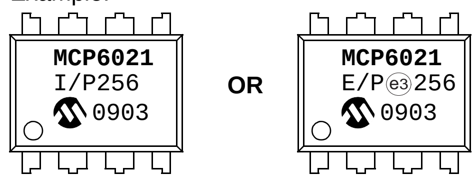
Example: (E-temp)



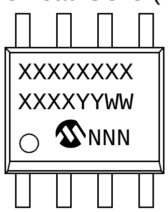
8-Lead PDIP (300 mil)



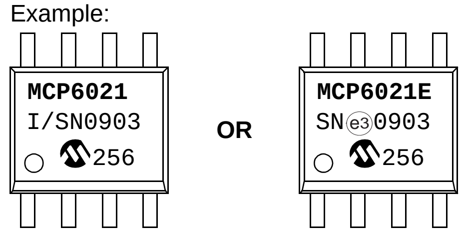
Example:



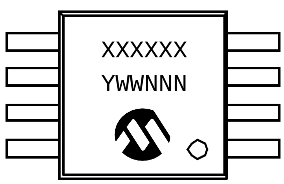
8-Lead SOIC (150 mil)



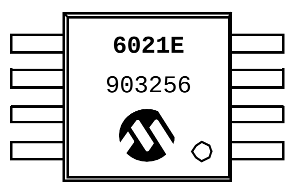
Example:



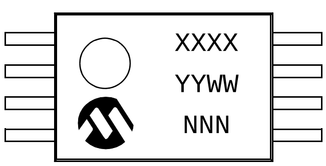
8-Lead MSOP



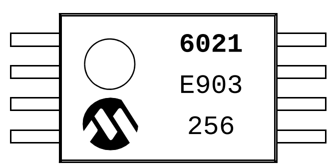
Example:



8-Lead TSSOP



Example:



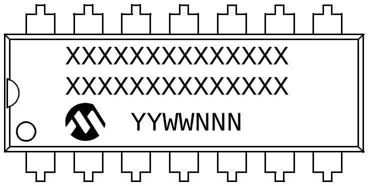
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

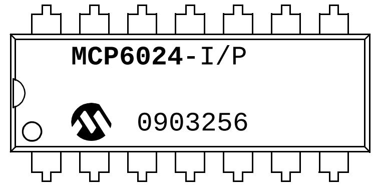
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

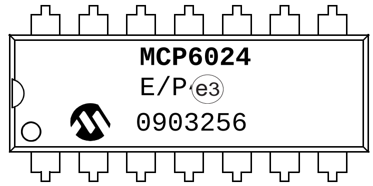
14-Lead PDIP (300 mil) **(MCP6024)**



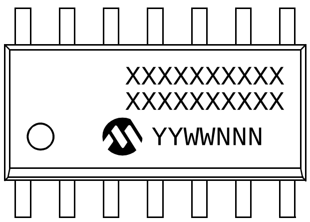
Example:



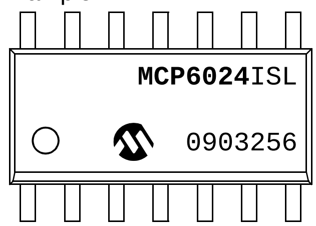
OR



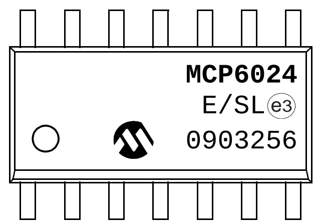
14-Lead SOIC (150 mil) **(MCP6024)**



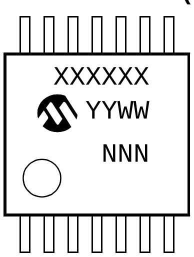
Example:



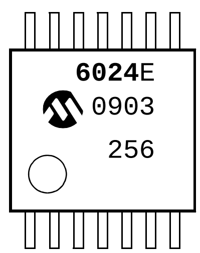
OR



14-Lead TSSOP **(MCP6024)**



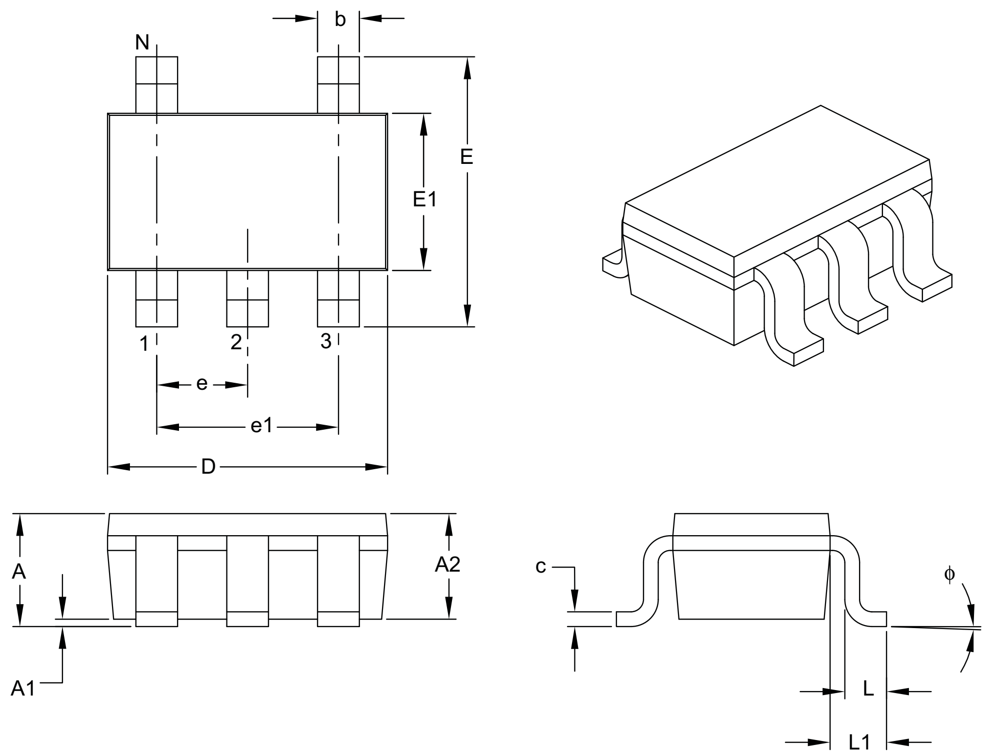
Example:



© 2009 Microchip Technology Inc.

[illegible] Lead Plastic Small Outline Transistor [illegible] OT [illegible] [SOT [illegible]]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http [illegible] www microchip com packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	[illegible]		
Lead Pitch	e	[illegible] BSC		
Outside Lead Pitch	e[illegible]	[illegible] BSC		
Overall Height	A	[illegible]	–	[illegible]
Molded Package Thickness	A[illegible]	[illegible]	–	[illegible]
Standoff	A[illegible]	[illegible]	–	[illegible]
Overall Width	E	[illegible]	–	[illegible]
Molded Package Width	E[illegible]	[illegible]	–	[illegible]
Overall Length	D	[illegible]	–	[illegible]
Foot Length	L	[illegible]	–	[illegible]
Footprint	L[illegible]	[illegible]	–	[illegible]
Foot Angle	ϕ	[illegible]°	–	[illegible]°
Lead Thickness	c	[illegible]	–	[illegible]
Lead Width	b	[illegible]	–	[illegible]

Notes:

[illegible] Dimensions D and E [illegible] do not include mold flash or protrusions. Mold flash or protrusions shall not exceed [illegible] mm per side.

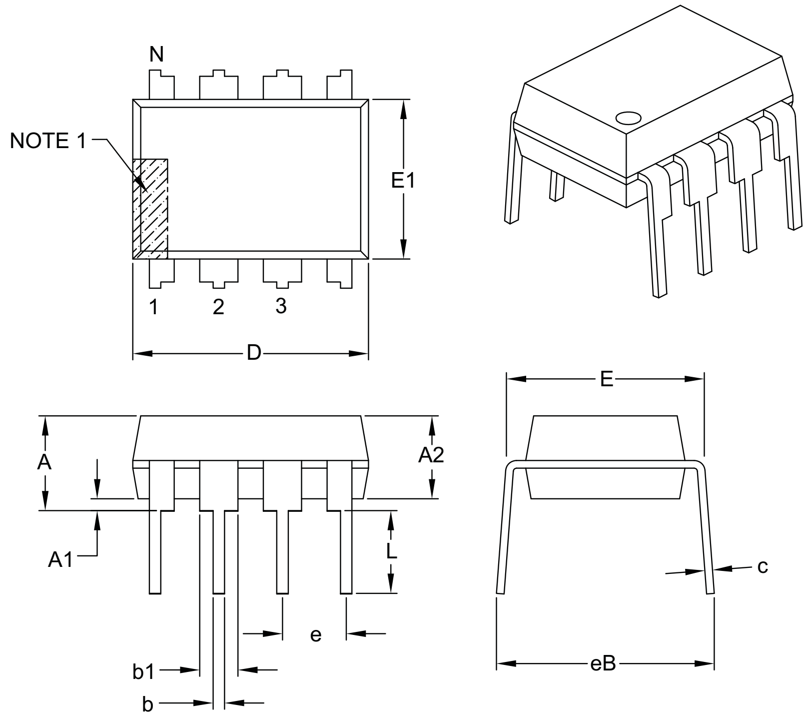
[illegible] Dimensioning and tolerancing per ASME Y [illegible] M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C[illegible]B

[illegible]-Lead Plastic Dual In-Line [illegible]P[illegible] – [illegible] mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	[illegible]		
Pitch	e	[illegible] BSC		
Top to Seating Plane	A	–	–	[illegible]
Molded Package Thickness	A[illegible]	[illegible]	[illegible]	[illegible]
Base to Seating Plane	A[illegible]	[illegible]	–	–
Shoulder to Shoulder Width	E	[illegible]	[illegible]	[illegible]
Molded Package Width	E[illegible]	[illegible]	[illegible]	[illegible]
Overall Length	D	[illegible]	[illegible]	[illegible]
Tip to Seating Plane	L	[illegible]	[illegible]	[illegible]
Lead Thickness	c	[illegible]	[illegible]	[illegible]
Upper Lead Width	b[illegible]	[illegible]	[illegible]	[illegible]
Lower Lead Width	b	[illegible]	[illegible]	[illegible]
Overall Row Spacing §	eB	–	–	[illegible]

Notes:

[illegible] Pin [illegible] visual index feature may vary, but must be located with the hatched area.

[illegible] § Significant Characteristic.

[illegible] Dimensions D and E[illegible] do not include mold flash or protrusions. Mold flash or protrusions shall not exceed [illegible] per side.

[illegible] Dimensioning and tolerancing per ASME Y[illegible]M.

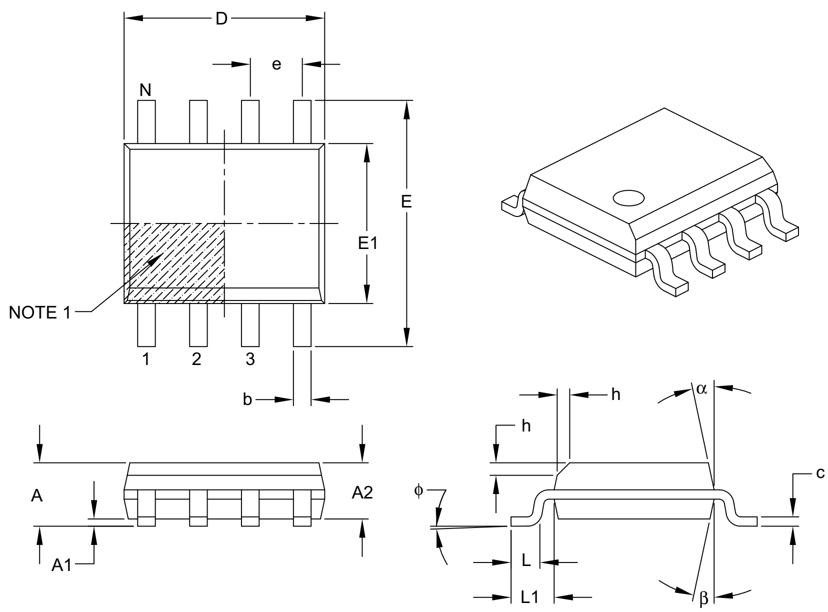
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C[illegible]B

© 2009 Microchip Technology Inc.

[illegible]Lead Plastic Small Outline [illegible]SN[illegible] – Narrow[illegible]mm Body [SOIC]

Note[illegible]	For the most current package drawings[illegible] please see the Microchip Packaging Specification located at[illegible] http[illegible]www[illegible]microchip[illegible]com[illegible]packaging



		Units	MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		[illegible]	
Pitch	e		[illegible] BSC	
Overall Height	A	–	–	[illegible]
Molded Package Thickness	A[illegible]	[illegible]	–	–
Standoff[illegible] §	A[illegible]	[illegible]	–	[illegible]
Overall Width	E		[illegible] BSC	
Molded Package Width	E[illegible]		[illegible] BSC	
Overall Length	D		[illegible] BSC	
Chamfer [illegible]optional[illegible]	h	[illegible]	–	[illegible]
Foot Length	L	[illegible]	–	[illegible]
Footprint	L[illegible]		[illegible] REF	
Foot Angle	ϕ	[illegible]°	–	[illegible]°
Lead Thickness	c	[illegible]	–	[illegible]
Lead Width	b	[illegible]	–	[illegible]
Mold Draft Angle Top	α	[illegible]°	–	[illegible]°
Mold Draft Angle Bottom	β	[illegible]°	–	[illegible]°

Notes[illegible]

[illegible] Pin [illegible] visual index feature may vary[illegible] but must be located within the hatched area[illegible]

[illegible] § Significant Characteristic[illegible]

[illegible] Dimensions D and E[illegible] do not include mold flash or protrusions[illegible] Mold flash or protrusions shall not exceed [illegible] mm per side[illegible]

[illegible] Dimensioning and tolerancing per ASME Y[illegible]M[illegible]

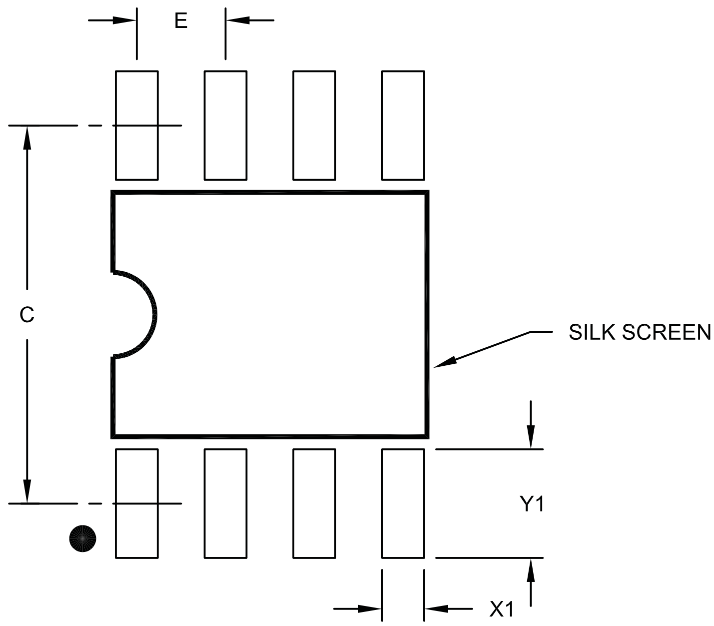
BSC[illegible] Basic Dimension[illegible] Theoretically exact value shown without tolerances[illegible]

REF[illegible] Reference Dimension[illegible] usually without tolerance[illegible] for information purposes only[illegible]

Microchip Technology Drawing C[illegible]B

Lead Plastic Small Outline SN – Narrow mm Body [SOIC]

Note	For the most current package drawings please see the Microchip Packaging Specification located at http www microchip com packaging



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E		1.27 BSC		
Contact Pad Spacing	C			5.40	
Contact Pad Width (X8)	X1				0.60
Contact Pad Length (X8)	Y1				1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

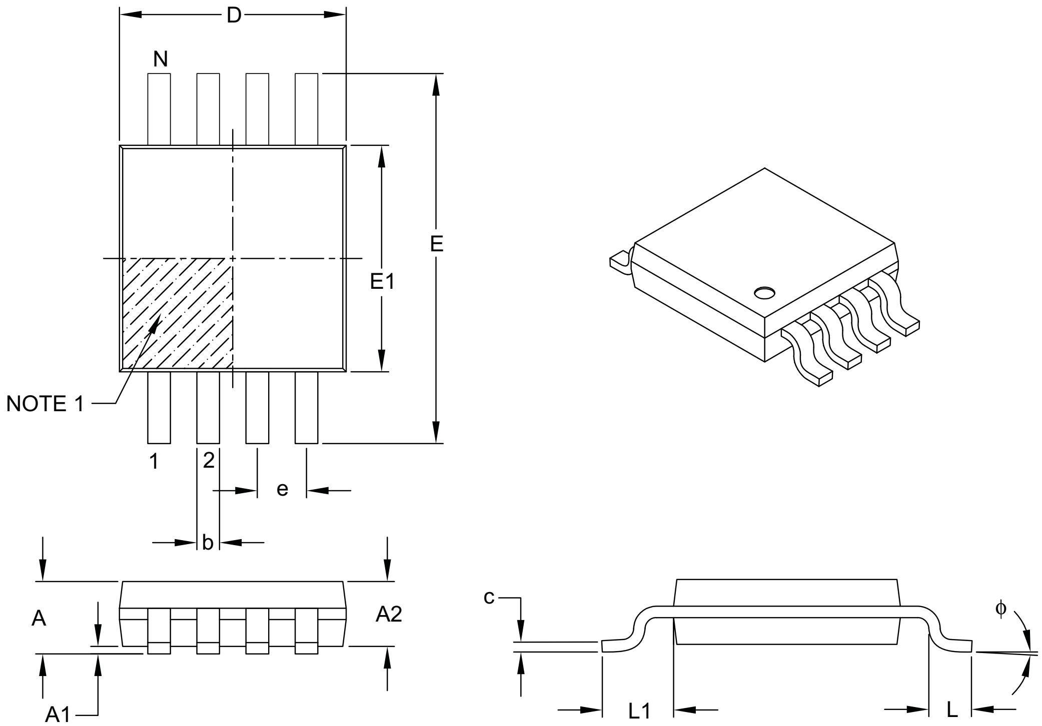
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

© 2009 Microchip Technology Inc.

[illegible] Lead Plastic Micro Small Outline Package [illegible] MS [illegible] [MSOP]

Note	For the most current package drawings please see the Microchip Packaging Specification located at http [illegible] www microchip com packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	[illegible]		
Pitch	e	[illegible] BSC		
Overall Height	A	–	–	[illegible]
Molded Package Thickness	A[illegible]	[illegible]	[illegible]	[illegible]
Standoff	A[illegible]	[illegible]	–	[illegible]
Overall Width	E	[illegible] BSC		
Molded Package Width	E[illegible]	[illegible] BSC		
Overall Length	D	[illegible] BSC		
Foot Length	L	[illegible]	[illegible]	[illegible]
Footprint	L[illegible]	[illegible] REF		
Foot Angle	ϕ	[illegible]°	–	[illegible]°
Lead Thickness	c	[illegible]	–	[illegible]
Lead Width	b	[illegible]	–	[illegible]

Notes

[illegible] Pin [illegible] visual index feature may vary but must be located within the hatched area

[illegible] Dimensions D and E [illegible] do not include mold flash or protrusions Mold flash or protrusions shall not exceed [illegible] mm per side

[illegible] Dimensioning and tolerancing per ASME Y [illegible] M

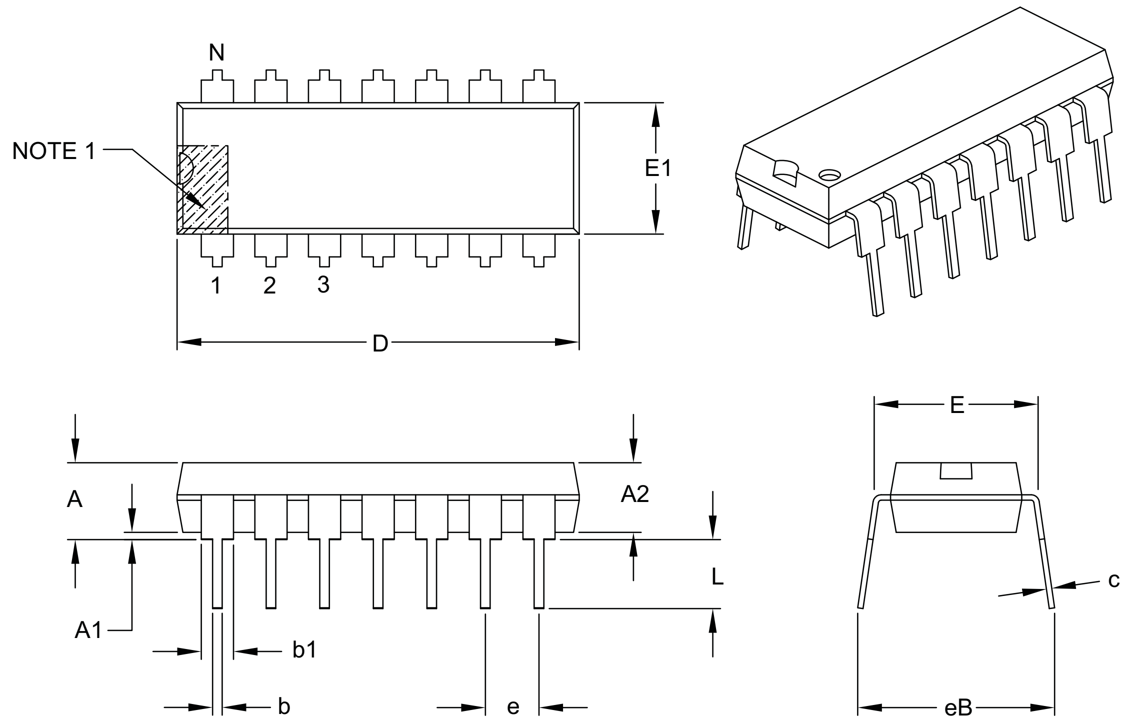
BSC Basic Dimension Theoretically exact value shown without tolerances

REF Reference Dimension usually without tolerance for information purposes only

Microchip Technology Drawing C[illegible]B

[illegible]-Lead Plastic Dual In-Line [illegible]P[illegible] – [illegible] mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	[illegible]		
Pitch	e	[illegible] BSC		
Top to Seating Plane	A	–	–	[illegible]
Molded Package Thickness	A[illegible]	[illegible]	[illegible]	[illegible]
Base to Seating Plane	A[illegible]	[illegible]	–	–
Shoulder to Shoulder Width	E	[illegible]	[illegible]	[illegible]
Molded Package Width	E[illegible]	[illegible]	[illegible]	[illegible]
Overall Length	D	[illegible]	[illegible]	[illegible]
Tip to Seating Plane	L	[illegible]	[illegible]	[illegible]
Lead Thickness	c	[illegible]	[illegible]	[illegible]
Upper Lead Width	b[illegible]	[illegible]	[illegible]	[illegible]
Lower Lead Width	b	[illegible]	[illegible]	[illegible]
Overall Row Spacing §	eB	–	–	[illegible]

Notes:

1. Pin [illegible] visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed [illegible] per side.
4. Dimensioning and tolerancing per ASME Y[illegible]M.

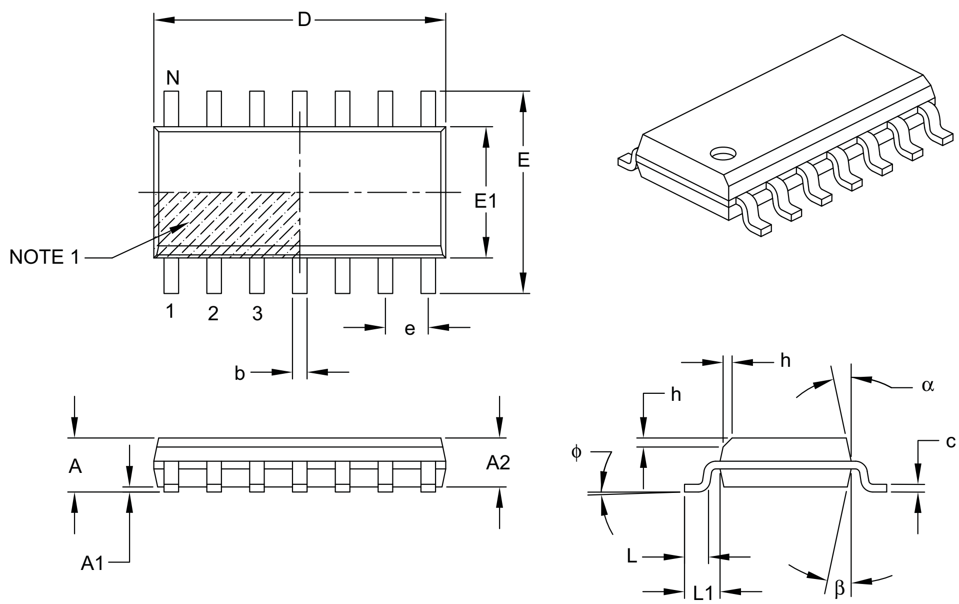
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C[illegible]B

© 2009 Microchip Technology Inc.

Lead Plastic Small Outline SL – Narrow mm Body [SOIC]

Note For the most current package drawings please see the Microchip Packaging Specification located at http www microchip com packaging



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		[illegible]	
Pitch	e		BSC	
Overall Height	A	–	–	[illegible]
Molded Package Thickness	A	[illegible]	–	–
Standoff §	A	[illegible]	–	[illegible]
Overall Width	E		BSC	
Molded Package Width	E		BSC	
Overall Length	D		BSC	
Chamfer optional	h	[illegible]	–	[illegible]
Foot Length	L	[illegible]	–	[illegible]
Footprint	L		REF	
Foot Angle	φ	°	–	°
Lead Thickness	c	[illegible]	–	[illegible]
Lead Width	b	[illegible]	–	[illegible]
Mold Draft Angle Top	α	°	–	°
Mold Draft Angle Bottom	β	°	–	°

Notes

Pin visual index feature may vary but must be located within the hatched area

§ Significant Characteristic

Dimensions D and E do not include mold flash or protrusions Mold flash or protrusions shall not exceed mm per side

Dimensioning and tolerancing per ASME Y M

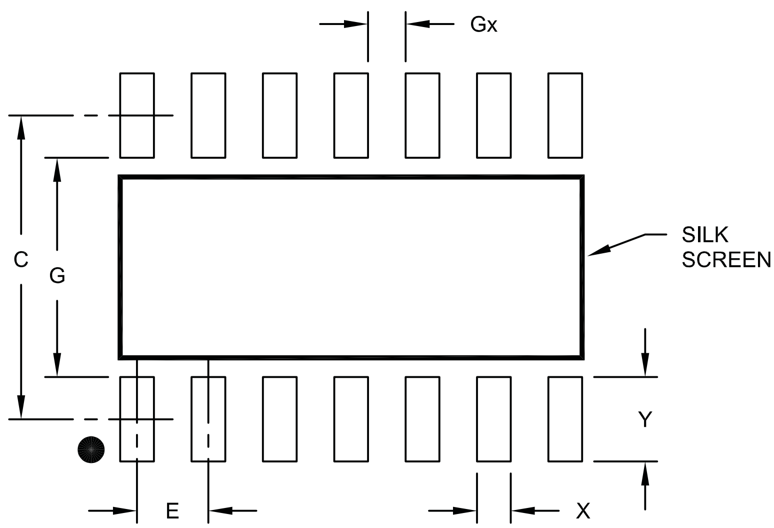
BSC Basic Dimension Theoretically exact value shown without tolerances

REF Reference Dimension usually without tolerance for information purposes only

Microchip Technology Drawing C B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

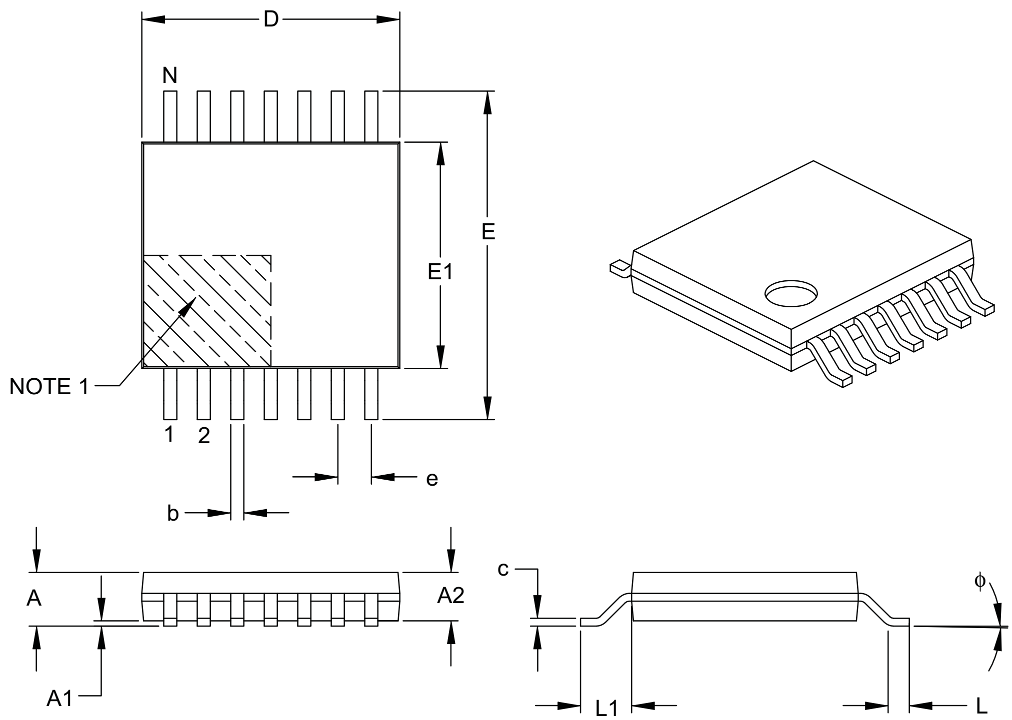
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

© 2009 Microchip Technology Inc.

[illegible]-Lead Plastic Thin Shrink Small Outline (ST) – [illegible] mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	[illegible]		
Pitch	e	[illegible] BSC		
Overall Height	A	–	–	[illegible]
Molded Package Thickness	A[illegible]	[illegible]	[illegible]	[illegible]
Standoff	A[illegible]	[illegible]	–	[illegible]
Overall Width	E	[illegible] BSC		
Molded Package Width	E[illegible]	[illegible]	[illegible]	[illegible]
Molded Package Length	D	[illegible]	[illegible]	[illegible]
Foot Length	L	[illegible]	[illegible]	[illegible]
Footprint	L[illegible]	[illegible] REF		
Foot Angle	φ	[illegible]°	–	[illegible]°
Lead Thickness	c	[illegible]	–	[illegible]
Lead Width	b	[illegible]	–	[illegible]

Notes:

[illegible] Pin [illegible] visual index feature may vary, but must be located within the hatched area.

[illegible] Dimensions D and E[illegible] do not include mold flash or protrusions. Mold flash or protrusions shall not exceed [illegible] mm per side.

[illegible] Dimensioning and tolerancing per ASME Y[illegible]M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C[illegible]B

NOTES:

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APPENDIX A: REVISION HISTORY

Revision D (February 2009)

The following is the list of modifications:

1. Changed all references to 6.0V back to 5.5V throughout document.
2. **Design Aids:** Name change for Mindi Simulation Tool.
3. **Section 1.0 "Electrical Characteristics", DC Electrical Specifications:** Corrected "Maximum Output Voltage Swing" condition from 0.9V Input Overdrive to 0.5V Input Overdrive.
4. **Section 1.0 "Electrical Characteristics", AC Electrical Specifications:** Changed Phase Margin condition from G = +1 to G= +1 V/V.
5. **Section 1.0 "Electrical Characteristics", AC Electrical Specifications:** Changed Settling Time, 0.2% condition from G = +1 to G = +1 V/V.
6. **Section 1.0 "Electrical Characteristics":** Added Section 1.1 Test Circuits.
7. **Section 5.0 "Design AIDS"**: Name change for Mindi Simulation Tool. Added new boards to **Section 5.5 "Analog Demonstration and Evaluation Boards"** and new application notes to **Section 5.6 "Application Notes"**.
8. Updates **Appendix A: "Revision History"**

Revision C (March 2006)

The following is the list of modifications:

1. Added SOT-23-5 package option for single op amps MCP6021 and MCP6021R (E-temp only).
2. Added MSOP-8 package option for E-temp single op amp (MCP6021).
3. Corrected package drawing on front page for dual op amp (MCP6022).
4. Clarified spec conditions (I_{SC}, PM and THD+N) in **Section 2.0 "Typical Performance Curves"**.
5. Added **Section 3.0 "Pin Descriptions"**.
6. Updated **Section 4.0 "Applications information"** for THD+N, unused op amps, and gain peaking discussions.
7. Corrected and updated package marking information in **Section 6.0 "Packaging Information"**.
8. Added **Appendix A: "Revision History"**.

Revision B (November 2003)

- Second Release of this Document

Revision A (November 2001)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. — Device | **X** — Temperature Range | **/XX** — Package

Device:	MCP6021	Single Op Amp
	MCP6021T	Single Op Amp (Tape and Reel for SOT-23, SOIC, TSSOP, MSOP)
	MCP6021R	Single Op Amp
	MCP6021RT	Single Op Amp (Tape and Reel for SOT-23)
	MCP6022	Dual Op Amp
	MCP6022T	Dual Op Amp (Tape and Reel for SOIC and TSSOP)
	MCP6023	Single Op Amp w/ $\overline{CS}$
	MCP6023T	Single Op Amp w/ $\overline{CS}$ (Tape and Reel for SOIC and TSSOP)
	MCP6024	Quad Op Amp
	MCP6024T	Quad Op Amp (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I	= -40°C to +85°C
	E	= -40°C to +125°C
Package:	OT	= Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6021, E-Temp; MCP6021R, E-Temp)
	MS	= Plastic MSOP, 8-lead (MCP6021, E-Temp)
	P	= Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN	= Plastic SOIC (150mil Body), 8-lead
	SL	= Plastic SOIC (150 mil Body), 14-lead
	ST	= Plastic TSSOP, 8-lead (MCP6021,I-Temp; MCP6022, I-Temp, E-Temp; MCP6023, I-Temp, E-Temp;)
	ST	= Plastic TSSOP, 14-lead

Examples:

a) MCP6021T-E/OT: Tape and Reel, Extended temperature, 5LD SOT-23.
b) MCP6021-E/P: Extended temperature, 8LD PDIP.
c) MCP6021-E/SN: Extended temperature, 8LD SOIC.

a) MCP6021RT-E/OT: Tape and Reel, Extended temperature, 5LD SOT-23.

a) MCP6022-I/P: Industrial temperature, 8LD PDIP.
b) MCP6022-E/P: Extended temperature, 8LD PDIP.
c) MCP6022T-E/ST: Tape and Reel, Extended temperature, 8LD TSSOP.

a) MCP6023-I/P: Industrial temperature, 8LD PDIP.
b) MCP6023-E/P: Extended temperature, 8LD PDIP.
c) MCP6023-E/SN: Extended temperature, 8LD SOIC.

a) MCP6024-I/SL: Industrial temperature, 14LD SOIC.
b) MCP6024-E/SL: Extended temperature, 14LD SOIC.
c) MCP6024T-E/ST: Tape and Reel, Extended temperature, 14LD TSSOP.

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