ACE24C32/64B
Two-wire Serial EEPROM

Description

The ACE24C32B/ACE24C64B provides 32,768/65,536 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

Features

- Wide Voltage Operation - V_{CC} = 1.7V to 5.5V
- Operating Ambient Temperature: -40℃ to +85℃
- Internally Organized: ACE24C32B, 4096 * 8 (2K bits) / ACE24C64B, 8192 * 8 (4K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 kHz (1.7V, 2.5V, 2.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 32-byte Page (32K, 64K) Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years

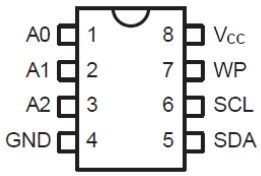
Absolute Maximum Ratings

Operating Temperature	-40℃ to 85℃
Storage Temperature	-65℃ to 150℃
DC Supply Voltage	0.3V ot 6.5V
Input / Output Voltage	GND-0.3V ot V_{CC}+0.3V

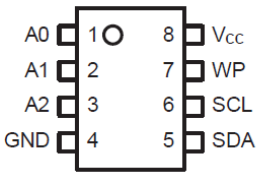
Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Packaging Type

DIP-8



SOP-8



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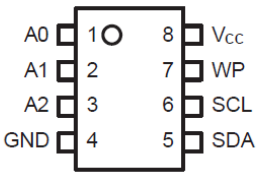

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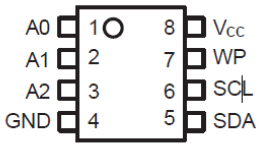
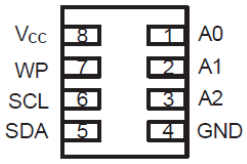


TDFN



Pin Configurations

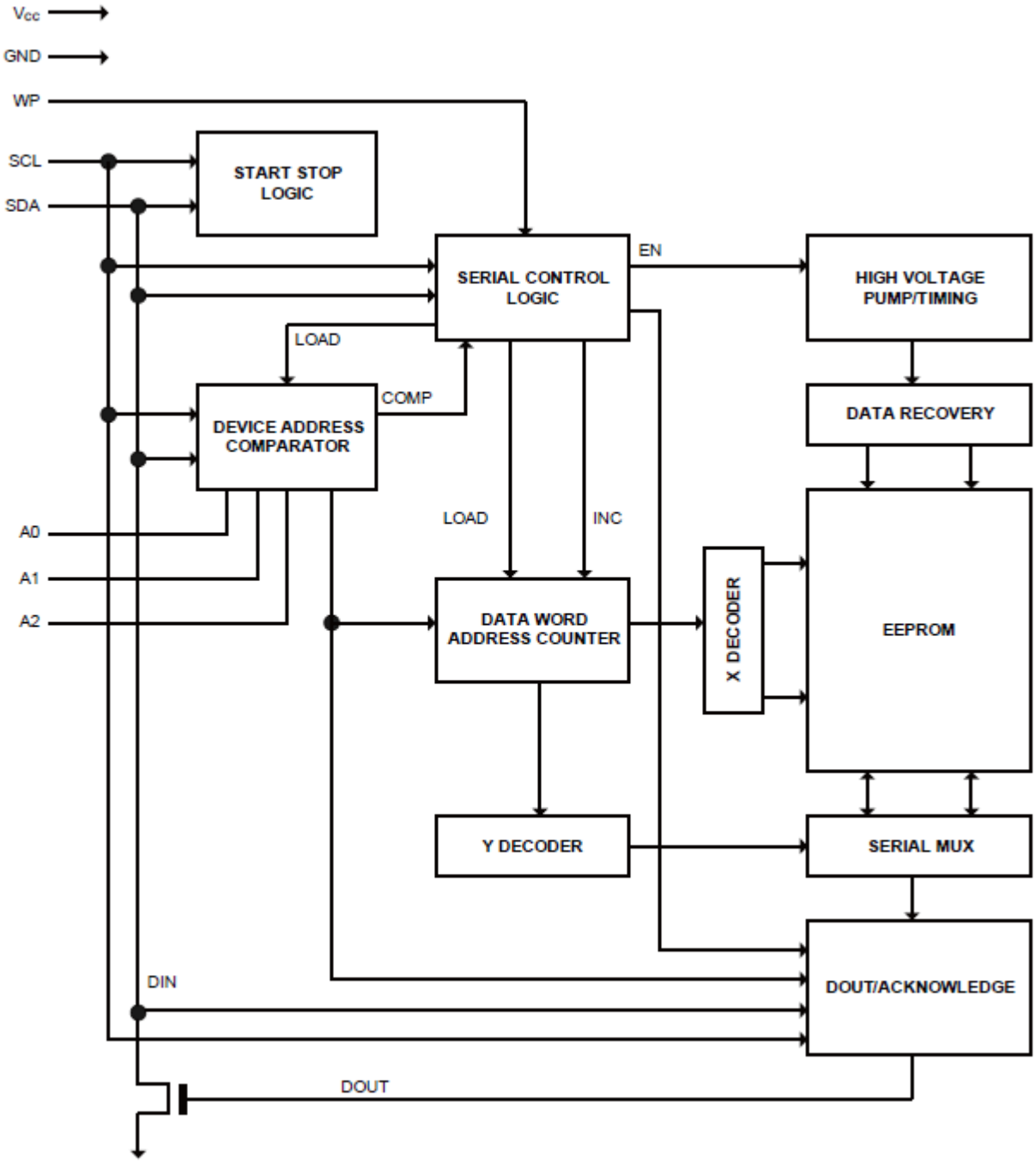
Pin Name	Functions
AO-A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
V_{CC}	Power Supply

Ordering information

ACE24C32/64B XX + X H

- H : Halogen-free
- X : U : Tube / T : Tape and Reel
- + : Pb - free
- XX : DP : DIP-8 / FM : SOP-8 / TM : TSSOP-8 / OM : MSOP-8 / DM : TDFN

Block Diagram



Pin Descriptions

Device/Page Addresses (A2, A1 and A0):

The A2, A1 and A0 pins are device address inputs that are hard wired for the ACE24C32B/ACE24C64B. Eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

Serial Data (SDA):

The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

Serial Clock (SCL):

The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Write Protect (WP):

The ACE24C32B/ACE24C64B has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following Table 2.

WP Pin Status	Part of the Array Protected	
	ACE24C32B	ACE24C64B
At V_{CC}	Full (32K) Array	Full (256K) Array
At GND	Normal Read / Write Operations	

Table 2 Write Protect

Memory Organization

ACE24C32B, 32K Serial EEPROM:

Internally organized with 128 pages of 32 bytes each, the 32K requires an 12-bit data word address for random word address.

ACE24C64B, 64K Serial EEPROM:

Internally organized with 256 pages of 32 bytes each, the 64K requires an 13-bit data word address for random word address.

Device Operation

Clock and Data Transitions:

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition:

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2).

Stop Condition:

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see to Figure 2).

Acknowledge:

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. The happens during the ninth clock cycle.

Standby Mode :

The ACE24C32B/ACE24C64B features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

Memory Reset :

After an interruption in protocol power loss or system reset, any two-wire part can be protocol reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high and then.
3. Create a start condition.

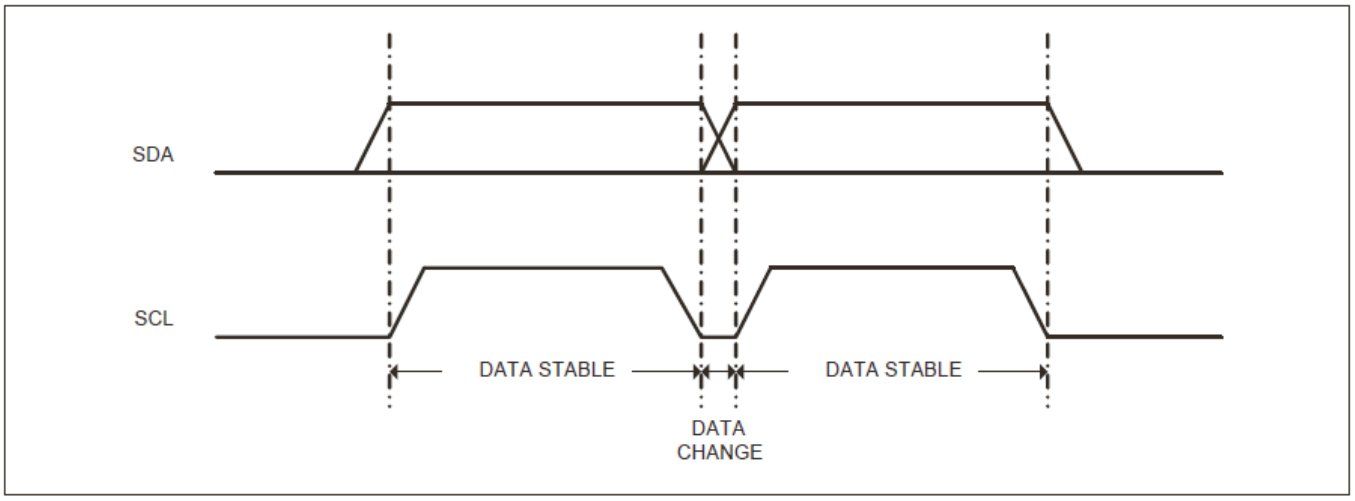


Figure 1: Data Validity

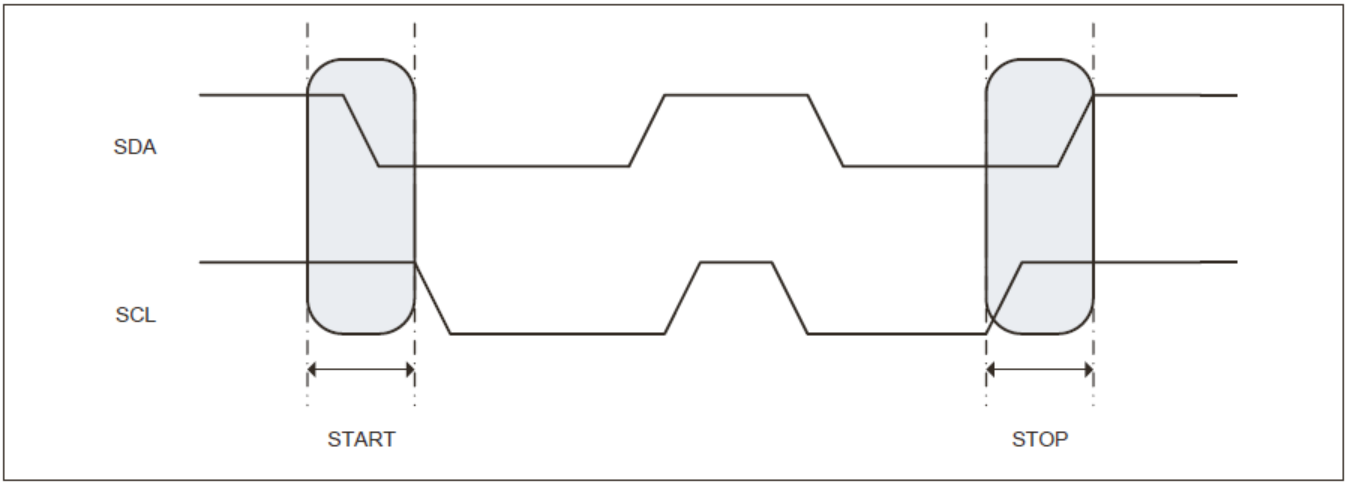


Figure 2: Start and Stop Definition

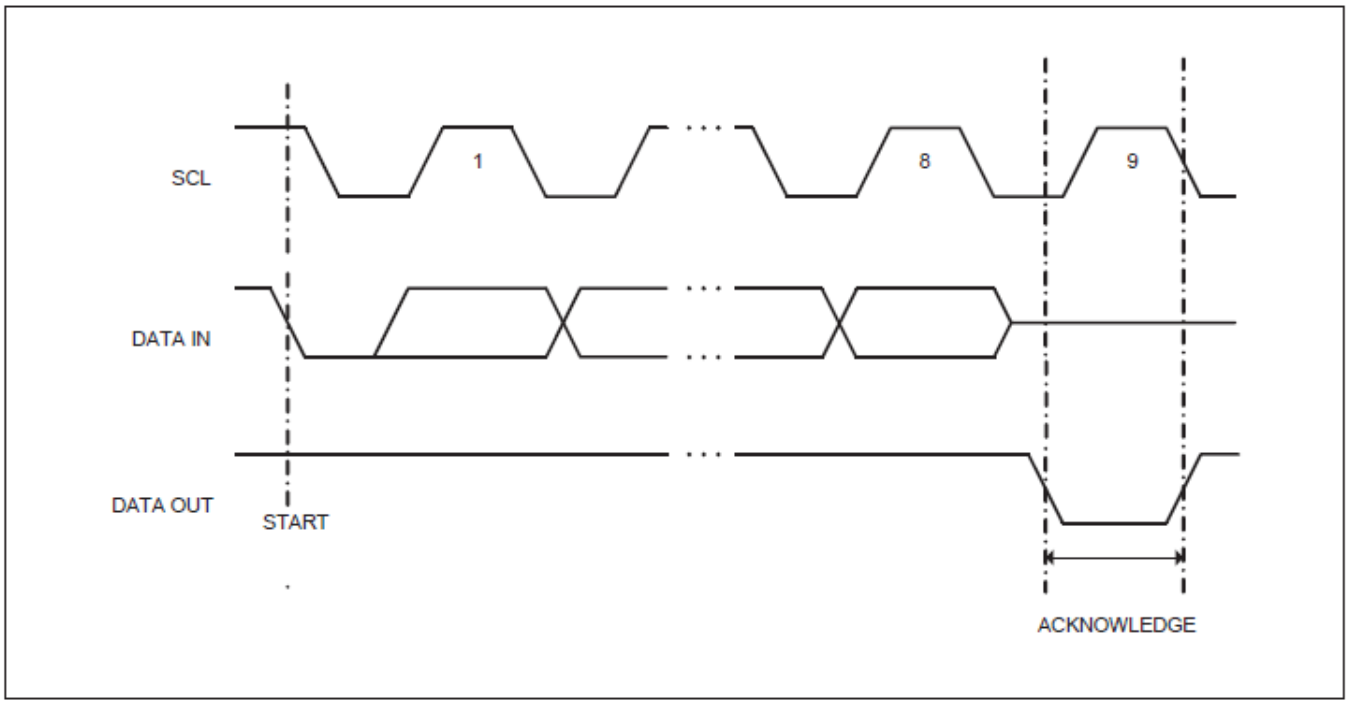


Figure 3: Output Acknowledge

Device Addressing

The 32K, and 64K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see to Figure 4).

The device address word consists of a mandatory “1”, “0” sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 32K/64K EEPROM. These 3 bits must compare to their corresponding hard-wired input pins.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a “0”. If a compare is not made, the chip will return to a standby state.

Write Operations

Byte Write:

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see to Figure 5).

Page Write:

The 32K/64K EEPROM is capable of an 32-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 (32K/64K) more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see to Figure 6).

The data word address lower three (32K/64K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 (32K/64K) data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

Acknowledge Polling:

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a “0” allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1". There are three read operations: current address read, random address read and sequential read.

Current Address Read:

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7).

Random Read:

A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 8).

Sequential Read:

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 9).

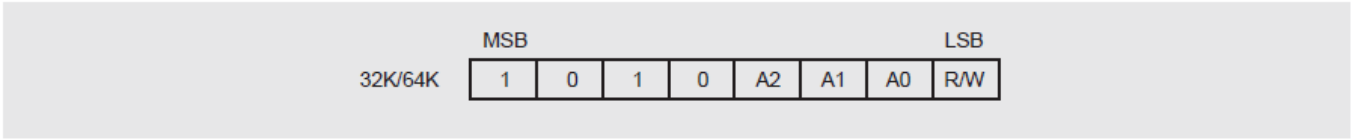


Figure 4: Device Address

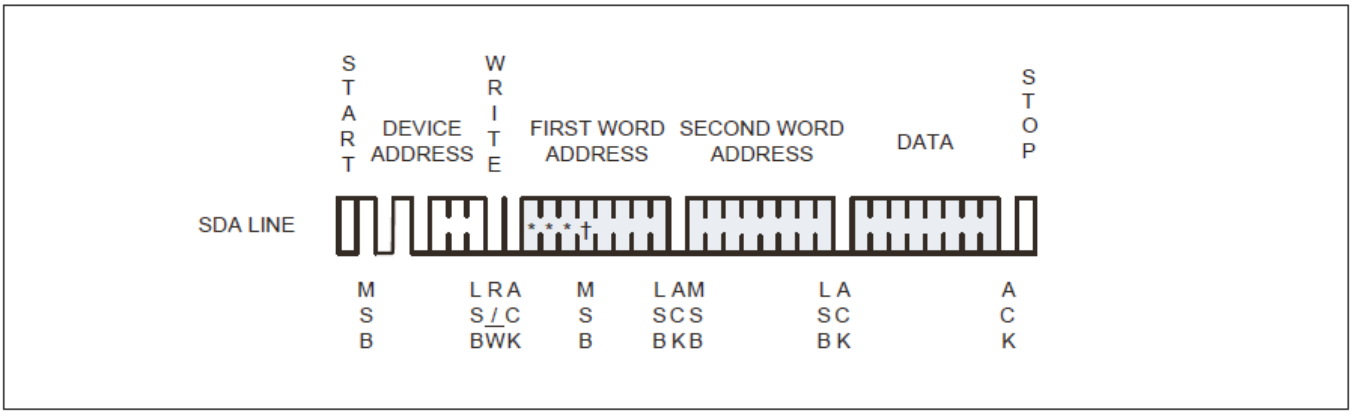


Figure 5: Byte write

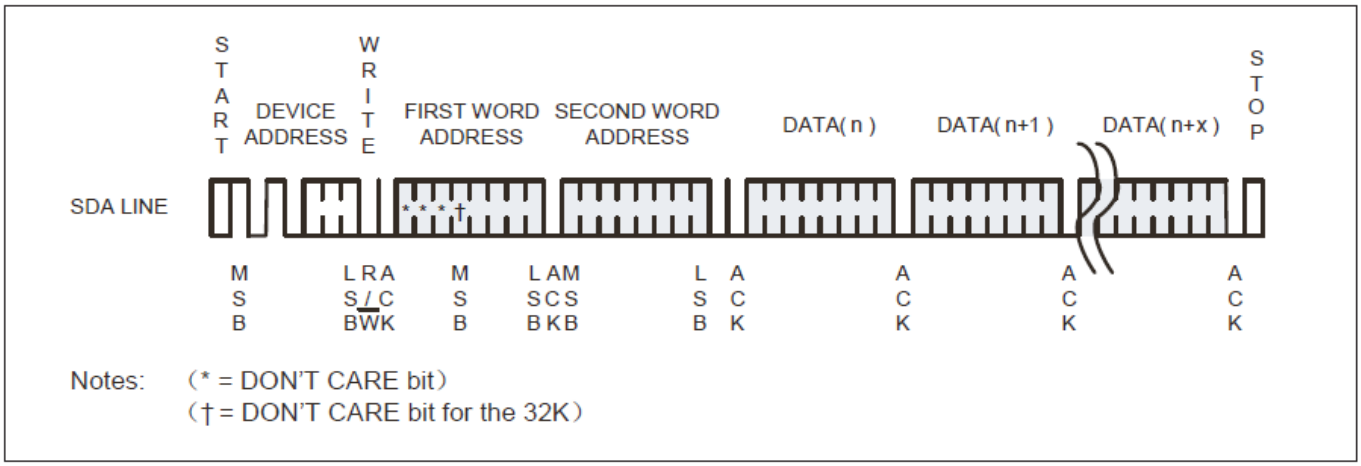


Figure 6: Page write

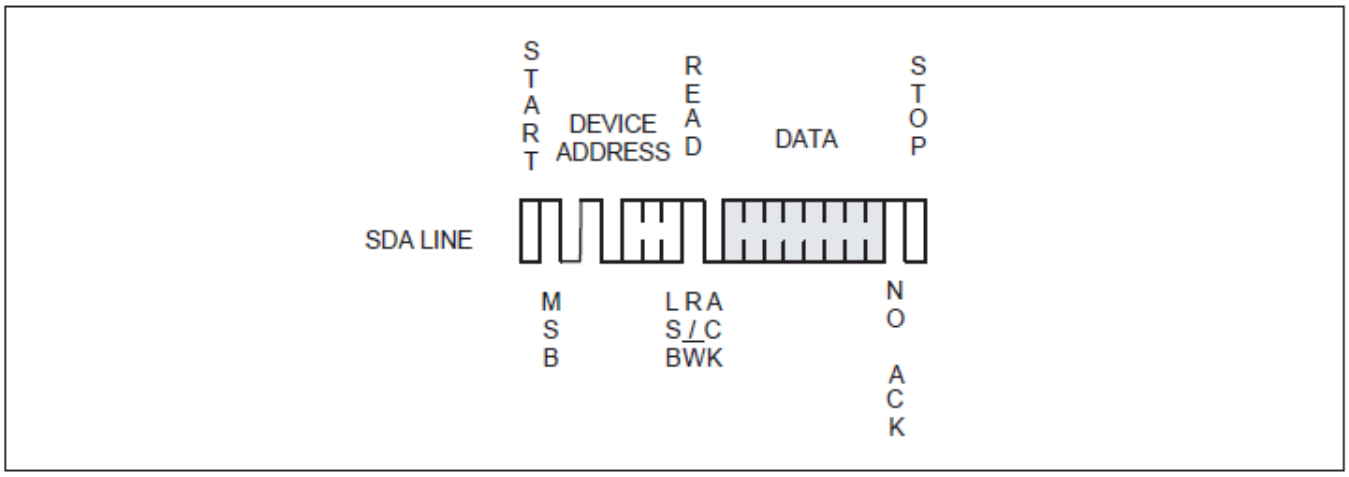


Figure 7: Current Address Read

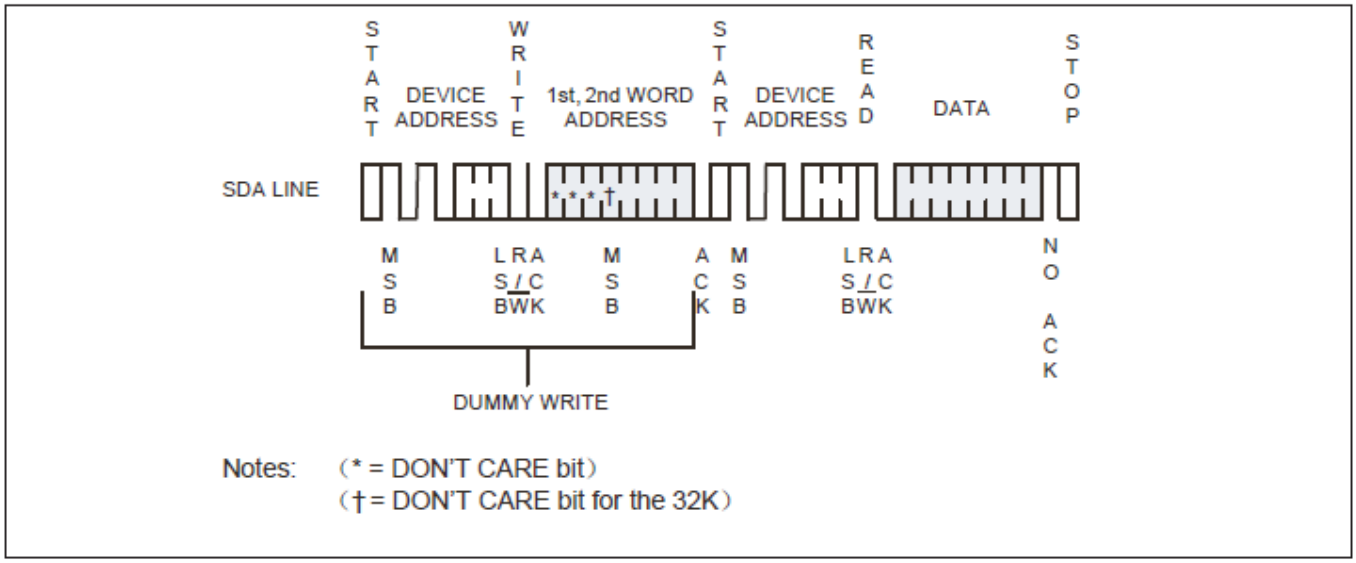


Figure 8: Random Read

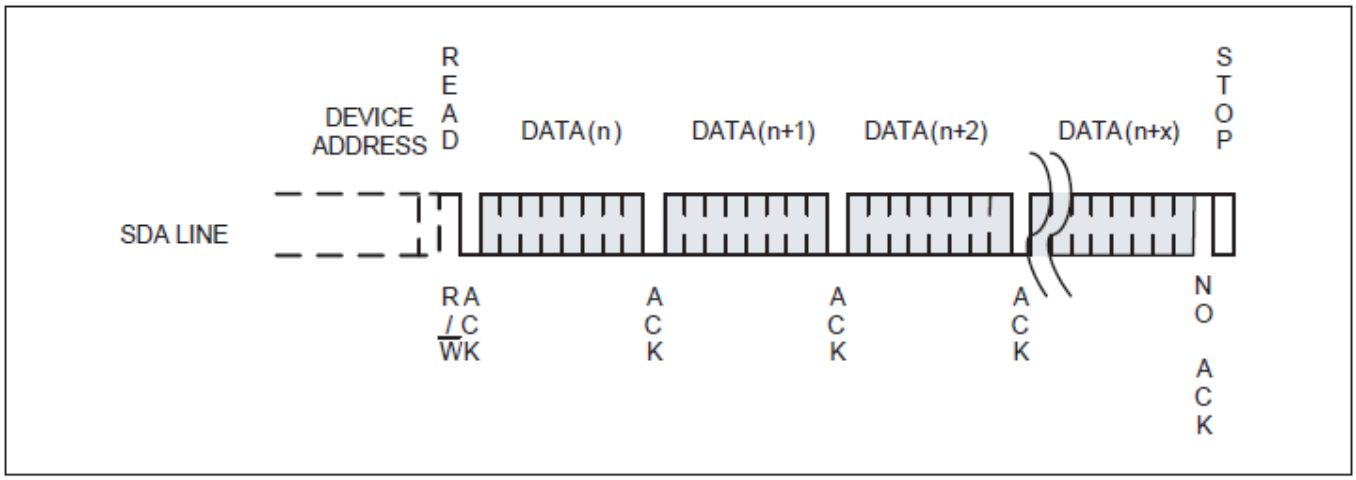


Figure 9: Sequential Read

Pin Capacitance

Applicable over recommended operating range from: T_A = 25℃, f = 1.0 MHz, V_{CC} = +1.7V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

DC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current	Read at 400kHz		0.4	1.0	mA
I_{CC2}	Supply Current	Write at 400 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = V_{CC} or GND			3.0	μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND			3.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND		0.05	3.0	μA
V_{IL1}	Input Low Level	V_{CC}=1.8V to 5.5V	-0.3		V_{CC}*0.3	V
V_{IH1}	Input High Level	V_{CC}=1.8V to 5.5V	V_{CC}*0.7		V_{CC}+0.3	V
V_{IL2}	Input Low Level	V_{CC}=1.7V	-0.3		V_{CC}*0.3	V
V_{IH2}	Input High Level	V_{CC}=1.7V	V_{CC}*0.7		V_{CC}+0.3	V
V_{OL3}	Output Low Level	I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Level	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level	I_{OL} = 0.15 mA			0.2	V

AC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, C_L=1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	1.7V≦V_{CC}<2.5V			2.5V≦V_{CC}≦5.5V			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Clock Frequency, SCL			400			1000	kHz
T_{LOW}	Clock Pulse Width Low	1.2			0.6			μs
T_{HIGH}	Clock Pulse Width High	0.6			0.4			μs
T_I	Noise Suppression Time			50			40	ns
T_{AA}	Clock Low to Data Out Valid	0.05		0.9	0.05		0.55	μs
T_{BUF}	Time the bus must be free before a new transmission can Start	1.2			0.5			μs
$T_{HD.STA}$	Start Hold Time	0.6			0.25			μs
$T_{SU.STA}$	Start Setup Time	0.6			0.25			μs
$T_{HD.DAT}$	Data In Hold Time	0			0			μs
$T_{SU.DAT}$	Data In Setup Time	100			100			ns
T_R	Inputs Rise Time			0.3			0.3	μs
T_F	Inputs Fall Time			300			100	ns
$T_{SU.STO}$	Stop Setup Time	0.6			0.25			μs
T_{DH}	Data Out Hold Time	50			50			ns
T_{WR}	Write Cycle Time (for 04B/16B)		1.5	5		1.5	5	ms
Endurance	5.0V, 25℃, Page Mode	1M						Write Cycles

Notes:1. This parameter is characterized and not 100% tested.

2.AC measurement conditions:

R_L (connects to Vcc): 1.3kΩ(2.5V,5V),10kΩ(1.7V)

Input pulse voltages: 0.3 Vcc to 0.7 Vcc

Input rise and fall times: ≦50 ns

Input and output timing reference voltages: 0.5Vcc

The value of RL should be concerned according to the actual loading on the user's system.

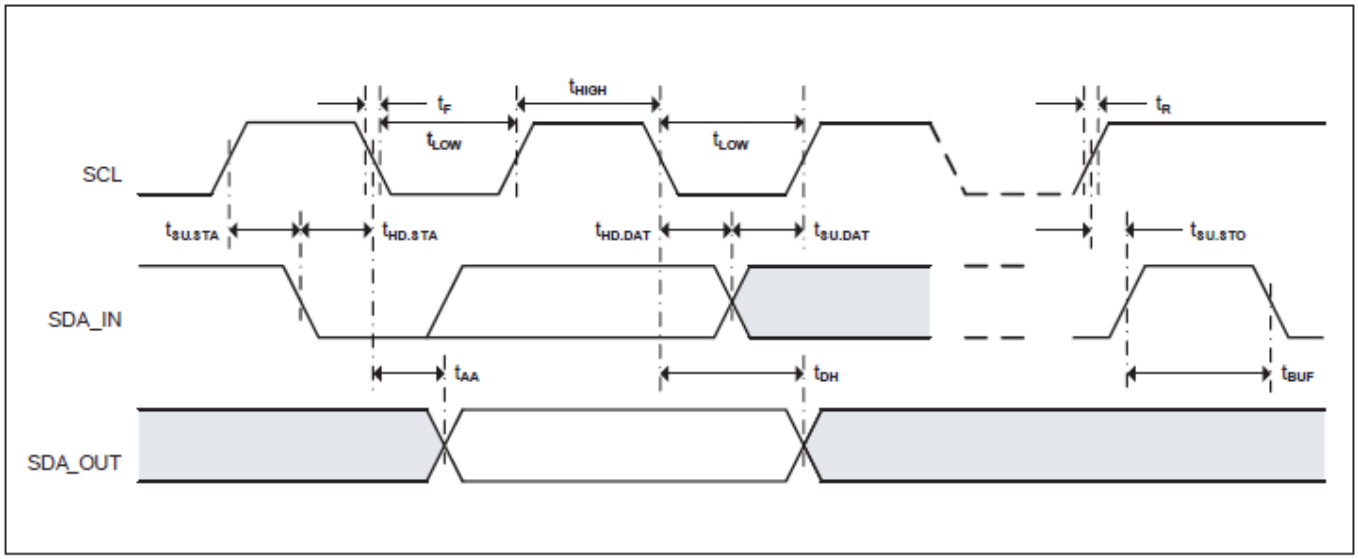


Figure 10 · SCL: Serial Clock, SDA: Serial Data I/O

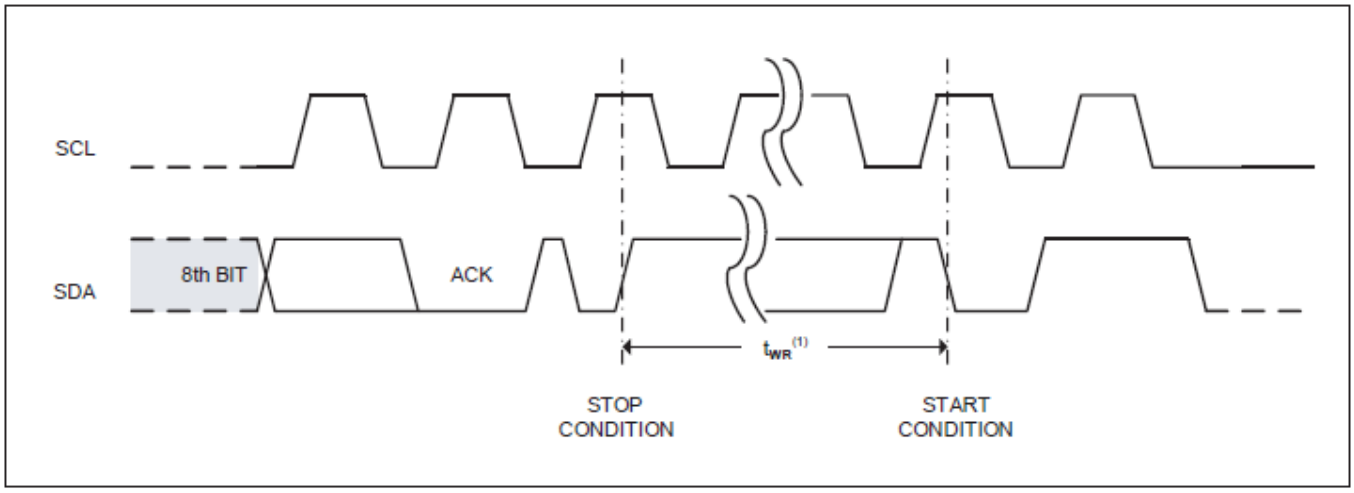
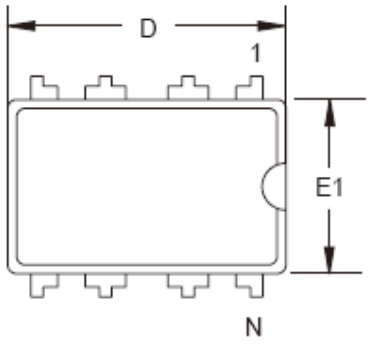


Figure 11 · SCL: Serial Clock, SDA: Serial Data I/O

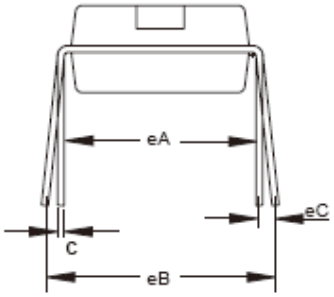
Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Packaging information

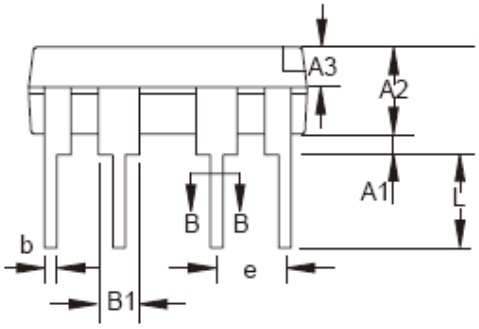
DIP-8



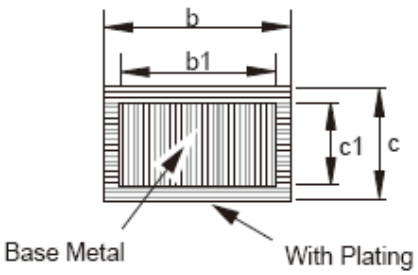
Top View



End View



Side View



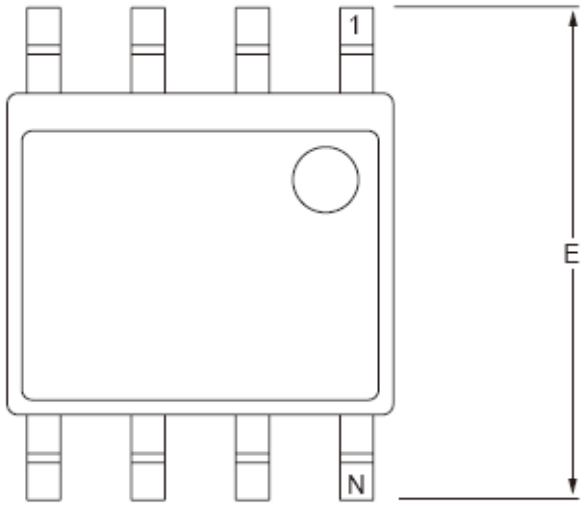
Section B-B

COMMON DIMENSIONS
(Unit of Measure = mm)

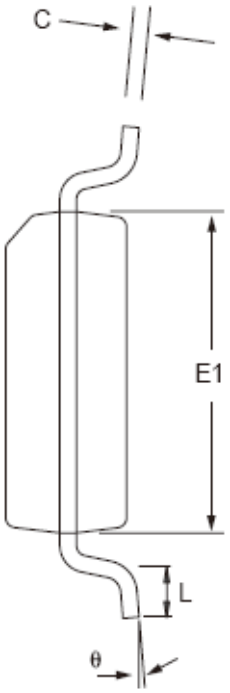
SYMBOL	MIN	MAX
A	3.60	4.00
A1	0.51	-
A2	3.10	3.50
A3	1.50	1.70
b	0.44	0.53
b1	0.43	0.48
B	1.52 BSC	
c	0.25	0.31
c1	0.24	0.26
D	9.05	9.45
E1	6.15	6.55
e	2.54 BSC	
eA	7.62 BSC	
eB	7.62	9.50
eC	0	0.94
L	3.00	-

Packaging information

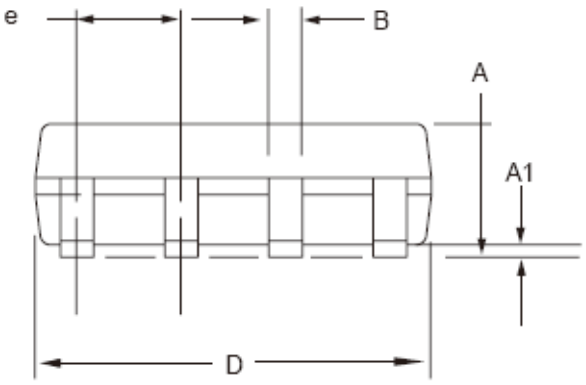
SOP-8



Top View



End View



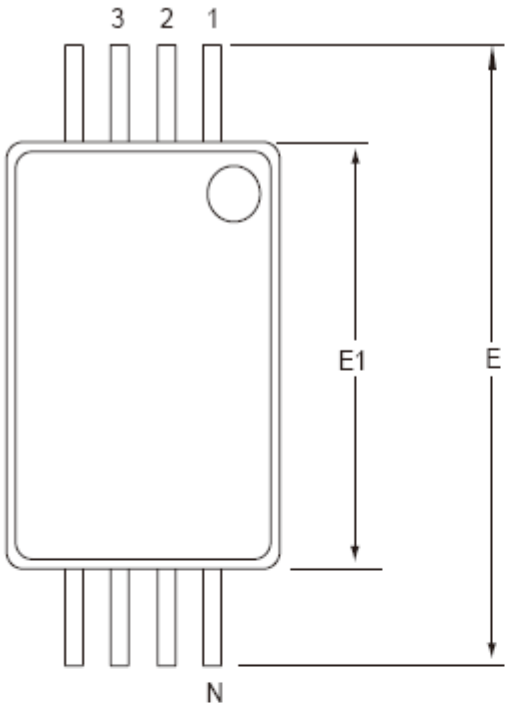
Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

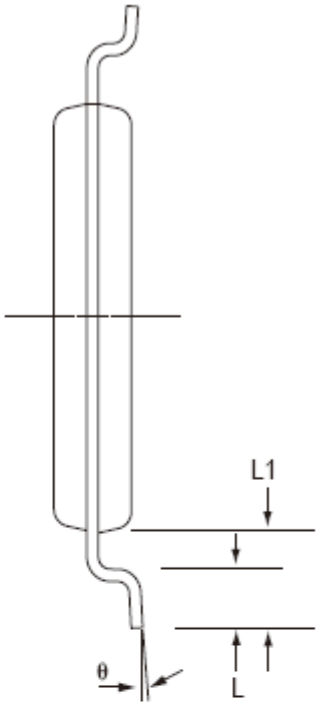
SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.31	0.51
C	0.17	0.25
D	4.70	5.10
E1	3.80	4.00
E	5.79	6.20
e	1.27 BSC	
L	0.40	1.27
θ	0°	8°

Packaging information

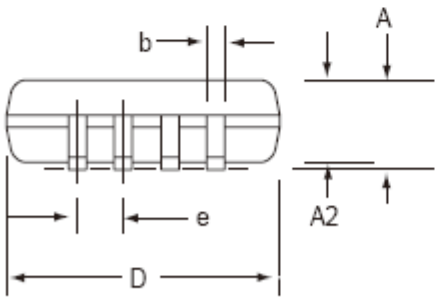
TSSOP-8



Top View



End View



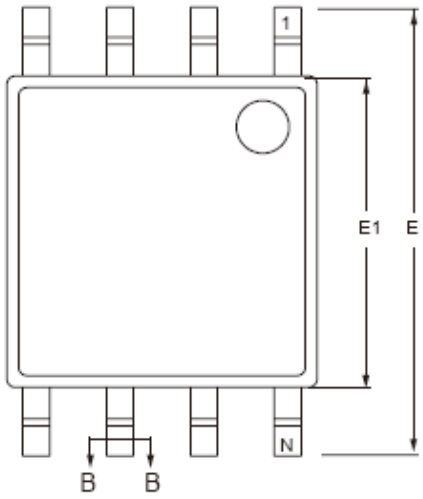
Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

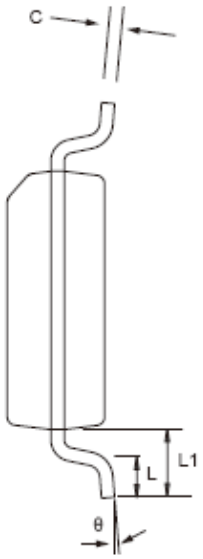
SYMBOL	MIN	MAX
D	2.80	3.20
E	6.20	6.60
E1	4.20	4.60
A	–	1.20
A2	0.80	1.15
b	0.19	0.30
e	0.65 BSC	
L	0.45	0.75
L1	1.00 BSC	
θ	0°	8°

Packaging information

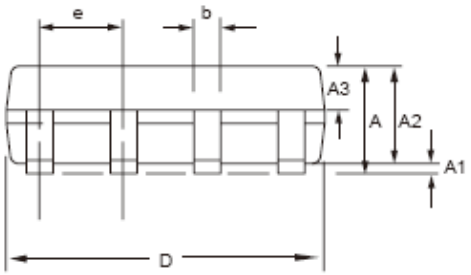
MSOP-8



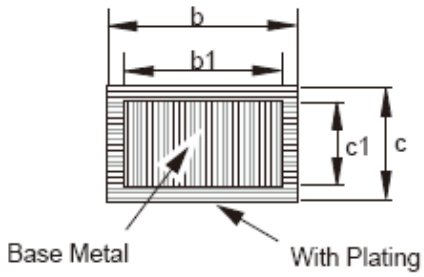
Top View



End View



Side View



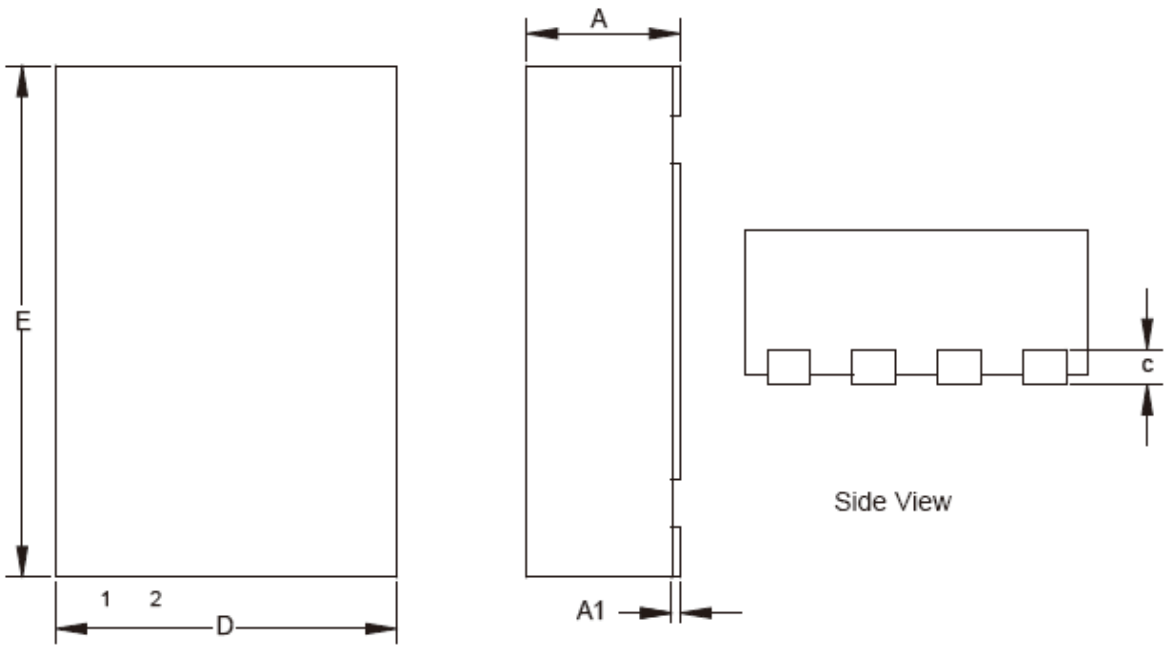
Section B-B

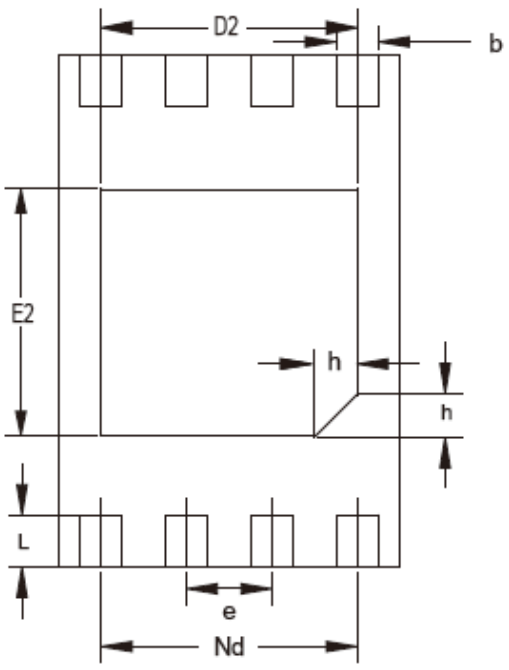
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	-	1.10
A1	0.05	0.15
A2	0.75	0.95
A3	0.30	0.40
b	0.29	0.38
b1	0.28	0.33
c	0.15	0.20
c1	0.14	0.16
D	2.90	3.10
E	4.70	5.10
E1	2.90	3.10
e	0.65 BSC	
L	0.40	0.70
L1	0.95 BSC	
θ	0°	8°

Packaging information

TDFN





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	0.70	0.80
A1	-	0.05
b	0.18	0.30
c	0.18	0.25
D	1.90	2.10
D2	1.50 REF	
e	0.50 BSC	
Nd	1.50 BSC	
E	2.90	3.10
E2	1.60 BSC	
L	0.30	0.50
h	0.20	0.30

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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