# ACE24C512D
# Two-wire Serial EEPROM

## Description

The ACE24C512D provides wide voltage of 524,288 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 65,536 words of 8 bits each. Wich 128-bit UID and 128-byte Security Sector. The device's cascadable feature allows up to 8 devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

## Features

- Low Operation Voltage: Vcc = 1.7V to 5.5V
- Internally Organized: 65,536 x 8
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 1MHz (2.5V~5.5V) and 400 kHz (1.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 128-byte Page Write Modes
- Partial Page Writes are Allowed
- Lockable 128-Byte Security Sector
- 128-Bit Unique ID for each device
- Self-timed Write Cycle (5 ms max)
- High-reliability
  - Endurance: 1,000,000 Write Cycles
  -Data Retention: 40 Years

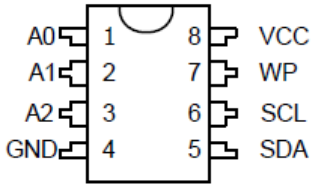
## Absolute Maximum Ratings

| | |
|---|---|
| Operating Temperature | -55℃ to +125℃ |
| Storage Temperature | -65℃ to +150℃ |
| Voltage on Any Pin with Respect to Ground | -1.0V to +7.0V |
| Maximum Operating Voltage | 6.25V |
| DC Output Current | 5.0 mA |

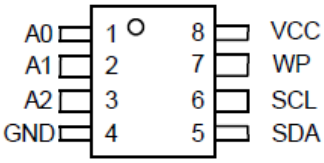
*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Packaging Type

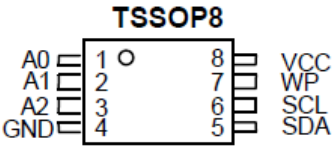
DIP 8



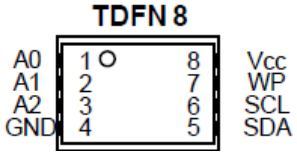

SOP8




TSSOP8




TDFN 8




## Pin Configurations

| Pin Name | Function |
|---|---|
| A0~A2 | Device Address Inputs |
| SDA | Serial Data Input / Output |
| SCL | Serial Clock Input |
| WP | Write Protect |
| VCC | Power Supply |
| GND | Ground |

## Block Diagram

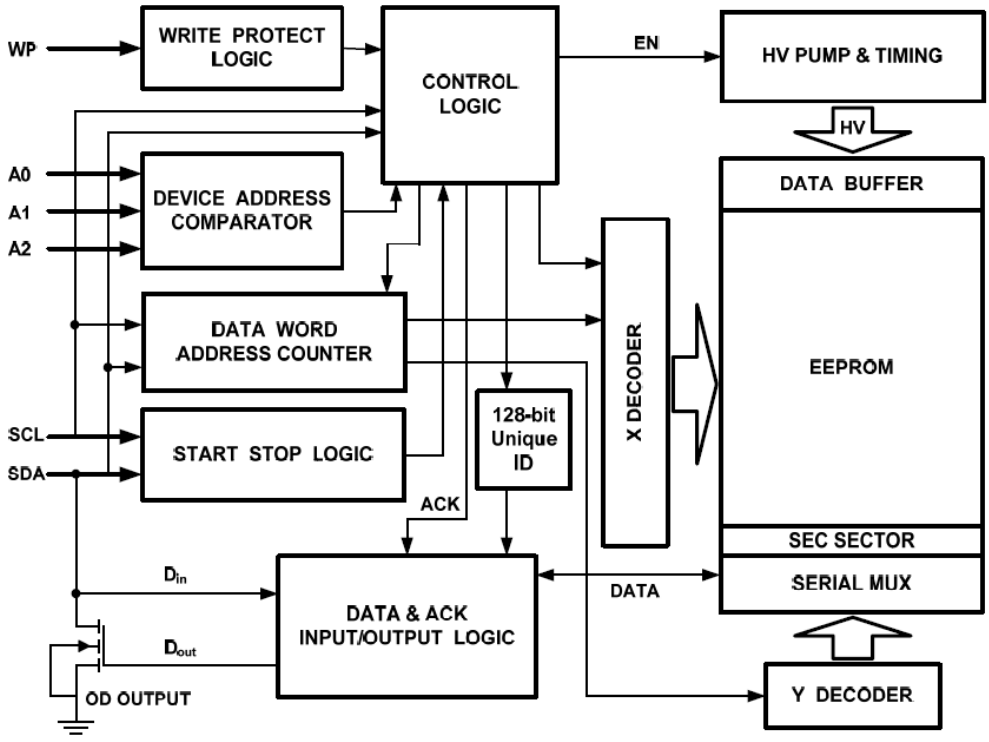
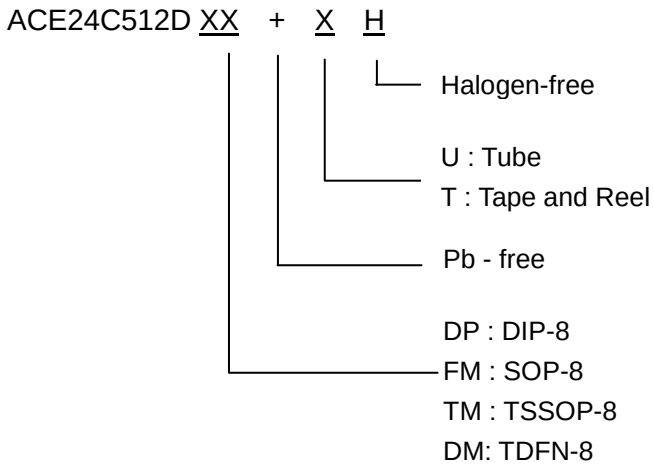



Figure 1

## Ordering information




**Serial Clock (SCL):**

The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**Serial Data (SDA):**

The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

**Device/Page Addresses (A2, A1, A0):**

The A2, A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other ACE24CXXX devices. When the pins are hardwired, as many as eight 512K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is < 3pF, if coupling is > 3 pF, ACE recommends connecting the address pins to GND.

**Write Protect (WP):**

The ACE24C512D has a Write Protect pin that provides hardware data protection. The WP pin allows normal write operations when connected to ground (GND). When the Write Protect pin is connected to Vcc. All write operations to the memory are inhibited. If the pin is left floating, the WP pin well be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is < 3pF, if coupling is > 3 pF, ACE recommends connecting the WP to GND. Switching WP to VCC prior to a write operation creates a software write protected function

## Write Protect Description

| WP Pin Status | Part of the Array Protected |
|---|---|
| WP=$V_{CC}$ | Full Memory |
| WP=GND | Normal Read/Write Operations |

## Memory Organization

**ACE24C512D, 512K Serial EEPROM:**

Internally organized with 512 pages of 128 bytes each, the 512K requires a 16-bit data word address for random word addressing.

Security Sector: The ACE24C512D offers 128-byte Security Sectors which can be written and (later) permanently locked in Read-only mode. This memory may be used by the system manufacturers to store security and other important information separately from the main memory array.

Unique ID: The ACE24C512D utilizes a separate memory block containing a factory programmed read-only 128-bit Unique ID.

| Device ADDR | Page ADDR | Byte Number | | |
|---|---|---|---|---|
| | | 127 | … | 0 |
| 1010 | 0 | Date Memory(512PX128B) | | |
| | 1 | | | |
| | 2 | | | |
| | … | | | |
| | 511 | | | |
| 1011 | xxxx x00x<br>xxxx xxxx[1] | Security Sector(128 Bytes) | | |
| 1011 | xxxx xx1x<br>xxxx xxxx[2] | Unique ID(128Bits) | | |

Note 1. Address bits ADDR<10:9>must be 00,ADDR<6:0> define byte address, Other bits are don't care

2. Address bits ADDR<10:9>must be x1,ADDR<3:0> define byte address, Other bits are don't care

## Pin Capacitance

| Symbol | Test Condition | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{I/O}$[1] | Input Capacitance | 8 | pF | $V_{I/O}$ = 0V,f=1MHz |
| $C_{OUT}$[1] | Output Capacitance | 6 | pF | $V_{IN}$ = 0V,f=1MHz |

Note 1. This parameter is characterized and is not 100% tested.

## DC Characteristics

Applicable over recommended operating range from: $T_A$ = -40℃ to +85℃, $V_{CC}$ = +1.7V to +5.5V, (unless otherwise noted).

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 1.7 | | 5.5 | V |
| $I_{CC1}$ | Supply Current | $V_{CC}$ = 5.0V, Read at 400K | | 0.4 | 1.0 | mA |
| $I_{CC2}$ | Supply Current | $V_{CC}$ = 5.0V, Write at 400K | | 2.0 | 3.0 | mA |
| $I_{SB1}$ | Standby Current | $V_{CC}$=1.7V$_1$ $V_{IN}$=$V_{CC}$ / $V_{SS}$ | | | 1.0 | μA |
| $I_{SB2}$ | Standby Current | $V_{CC}$=5.5V$_1$ $V_{IN}$=$V_{CC}$ / $V_{SS}$ | | | 6.0 | μA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = $V_{CC}$/$V_{SS}$ | | 0.10 | 3.0 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = $V_{CC}$/ $V_{SS}$ | | 0.05 | 3.0 | μA |
| $V_{IL}$[1] | Input Low Level | | -0.6 | | $V_{CC}$x0.3 | V |
| $V_{IH}$[1] | Input High Level | | $V_{CC}$x0.7 | | $V_{CC}$+0.5 | V |
| $V_{OL2}$ | Output Low Level 2 | $V_{CC}$ = 3.0V, $I_{OL}$ = 2.1 mA | | | 0.4 | V |
| $V_{OL1}$ | Output Low Level 1 | $V_{CC}$ = 1.7V, $I_{OL}$ = 0.15 mA | | | 0.2 | V |

Note: 1. $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested.

## AC Characteristics / 400kHz AC characteristics

Recommended operating conditions: $T_A$ = -40℃ to +85℃, $V_{CC}$ = +1.7V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note2.

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency, SCL | | 400 | kHz |
| $t_{LOW}$ | Clock Pulse Width Low | 1.3 | | μs |
| $t_{HIGH}$ | Clock Pulse width High | 0.6 | | μs |
| $t_j$[1] | Noise Suppression Time | | 80 | ns |
| $T_{AA}$ | Clock Low to Data Out Valid | 0.1 | 0.9 | μs |
| $t_{BUF}$[1] | Time the bus must be free before a new transmission can Start | 1.3 | | μs |
| $t_{HD.STA}$ | Start Hold Time | 0.6 | | μs |
| $t_{SU.STA}$ | Start Setup Time | 0.6 | | μs |
| $t_{HD.DAT}$ | Data In Hold Time | 0 | | μs |
| $t_{SU.DAT}$ | Data In Setup Time | 100 | | ns |
| $t_R$ | Input Rise Time[1] | | 300 | ns |
| $t_F$ | Input Fall Time[1] | | 300 | ns |
| $t_{SU.STO}$ | Stop Setup Time | 0.6 | | μs |
| $t_{DH}$ | Data Out Hold Time | 100 | | ns |
| $t_{WR}$ | Write Cycle Time | | 5 | ms |
| Endurance[1] | 3.3V,25℃,Page Mode | 1,000,000 | | Write Cycles |

**1MHz AC characteristics** Recommended operating conditions: $T_A$ = -40℃ to +85℃, $V_{CC}$ = +2.5V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note2.

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency, SCL | | 1 | MHz |
| $t_{LOW}$ | Clock Pulse Width Low | 500 | | Ns |
| $t_{HIGH}$ | Clock Pulse width High | 320 | | Ns |
| $t_j$[1] | Noise Suppression Time | | 80 | Ns |
| $T_{AA}$ | Clock Low to Data Out Valid | | 450 | Ns |
| $t_{BUF}$[1] | Time the bus must be free before a new transmission can Start | 500 | | Ns |
| $t_{HD.STA}$ | Start Hold Time | 250 | | Ns |
| $t_{SU.STA}$ | Start Setup Time | 250 | | Ns |
| $t_{HD.DAT}$ | Data In Hold Time | 0 | | Ns |
| $t_{SU.DAT}$ | Data In Setup Time | 50 | | Ns |
| $t_R$ | Input Rise Time[1] | | 120 | Ns |
| $t_F$ | Input Fall Time[1] | | 120 | Ns |
| $t_{SU.STO}$ | Stop Setup Time | 250 | | Ns |
| $t_{DH}$ | Data Out Hold Time | 100 | | Ns |
| $t_{WR}$ | Write Cycle Time | | 5 | Ms |
| Endurance[1] | 3.3V,25℃,Page Mode | 1,000,000 | | Write Cycles |

Notes 1. This parameter is characterized and not 100% tested.

2.AC measurement conditions:

RL (connects to Vcc): 1.3kΩ

Input pulse voltages: 0.3 Vcc to 0.7 Vcc

Input rise and fall times: ≦50 ns

Input and output timing reference voltages: 0.5Vcc

## Device Operation

### Clock and Data Transitions:

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 4).Data changes during SCL high periods will indicate a start or stop condition as defined below.

### Start Condition:

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 5).

**Stop Condition:**

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

**Acknowledge:**

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

**Standby Mode :**

The ACE24C512D features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

**Memory Reset :**

After an interruption in protocol power loss or system reset, any two-wire part can be protocol reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high and then.
3. Create a start condition as SDA is high.

## Bus Timing

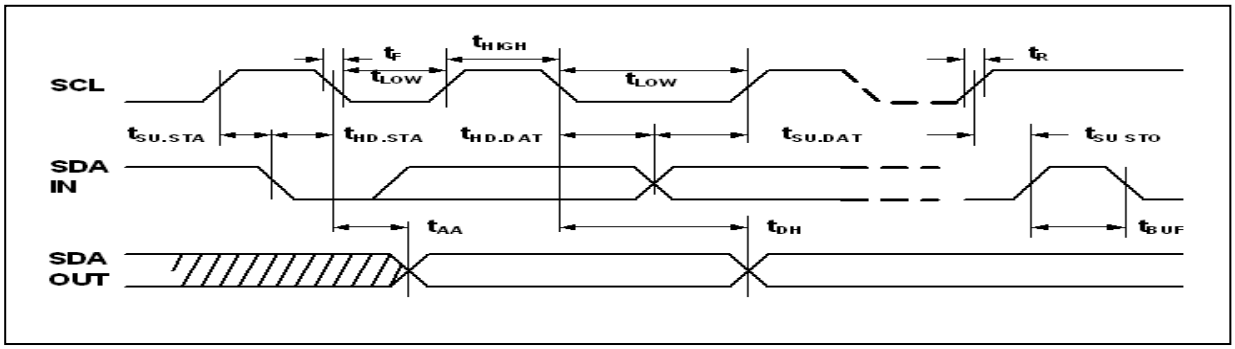



Figure 2 · SCL: Serial Clock, SDA: Serial Data I/O

## Write Cycle Timing

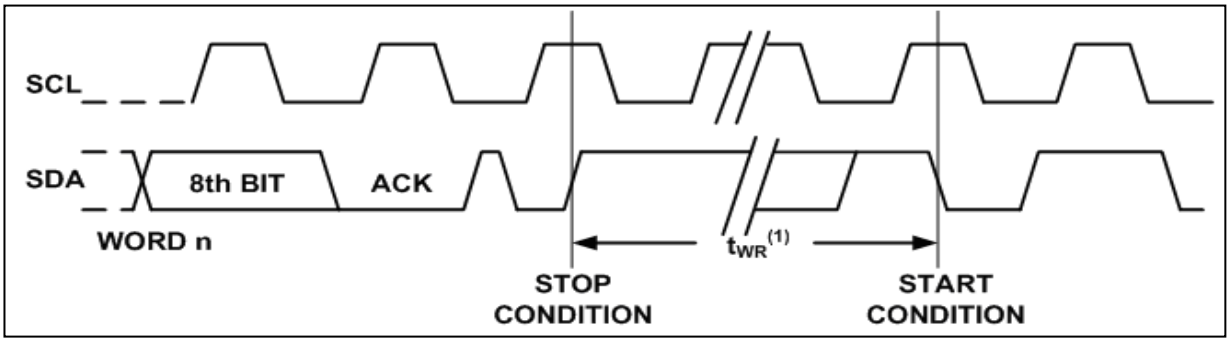



Figure 3. SCL: Serial Clock, SDA: Serial Data I/O

Note: The write cycle time $t_{WR}$ is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

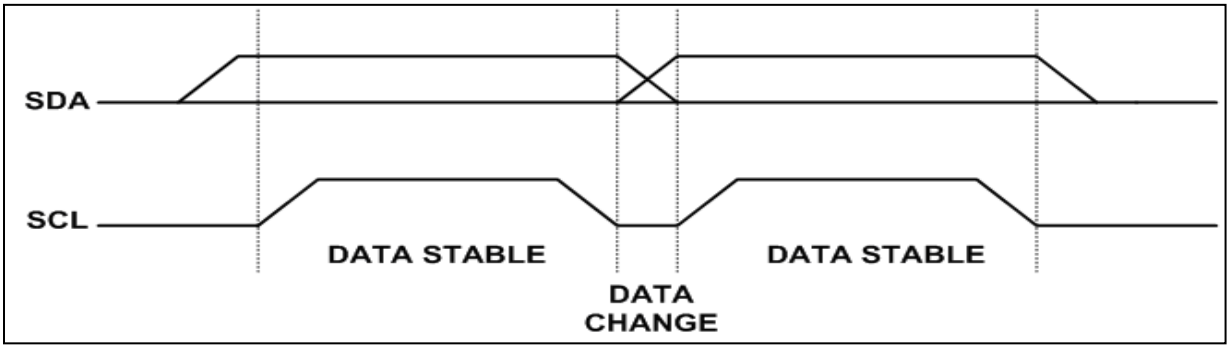



Figure 4 · Data Validity

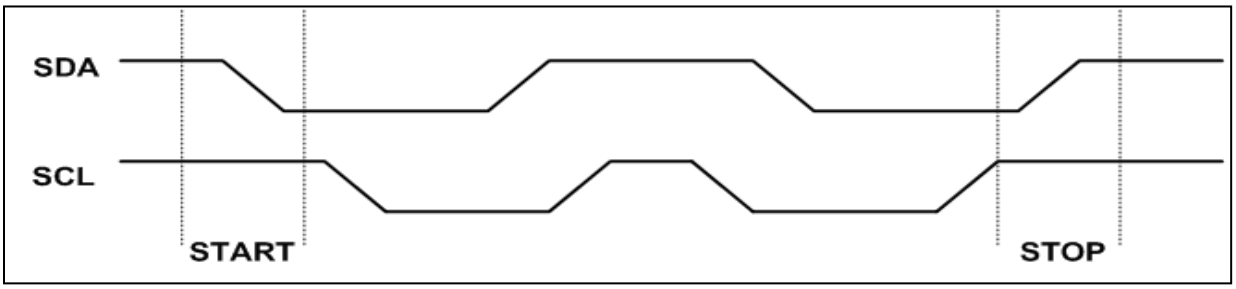



Figure 5 · Start and Stop Definition

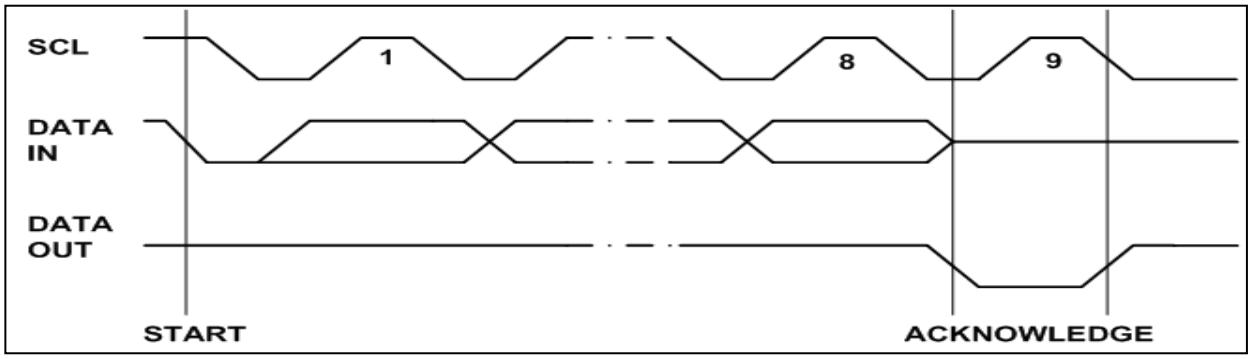



Figure 6 · Output Acknowledge

## Device Addressing

Data Memory Access: The 512K EEPROM device require an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1).

The device address word consists of a mandatory “1010”(Ah) sequence for the first four most significant bits as shown in Table 1 . This is common to all the EEPROM devices.

The 512K EEPROM uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hard-wired input pins. The A2,A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The Module package device address word also consists of a mandatory “1010”(Ah) sequence for the first four most significant bits. The next 3 bits are all zero.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

## Unique ID Access

The ACE24C512D utilizes a separate memory block containing a factory programmed 128-bit unique ID. Access to this memory location is obtained by beginning the device address word with a “1010”(Bh) sequence(refer to Table 1). The behavior of the next three bits(A2,A1 and A0) remains the same as during a standard memory addressing sequence.

The eighth bit of the device address needs be set to a one to read the Serial Number. Writing or altering the 128-bit unique ID is not possible.

For more details on accessing this special feature See Read Operations on page 14.

## Security Sector Access

The ACE24C512D offers 128-byte Security Sector which can be written and (later) permanently locked in Read-only mode. Access to this memory location is obtained by beginning the device address word with a “1010”(Bh) sequence(refer to Table 1). The behavior of the next three bits(A2,A1 and A0) remains the same as during a standard memory addressing sequence.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low

For more details on accessing this special feature, See Write Operations and Read Operations on page 13, 14.

**Noise protection:**

Special internal circuitry place on the SDA and SCL pins prevent small noise spikes from activating the device.

**Date Security:**

The Device has a hardware data protect scheme that allows the user to write protect the entire memory when the WP pin is at Vcc.

| Access Area | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Data Memory | 1 | 0 | 1 | 0 | A2 | A1 | A0 | R/W |
| Security Sector | 1 | 0 | 1 | 1 | A2 | A1 | A0 | R/W |
| Security Sector Lock Bit | 1 | 0 | 1 | 1 | A2 | A1 | A0 | R/W |
| Unique ID Number | 1 | 0 | 1 | 1 | A2 | A1 | A0 | 1 |
| | MSB | | | | | | | LSB |

Table 1-1. Device Address

| Access Area | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Data Memory | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |
| Security Sector | X | X | X | X | X | 0 | 0 | X |
| Security Sector Lock Bit | X | X | X | X | X | 1 | 0 | X |
| Unique ID Number | X | X | X | X | X | X | 1 | X |
| | MSB | | | | | | | LSB |

NOTE: x = Don't care bit

Table 1-2. First Word Address

| Access Area | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Data Memory | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Security Sector | X | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Security Sector Lock Bit | X | X | X | X | X | X | X | X |
| Unique ID Number | X | X | X | X | 0 | 0 | 0 | 0 |
| | MSB | | | | | | | LSB |

NOTE: x = Don't care bit

Table 1-3. Second Word Address

## Write Operations

### Byte Write:

A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure7 on page 15).

### Page Write:

The 512K EEPROM is capable of an 128-byte page write.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 127 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure8 on page 15).

The data word address lower 7 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 128 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

**Acknowledge Polling:**

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

**Write Security Sector:**

Write the Security Sector is similar to the page write but requires use of device address, and the special word address, and the special word address seen in Table 1 on page 12.The higher address bits ADDR<15:7> are don't care except for address bits ADDR<10:9>,which must be equal to'00b'. Lower address bits ADDR<6:0> define the byte address inside the Security Sector (see Figure 12 on page 16).

If the Security Sector is locked, the data bytes transferred during the Write Security Sector operation are not acknowledged (NoAck).

## Lock Security Sector

Lock the Security Sector is similar to the byte write but requires use of device address, and special word address seen in Table 1 on page 12. The word address bits ADDR<10:9> must be '10b', all other word address bits are don't care. The data byte must be equal to the binary value xxxx xx1x, where x is don' care (see Figure 14 on page 17).

If the Security Sector is locked, the data bytes transferred during the Lock Security Sector operation are not acknowledged (NoAck).

## Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

**Current Address Read:**

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure9 on page 15).

**Random Read:**

A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure10 on page 16).

**Sequential Read:**

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure11 on page 16).

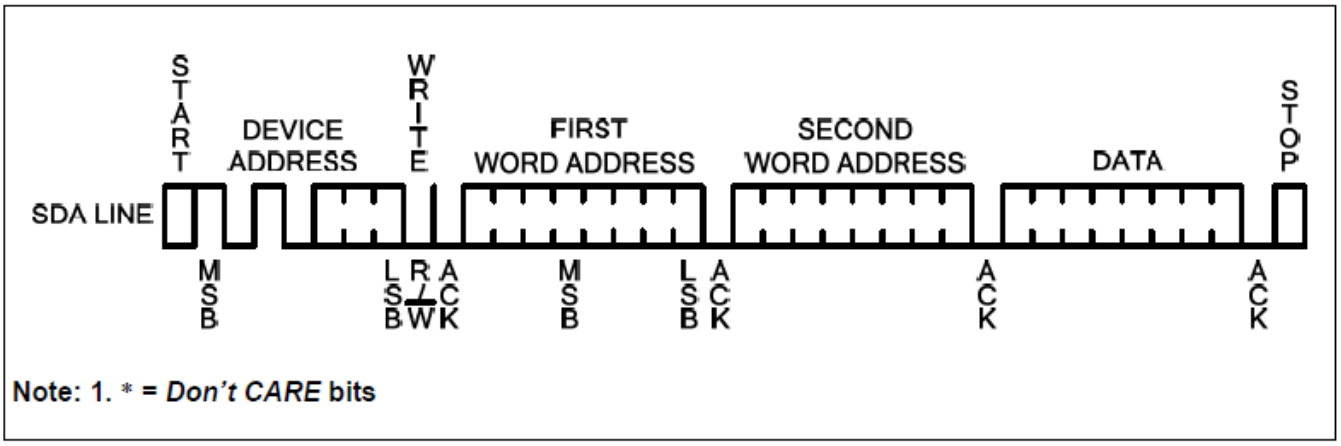



Figure 7 · Byte Write

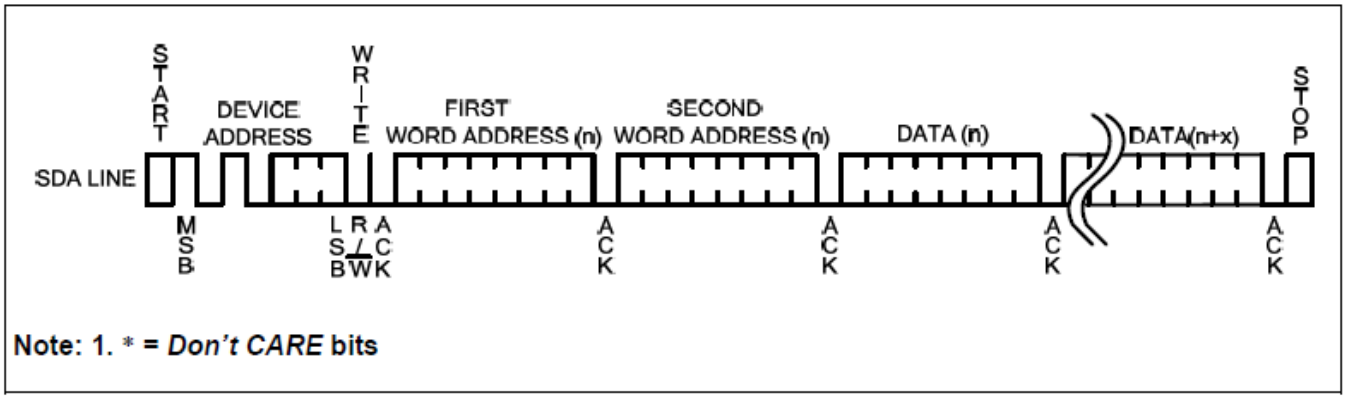



Figure 8 · Page Write

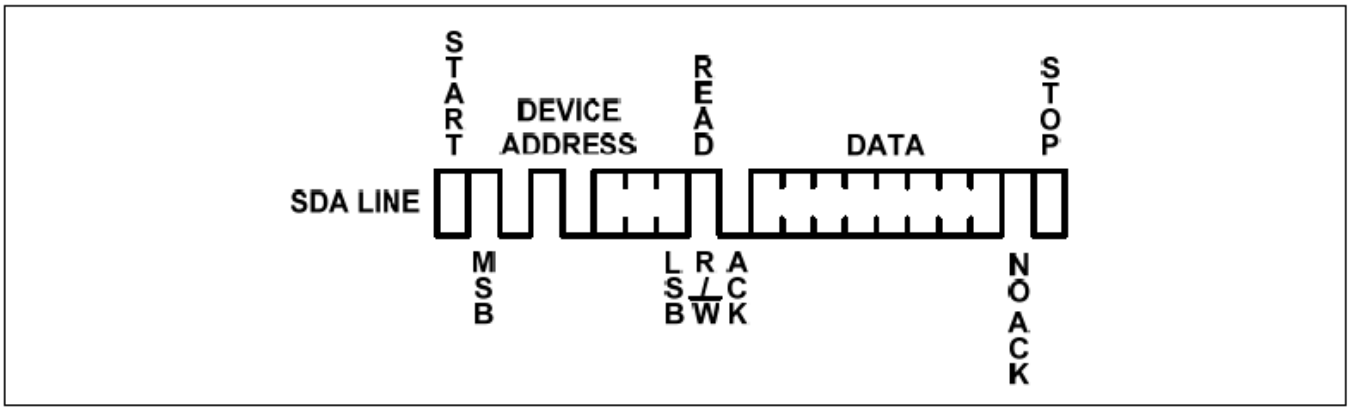



Figure 9 · Current Address Read

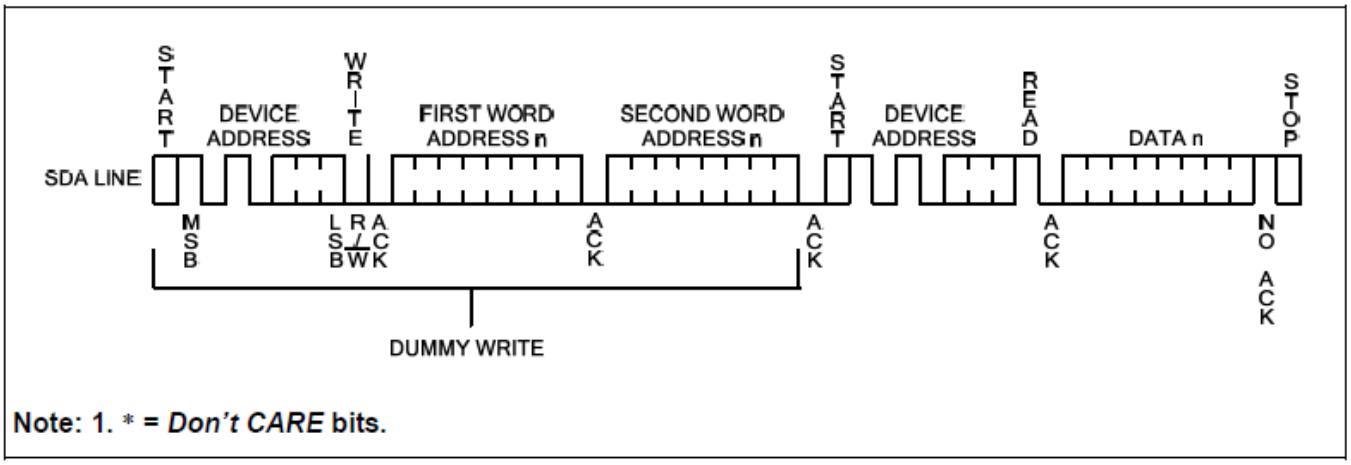



Figure 10 · Random Read

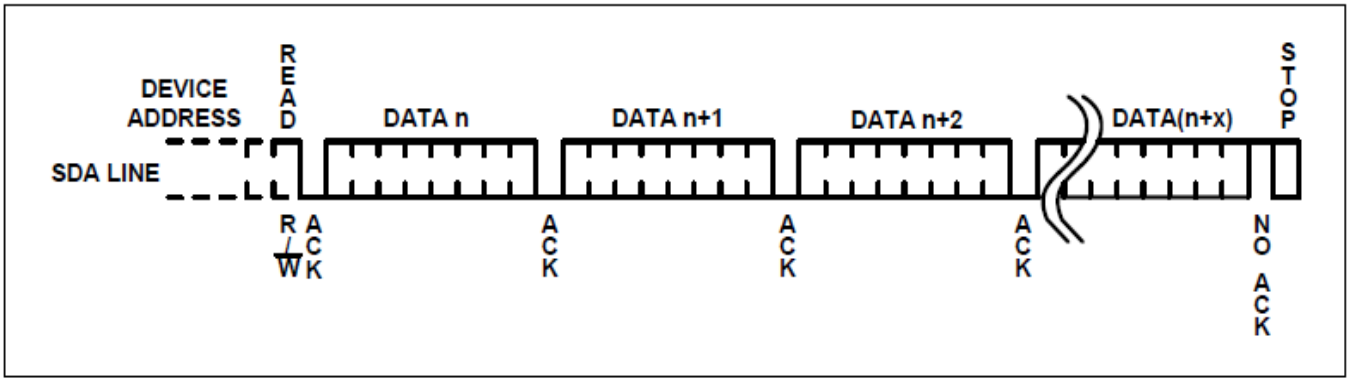



Figure 11 · Sequentia Read

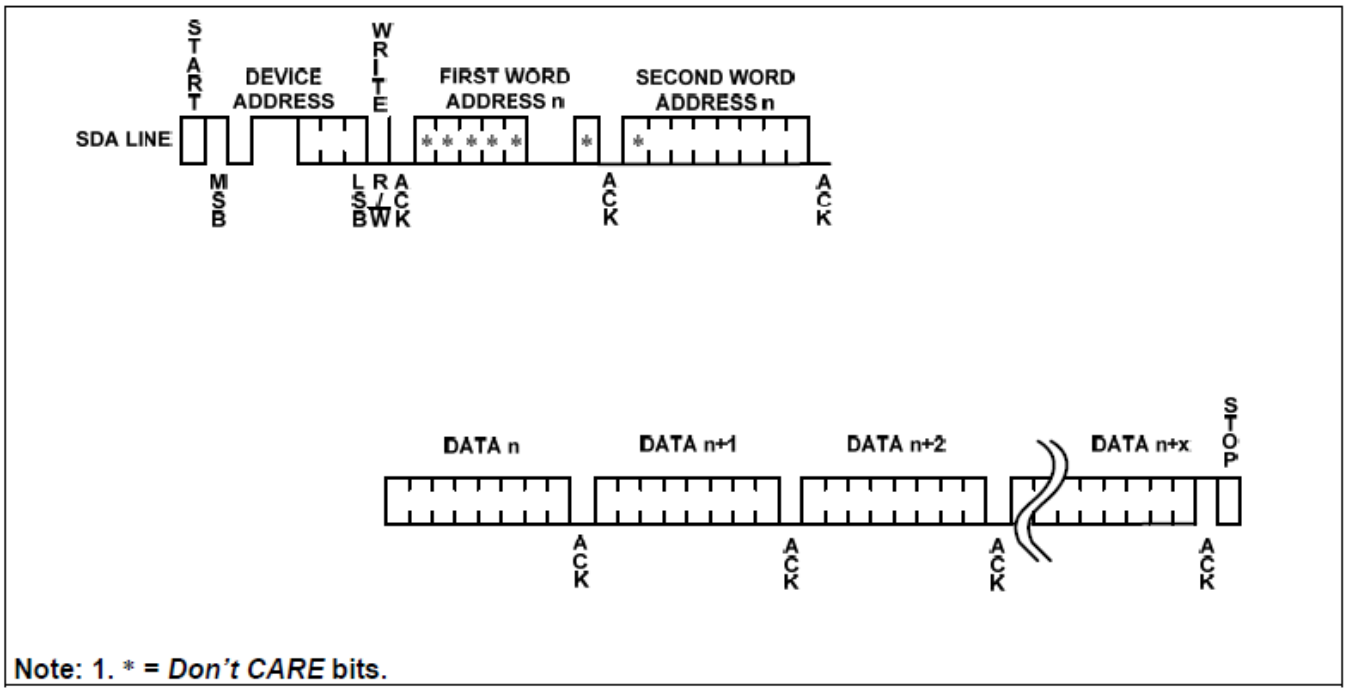



Figure 12 · Write Security Sector

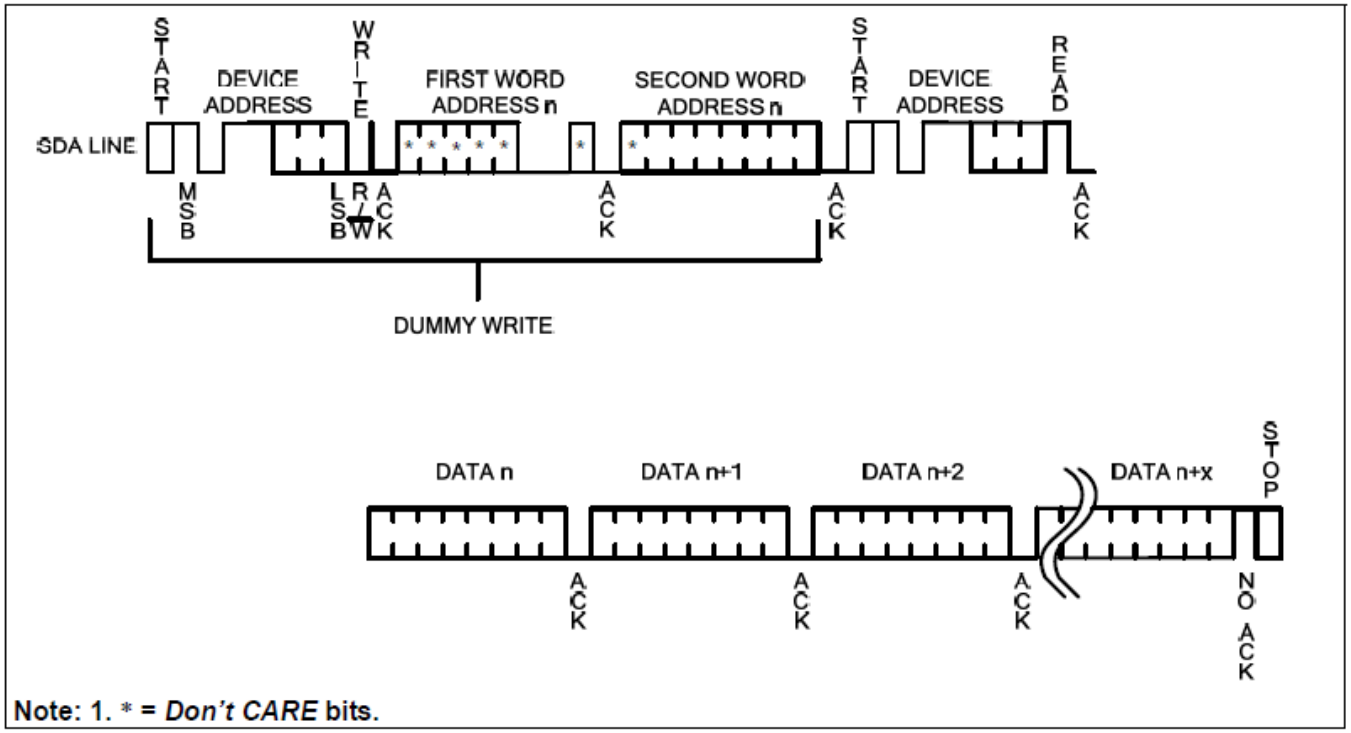



Figure 13 · Read Security sector

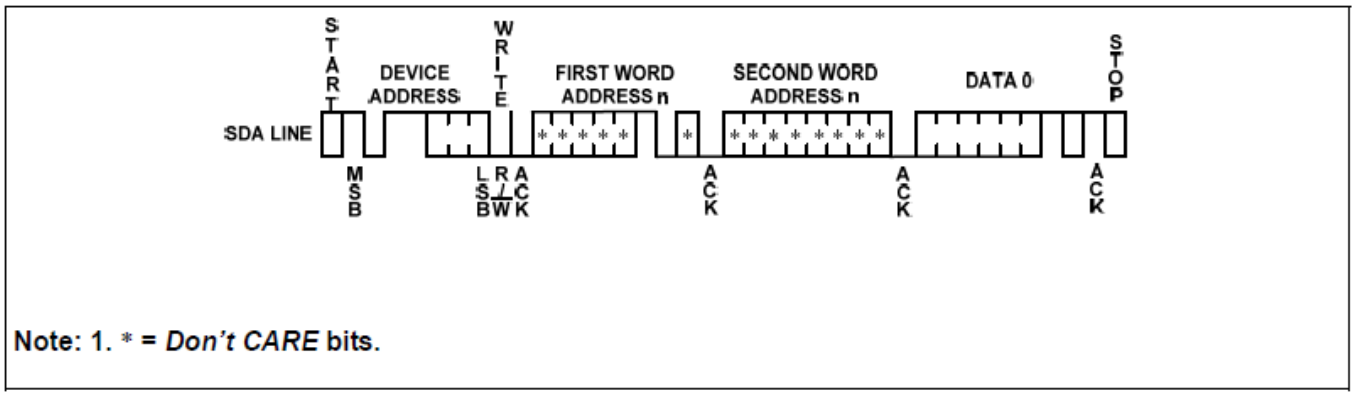



Figure 14 · Lock Security Sector

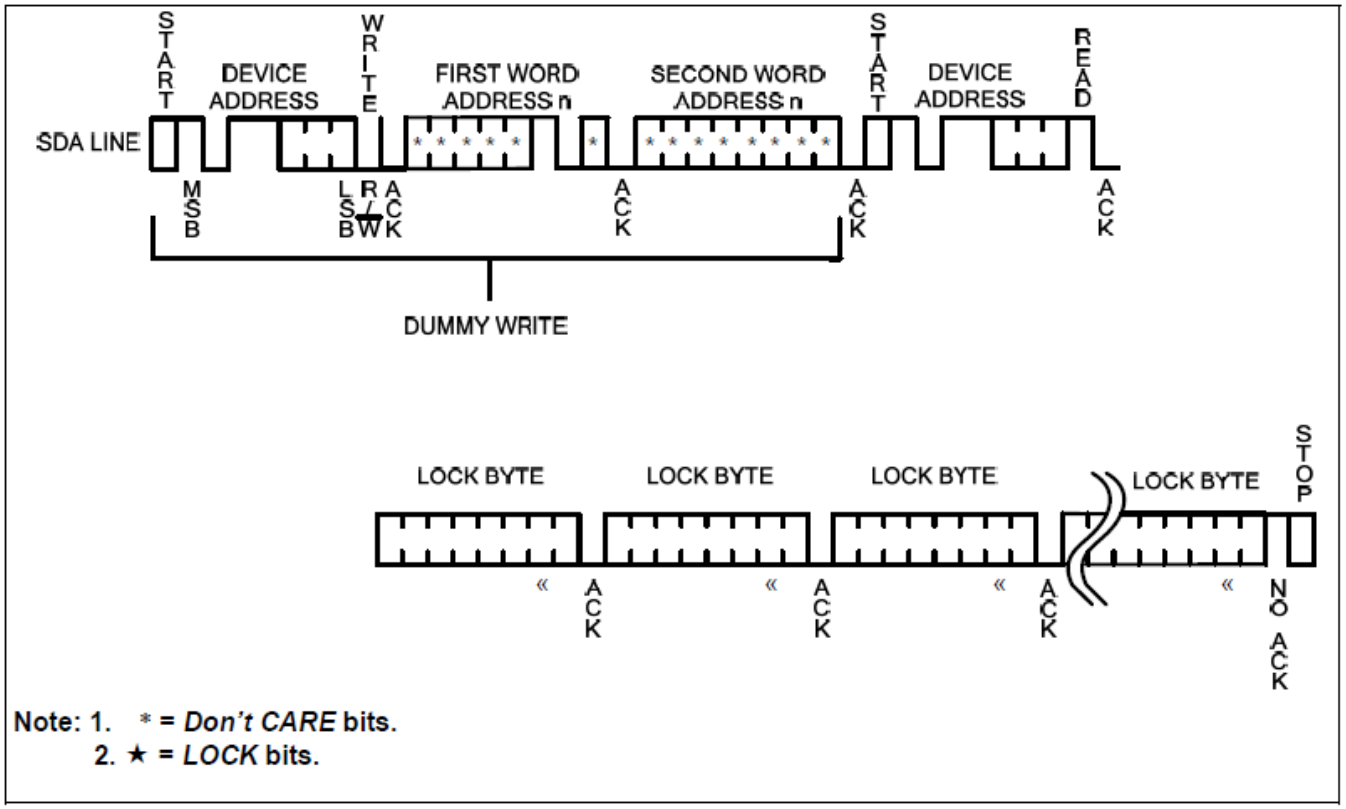



Figure 15 · Read Lock Status

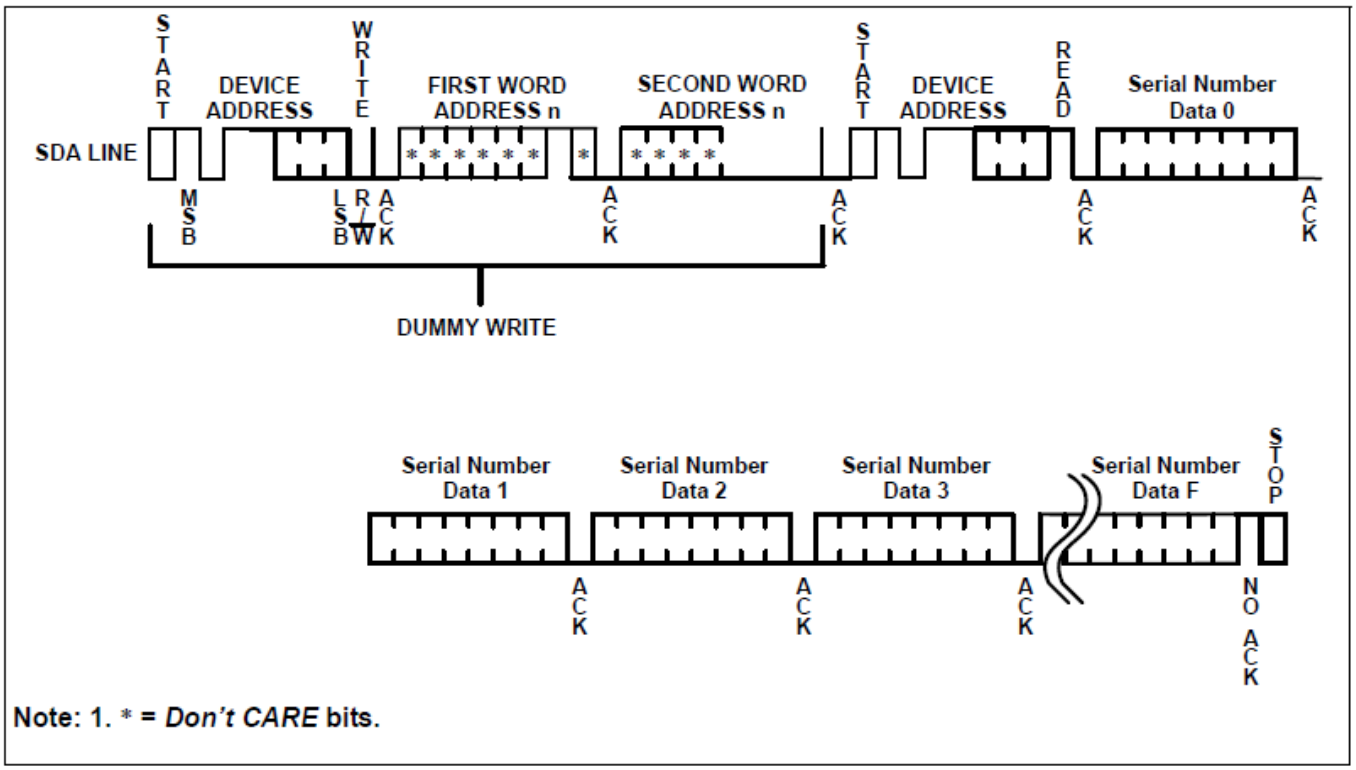
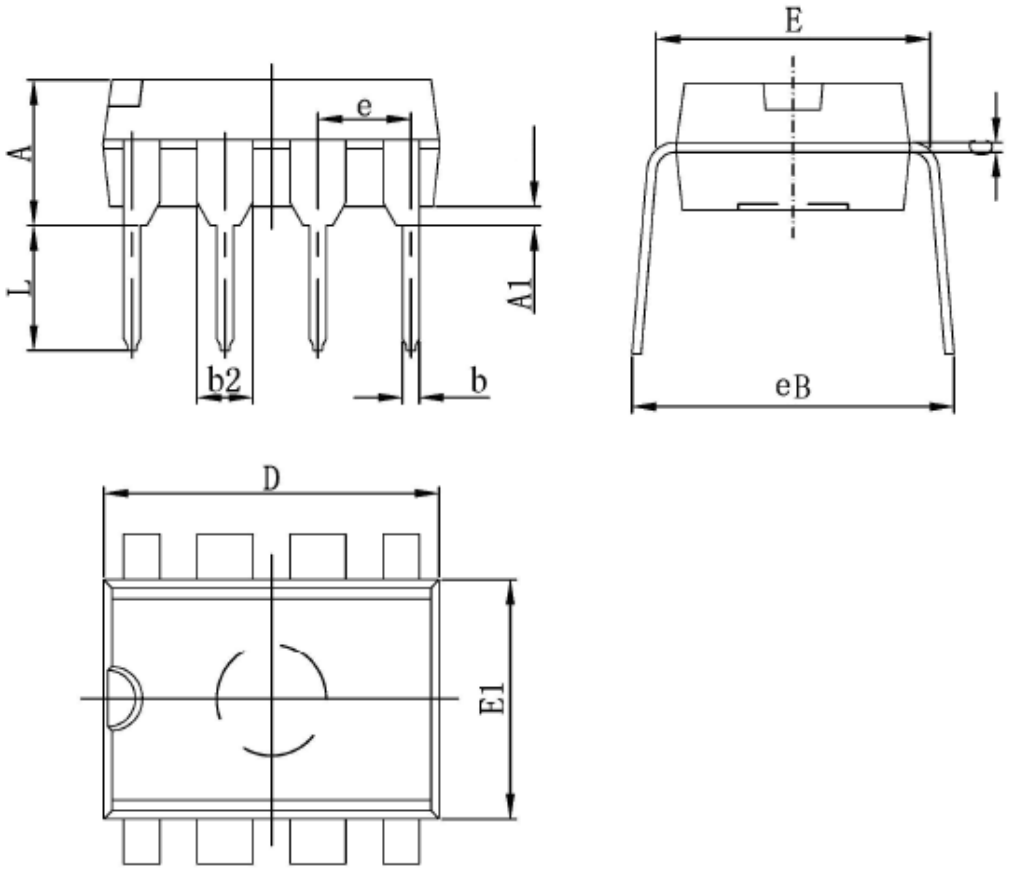



Figure 16 · Read Unique ID

## Packaging information

### DIP-8

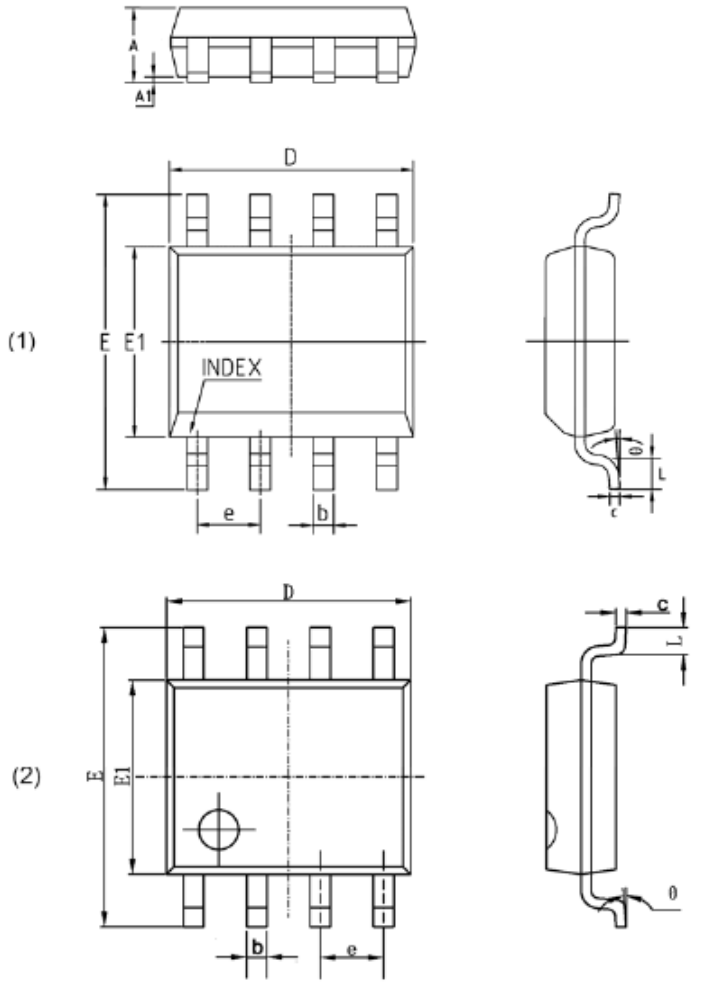



| Symbol | MIN | MAX |
|---|---|---|
| A | --- | 5.000 |
| A1 | 0.380 | --- |
| b | 0.380 | 0.570 |
| b2 | 1.300 | 1.700 |
| C | 0.200 | 0.360 |
| D | 9.000 | 10.000 |
| E1 | 6.100 | 7.000 |
| E | 7.320 | 8.250 |
| e | 2.540(BSC) | |
| L | 2.920 | 3.810 |
| eB | --- | 10.900 |

NOTE:
1. Dimensions are in Millimeters.

## Packaging information

### SOP-8

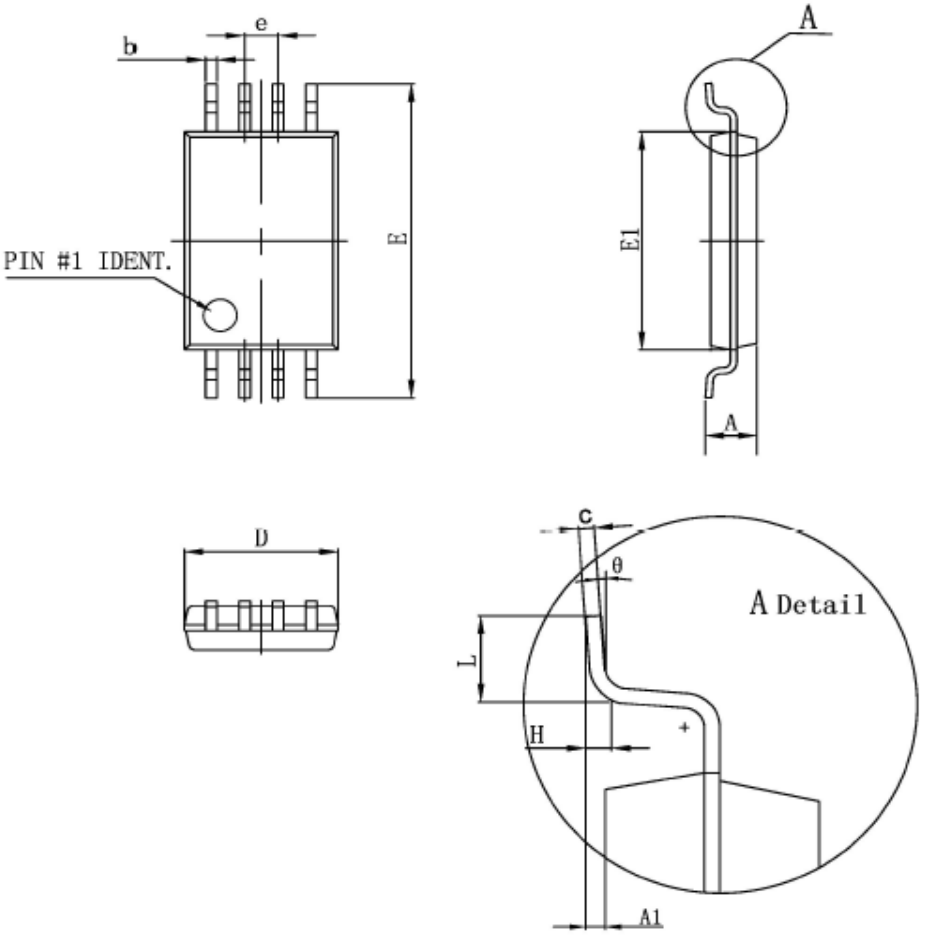



| Symbol | MIN | MAX |
|---|---|---|
| A | 1.350 | 1.750 |
| A1 | 0.050 | 0.250 |
| b | 0.330 | 0.510 |
| c | 0.150 | 0.250 |
| D | 4.700 | 5.150 |
| E1 | 3.800 | 4.000 |
| E | 5.800 | 6.200 |
| e | 1.270(BSC) | |
| L | 0.400 | 1.270 |
| θ | 0° | 8° |

NOTE:
1. Dimensions are in Millimeters.

## Packaging information

### TSSOP-8

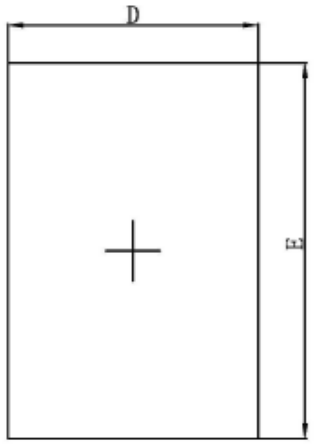



| Symbol | MIN | MAX |
|---|---|---|
| D | 2.900 | 3.100 |
| E1 | 4.300 | 4.500 |
| b | 0.190 | 0.300 |
| c | 0.090 | 0.200 |
| E | 6.250 | 6.550 |
| A | | 1.200 |
| A1 | 0.050 | 0.150 |
| e | 0.650 (BSC) | |
| L | 0.450 | 0.750 |
| θ | 0° | 8° |

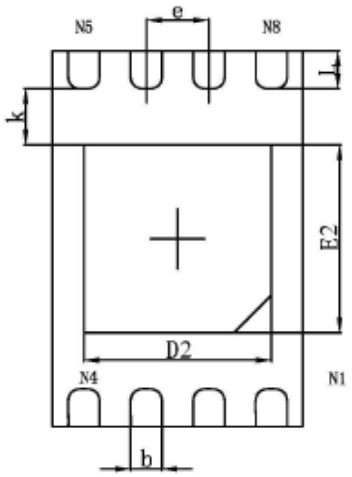
NOTE:
1. Dimensions are in Millimeters. Notes

## Packaging information

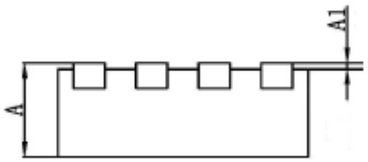
### TDFN-8




Top View




Bottom View




Side View

| Symbol | MIN | MAX |
|---|---|---|
| A | 0.700 | 0.800 |
| A1 | 0.000 | 0.050 |
| D | 1.900 | 2.100 |
| E | 2.900 | 3.100 |
| D2 | 1.400 | 1.600 |
| E2 | 1.400 | 1.600 |
| k | 0.200(MIN) | |
| b | 0.200 | 0.300 |
| e | 0.500(TYP) | |
| L | 0.200 | 0.400 |

NOTE:
1. Dimensions are in Millimeters.

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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