

#### **Description**

The ACE2303 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and Battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

#### **Features**

- -30V/-2.6A,  $R_{DS(ON)}$ =130m $\Omega$ @ $V_{GS}$ =-10V
- -30V/-2.0A,  $R_{DS(ON)}$ =180m $\Omega$ @ $V_{GS}$ =-4.5V
- Super high density cell design for extremely low R<sub>DS(ON)</sub>
- Exceptional on-resistance and maximum DC current capability

#### **Application**

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

#### **Absolute Maximum Ratings**

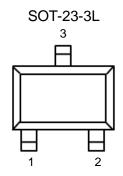
 $(T_A=25^{\circ}C$  Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	$V_{DSS}$	-30	٧
Gate-Source Voltage	$V_{GSS}$	±20	V
Continuous Drain Current (T <sub>J</sub> =150°C)		-3.0	Α
T <sub>A</sub> =70°C	l I <sub>D</sub>	-2.0	
Pulsed Drain Current	I <sub>DM</sub>	-10	Α
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	-1.25	Α
Power Dissipation T <sub>A</sub> =25°C	P <sub>D</sub>	1.25	W
Power Dissipation T <sub>A</sub> =70°C	' D	8.0	VV
Operating Junction Temperature	$T_J$	150	$^{\circ}$
Storage Temperature Range	T <sub>STG</sub>	-55/150	$^{\circ}\!\mathbb{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	100	$^{\circ}$ C/W

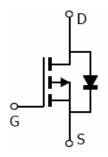




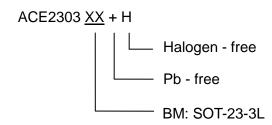
# **Packaging Type**



SOT-23-3L	Description		
1	Gate		
2	Source		
3	Drain		



# **Ordering information**



### **Electrical Characteristics**

(T<sub>A</sub>=25°C, Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Тур	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V <sub>GS</sub> =0V, I <sub>D</sub> =-10uA	-30			v	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=-250uA$	-1.0		-3.0	V	
Gate Leakage Current	I <sub>GSS</sub>	$V_{DS}$ =0.V, $V_{GS}$ =±20V			±100	nA	
Zava Cata Valtaga Dvain Current	I <sub>DSS</sub>	$V_{DS}$ =-30V, $V_{GS}$ =0V			-1		
Zero Gate Voltage Drain Current		V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-10	uA	
On-State Drain Current	I <sub>D(ON)</sub>	$V_{DS}$ $\leq$ -5V, $V_{GS}$ = -10V	-6			Α	
Desir Course On Basistan	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-2.6A		0.095	0.130		
Drain-Source On-Resistance		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-2.0A		0.125	0.180	Ω	
Forward Transconductance	gfs	V <sub>DS</sub> =-10V, I <sub>D</sub> =-1.7A	/ <sub>DS</sub> =-10V, I <sub>D</sub> =-1.7A			S	
Diode Forward Voltage	$V_{SD}$	I <sub>S</sub> =-1.25A, V <sub>GS</sub> =0V		-0.8	-1.2	V	
Dynamic							
Total Gate Charge	$Q_g$	15)/ 15)/ 10)/		5.8	10		
Gate-Source Charge	$Q_{gs}$	$V_{DS}$ =-15V, $V_{GS}$ =-10V, $I_{D}$ $\equiv$ -1.7A		0.8		nC	
Gate-Drain Charge	$Q_{gd}$	ID=-1./A		1.5			
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V,		226		55	
Output Capacitance	C <sub>oss</sub>	f=1MHz		87		pF	



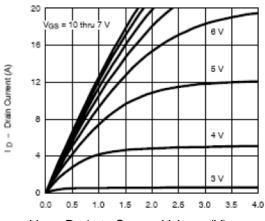
# **ACE2303**

### **P-Channel Enhancement Mode MOSFET**

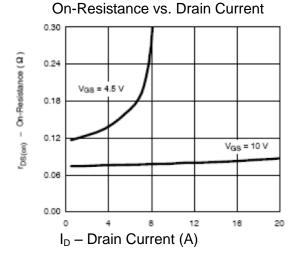
	Reverse Transfer Capacitance	$C_{rss}$		19			
	Turn On Time	t <sub>d(on)</sub>		9	20		
	Turn-On Time	t <sub>r</sub>	$V_{DD}$ =-15V, $R_L$ =15 $\Omega$	9	20	no	
	Turn Off Time o	t <sub>d(off)</sub>	$I_D$ =-1.0A, $V_{GEN}$ =-10V $R_G$ =6 $\Omega$	18	35	ns	
Turn-Off Time	t <sub>f</sub>	NG-032	6	20	i		

## **Typical Characteristics**

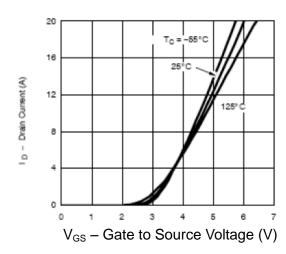
## **Output Characteristics**



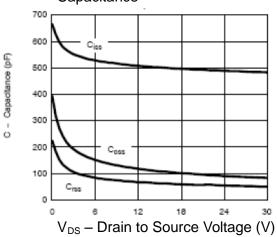
 $V_{\text{DS}}$  – Drain to Source Voltage (V)



#### **Transfer Characteristics**







3



# **ACE2303**

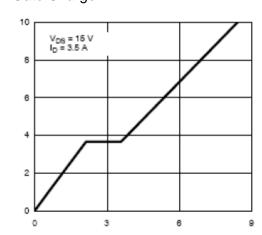
#### P-Channel Enhancement Mode MOSFET

## **Typical Characteristics**

### Gate Charge

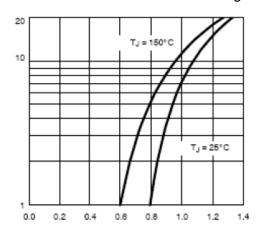
V<sub>GS</sub> - Gate-to-Source Voltage (V)

Is - Source Current (A)



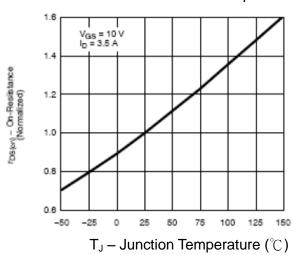
O<sub>q</sub> Total Gate Charge (nC)

### Source-Drain Diode Forward Voltage

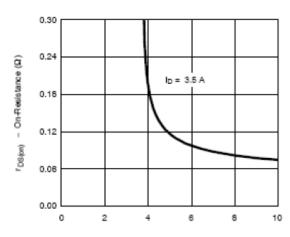


V<sub>SD</sub> Source to Drain Voltage (V)

#### On-Resistance vs. Junction Temperature



### On-Resistance vs. Gate-to-Source Voltage



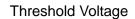
V<sub>GS</sub> - Gate to Source Voltage (V)

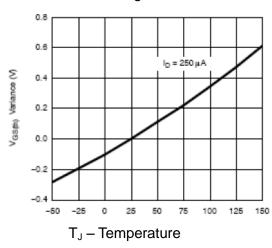
4



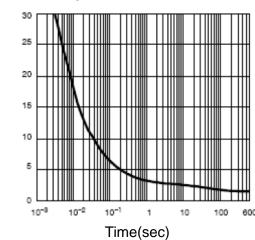


## **Typical Characteristics**

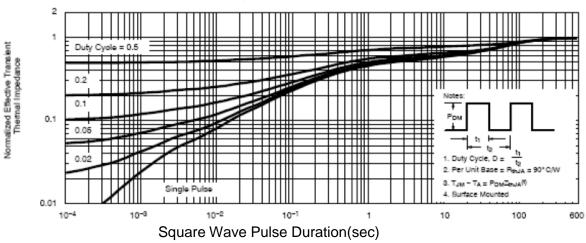




# Single Pulse Power



## Normalized Thermal Transient Impedance, Junction-to-Ambient

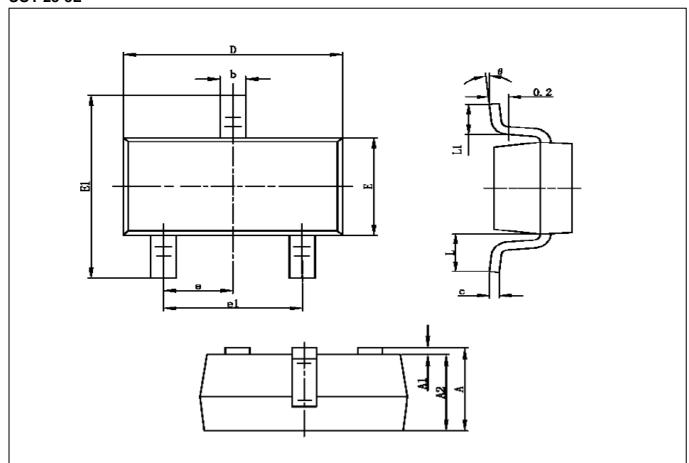


Power (W)



# **Packing Information**

## SOT-23-3L



Cambal	Dimensions	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	1.050	1.250	0.041	0.049	
A1	0.000	0.100	0.000	0.004	
A2	1.050	1.150	0.041	0.045	
b	0.300	0.400	0.012	0.016	
С	0.100	0.200	0.004	0.008	
D	2.820	3.020	0.111	0.119	
E	1.500	1.700	0.059	0.067	
E1	2.650	2.950	0.104	0.116	
е	0.950TYP		0.037TYP		
e1	1.800	2.000	0.071	0.079	
L	0.700	REF	0.028REF		
L1	0.300	0.600	0.012	0.024	
θ	0°	8°	0°	8°	



## **ACE2303**

#### P-Channel Enhancement Mode MOSFET

#### Notes

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- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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