



ACE6428B

N-Channel Enhancement Mode Field Effect Transistor

Description

The ACE6428B uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. This device is suitable for use as a high side switch in SMPS and general purpose applications.

Features

- $V_{DS}(V)=30V$
- $I_D=43A (V_{GS}=10V)$
- $R_{DS(ON)} < 10m\Omega (V_{GS}=10V)$
- $R_{DS(ON)} < 14.5m\Omega (V_{GS}=4.5V)$
- 100% Delta Vsd Tested
- 100% Rg Tested

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current (Continuous)	$T_A=25^\circ C$	43	A
	$T_A=100^\circ C$	27	
Drain Current (Pulse) ^C	I_{DM}	80	
Drain Current (Continuous)	$T_A=25^\circ C$	11	A
	$T_A=70^\circ C$	8	
Power Dissipation ^B	$T_A=25^\circ C$	30	W
	$T_A=100^\circ C$	12	
Power Dissipation ^A	$T_A=25^\circ C$	2	W
	$T_A=70^\circ C$	1.3	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

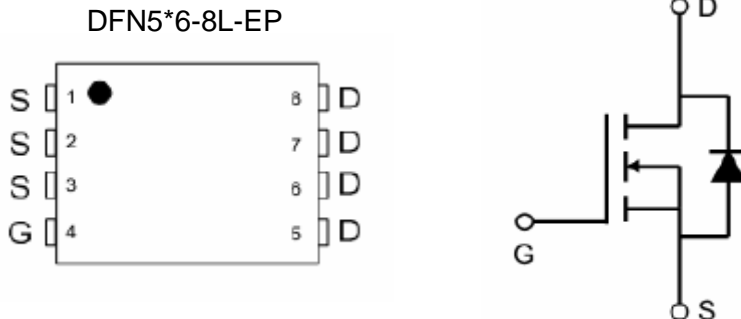
Thermal Characteristics					
Parameter	Symbol	Typ	Max	Units	
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	21	25	$^\circ C/W$	
Maximum Junction-to-Ambient ^{A,D}		Steady-State	50	60	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.5	4.2	$^\circ C/W$	



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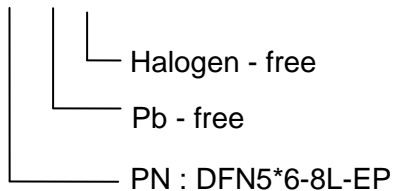
N-Channel Enhancement Mode Field Effect Transistor

Packaging Type



Ordering information

ACE6428B XX + H



Electrical Characteristics $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$			1	μA
Gate Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$		5.7	10	m Ω
		$V_{GS}=4.5V, I_D=20A$		7.9	14.5	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.2	1.9	2.5	V
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=15A$		25		S
Diode Forward Voltage	V_{SD}	$I_{SD}=2A, V_{GS}=0V$		0.71	1.0	V
Maximum Body-Diode Continuous Current	I_S				2	A
Switching						
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=20A$ $V_{GS}=5V$		16	20.8	nC
Gate-Source Charge	Q_{gs}			5	6.5	
Gate-Drain Charge	Q_{gd}			3	3.9	
Turn-On Delay Time	$T_{d(on)}$	$V_{DS}=15V, V_{GS}=10V$ $R_{GEN}=6\Omega, R_L=15\Omega$		17	34	ns
Turn-On Rise Time	t_f			5	10	
Turn-Off Delay Time	$t_{d(off)}$			50	100	
Turn-Off Fall Time	t_f			10	20	



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Dynamic				
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$	2470	pF
Output Capacitance	C_{oss}		325	
Reverse Transfer Capacitance	C_{rss}		185	

Note:

- A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}C$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of $150^{\circ}C$. The value in any given application depends on the user's specific board design.
- B. The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}C$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}C$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}C$.
- D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu s$ pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^{\circ}C$. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}C$

Typical Performance Characteristics

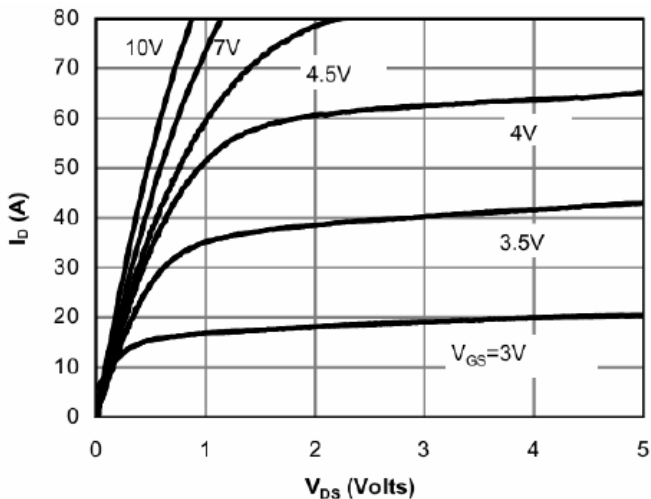


Fig 1: On-Region Characteristics (Note E)

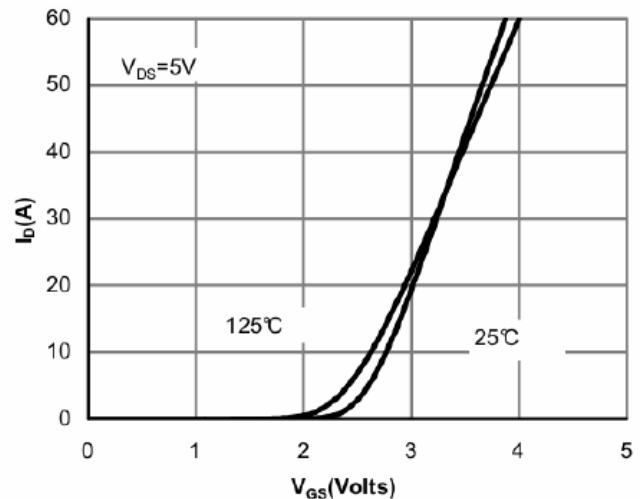


Figure 2: Transfer Characteristics (Note E)



Typical Performance Characteristics

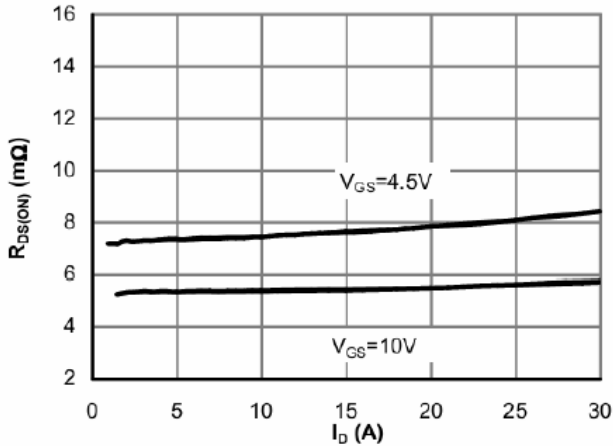


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

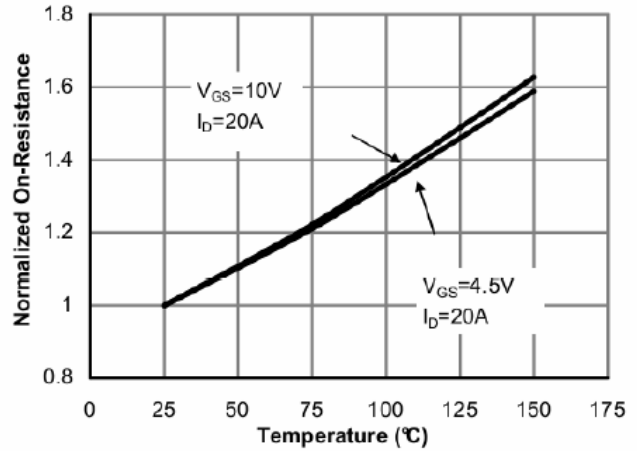


Figure 4: On-Resistance vs. Junction Temperature (Note E)

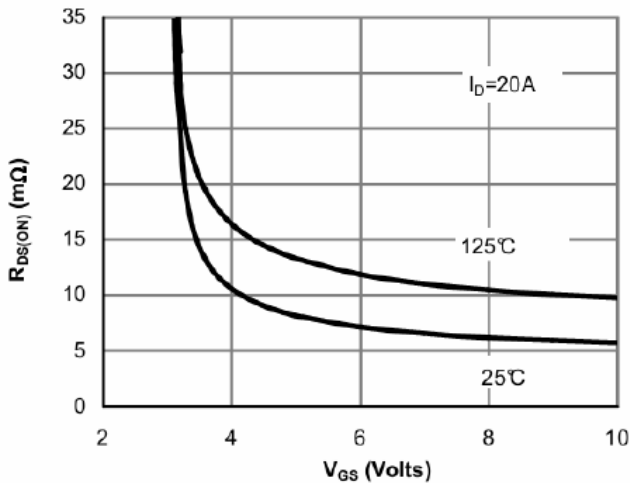


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

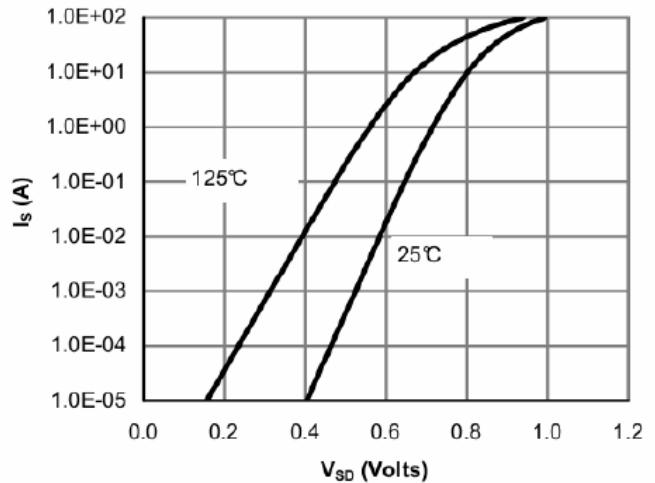


Figure 6: Body-Diode Characteristics (Note E)

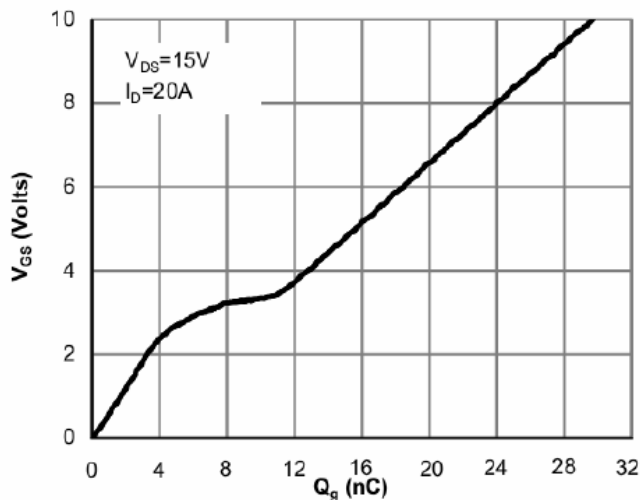


Figure 7: Gate-Charge Characteristics

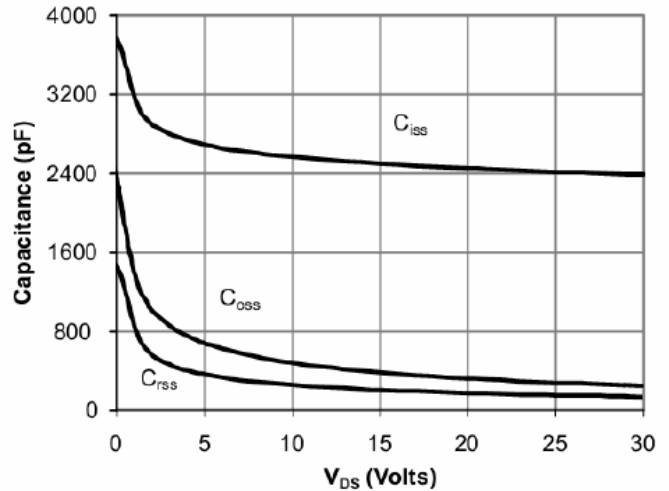


Figure 8: Capacitance Characteristics



Typical Performance Characteristics

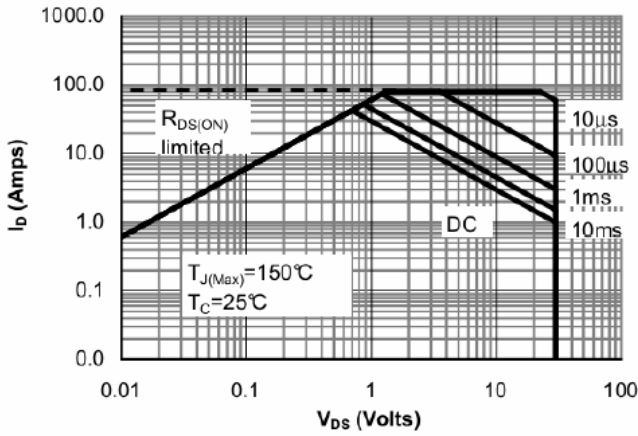


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

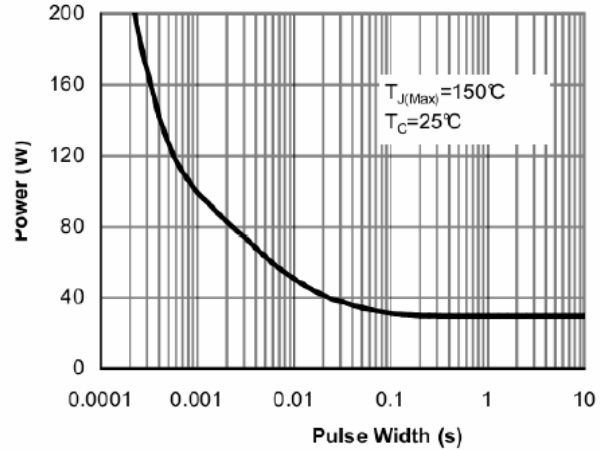


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

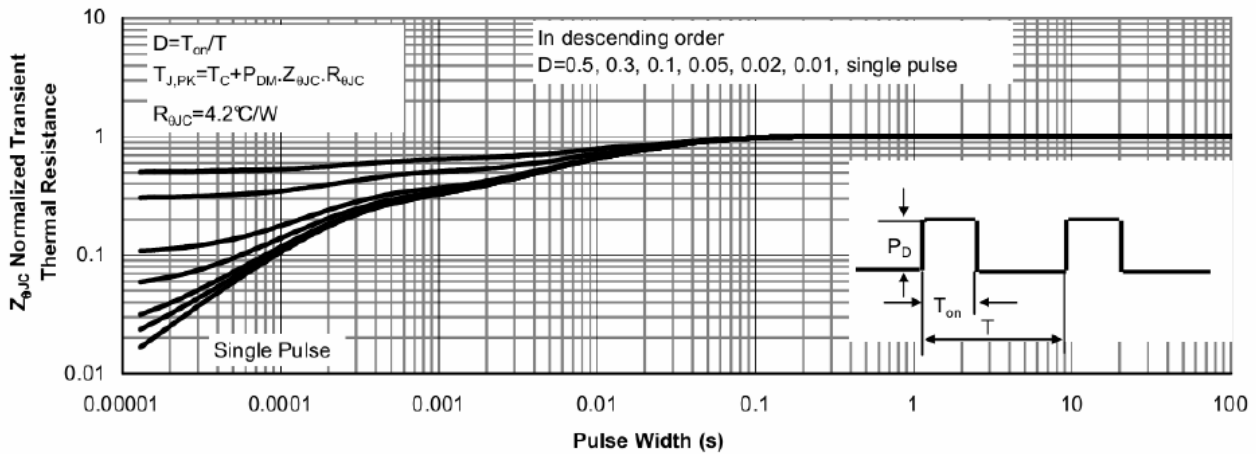


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

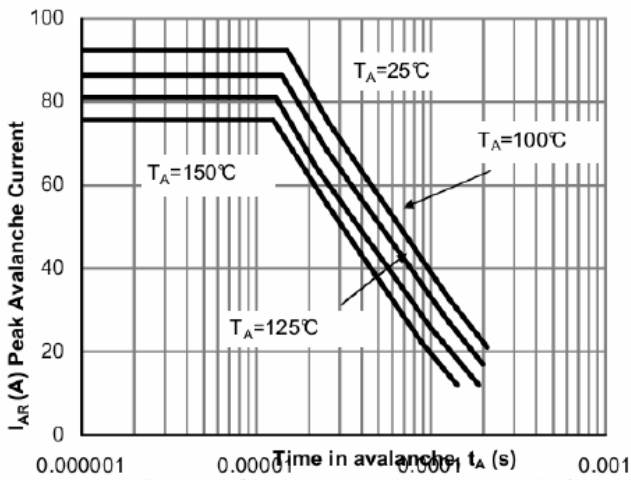


Figure 12: Single Pulse Avalanche capability (Note F)

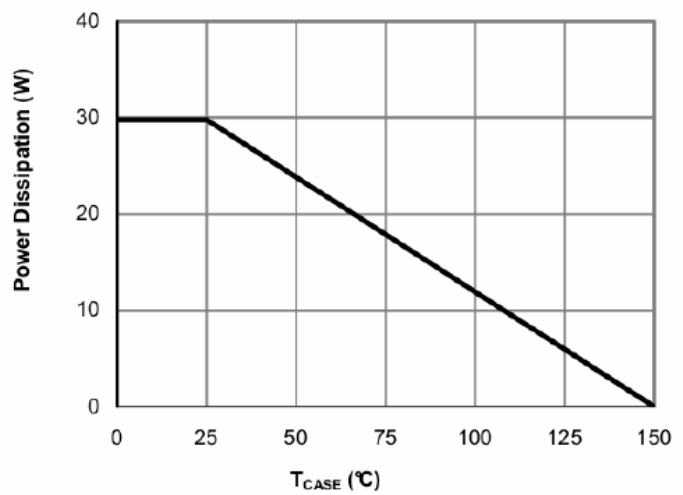


Figure 13: Power De-rating (Note F)



Typical Performance Characteristics

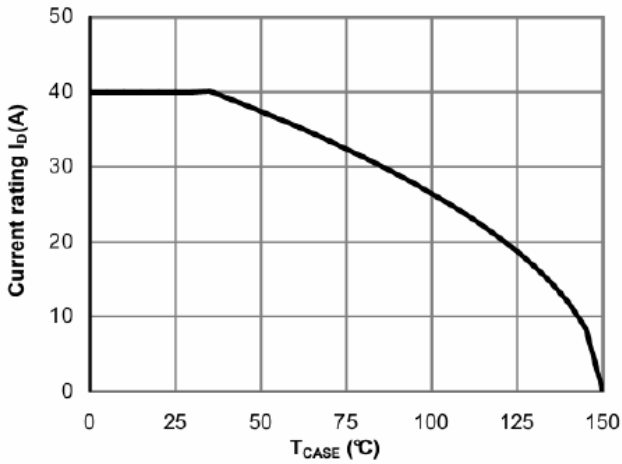


Figure 14: Current De-rating (Note F)

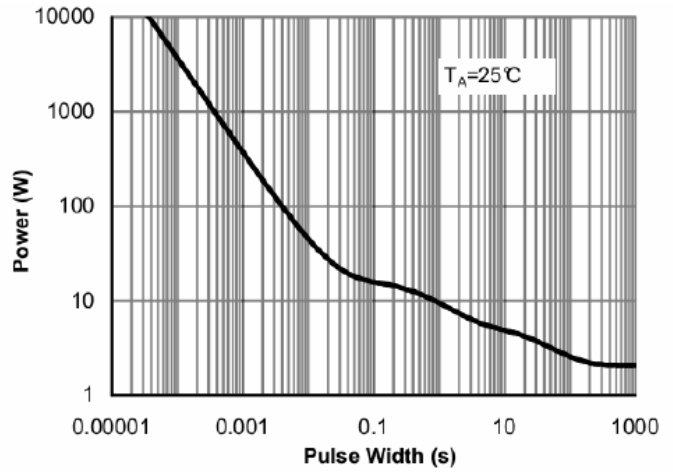


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

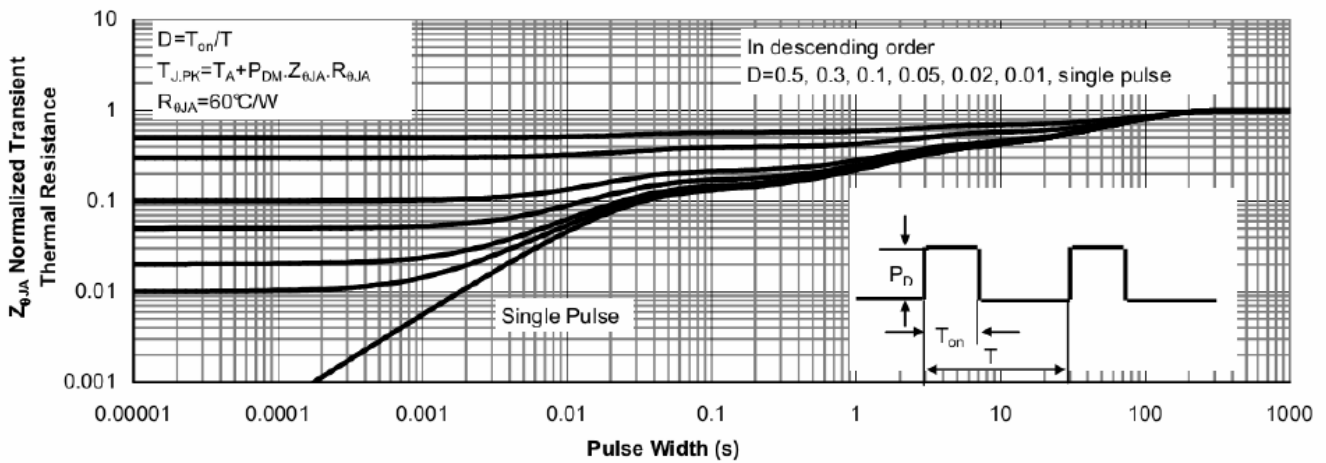


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

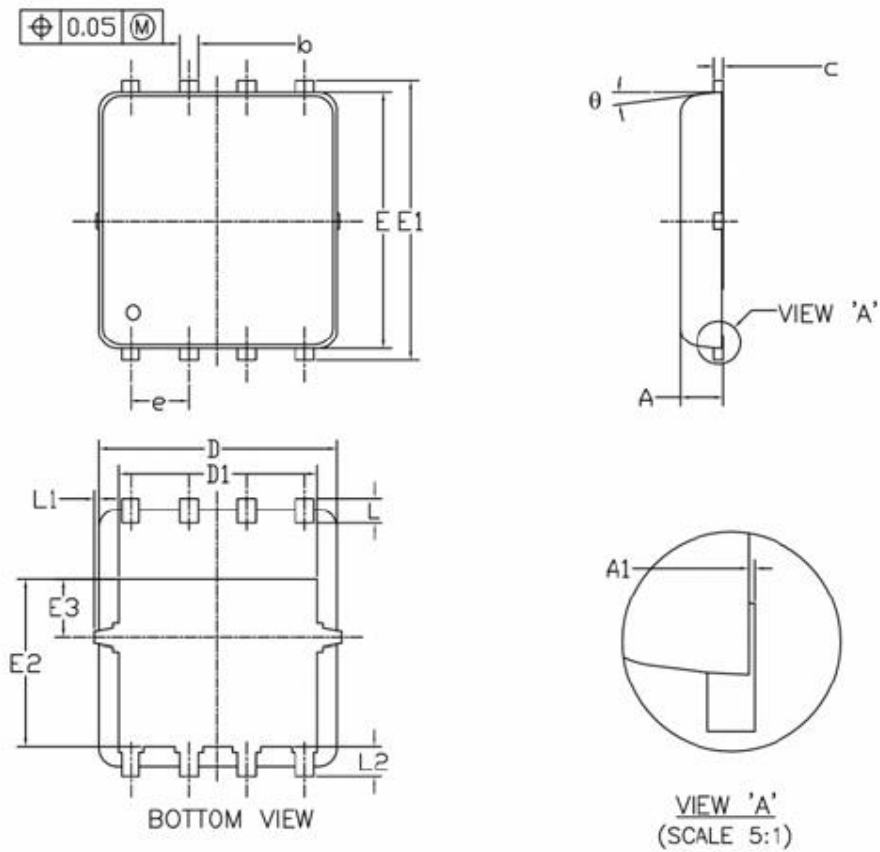


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Packing Information

DFN5*6-8L-EP



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	—	0.05	0.000	—	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC		
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	3.625 BSC			0.143 BSC		
E3	1.275 BSC			0.050 BSC		
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	—	0.15	0	—	0.006
L2	0.68 REF			0.027 REF		
θ	0°	—	10°	0°	—	10°



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Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD.

As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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