



ACE306A

Low Voltage Detector with Built-in Delay Circuit

Description

The ACE306A Series is a series of high-precision voltage detectors with a built-in delay time generator of fixed time. developed using CMOS process.

The detection voltage is fixed internally, with an accuracy of $\pm 2.0\%$. Internal oscillator and counter timer can delay the release signal without external parts, delay times 210 ms Two output forms, NMOS open-drain and CMOS output are available.

Features

- High-precision detection Voltage : $\pm 2\%$
- Detection Voltage : 1.5V~6.0V (10mV steps)
- Operating Voltage range : 0.95V~7.0V
- Ultra-low current consumption : 0.9 μ A@3.5V(Typ.)
- Two Output forms: CMOS and N-channel open-drain (Active Low)
- Hysteresis characteristics:-VDET*5%(Typ.)
- Delay time:210 ms(Typ.)

Application

- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- Power monitor for portable equipment such as notebook computers, digital cameras, PDA, and cellular phones.
- Constant voltage power monitors for cameras, video equipment and communication devices
- Power monitor for microcomputers and reset for CPUs

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Max	Unit
Power supply voltage(V _{DD})	V _{SS} -0.3 ~ V _{SS} +8	V
Output voltage(V _{OUT})	V _{SS} -0.3 ~ V _{SS} +8	V
Power dissipation(PD)	250	mW
	500	mW
	500	mW
	250	mW
Operating ambient temperature(T _{opr})	-40 ~ +85	°C
Storage temperature(T _{stg})	-40 ~ +125	°C
Soldering Temperature & Time(T _{solder})	260°C, 10s	

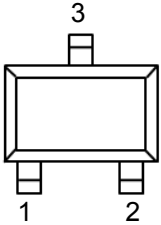


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Packaging Type

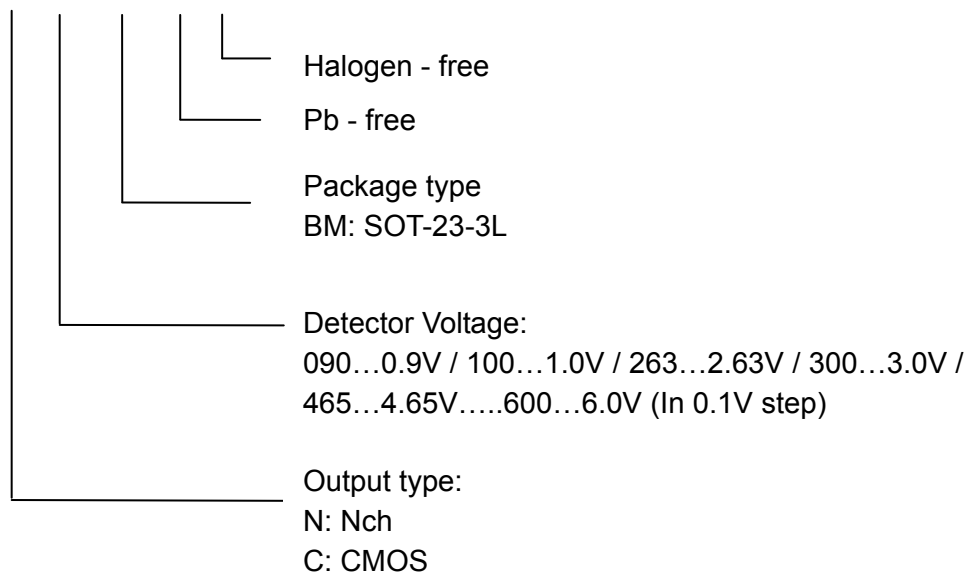
SOT-23-3L



SOT-23-3	Description	Function
3	V _{DD}	Voltage input Pin
1	V _{OUT}	Voltage detection output pin
2	V _{SS}	GND Pin

Ordering information

ACE306A X XXX XX + H

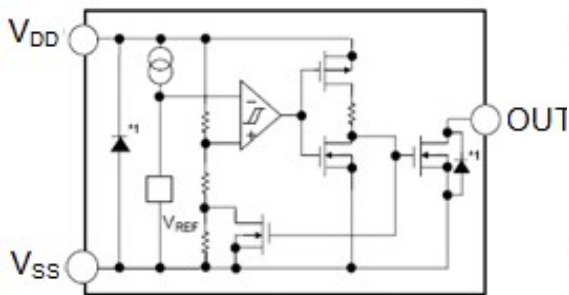




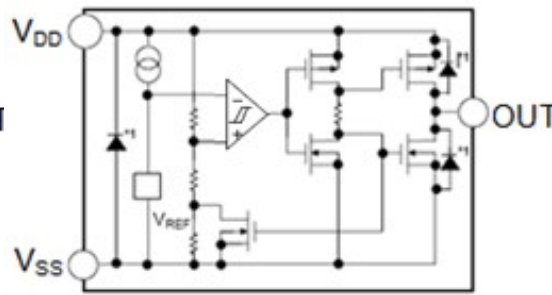
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Block diagram



N channel open-drain



CMOS output

Electrical Characteristics

(Ta=25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Reference data			Unit	
			Min.	Typ.	Max.		
$-V_{DET}$	Detection Voltage*1	-	$-V_{DET(S)} \times 0.98$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02$	V	
V_{HYS}	Hysteresis Width	-	$0.02 \times -V_{DET(S)}$	$0.05 \times -V_{DET(S)}$	$0.08 \times -V_{DET(S)}$	V	
L_{SS}	Current Consumpti	$V_{DD} = -V_{DET} + 0.5V$	ACE306A C/N20~26	-	1.0	3.0	μA
			ACE306A C/N26~39	-	1.2	3.2	μA
			ACE306A C/N39~60	-	1.5	3.5	μA
V_{DD}	Operating Voltage	-	0.95	-	7	V	
L_{OUT}	Output current	NMOS: $V_{OUT} = 0.5V$ $V_{DD} = -V_{DET} - 0.5V$	ACE306A C/N20~26	3.0	13.0	-	mA
			ACE306A C/N26~39	3.0	15.0	-	mA
			ACE306A C/N39~60	3.0	18.0	-	mA
		PMOS: $V_{DD} - V_{OUT} =$	ACE306A C/N20~26	1.5	4.0	-	mA
			ACE306A C/N26~39	1.5	6.0	-	mA



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		0.5V $V_{DD} = -V_{DET}$ +0.5V	ACE306A C/N39~60	1.5	8.0	-	mA
I_{LEAK}	Leakage Current	Only for NMOS open-drain output products, $V_{DD} = 8.0$ V, $V_{OUT} = 8.0$ V			-	1.0	μ A
	Temperature Coefficient	$T_a = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$		-	± 120	± 360	ppm/ $^{\circ}\text{C}$
T_{PLH}	Delay time	$V_{in} = V_{det} + 0.5V$		130	210	290	ms

*1. -VDET: Actual detection voltage value, -VDET(S): Specified detection voltage value

Function description

When a voltage higher than the release voltage ($+V_{DET}$) is applied to the voltage input pin (V_{DD}), the voltage will gradually fall. When a voltage higher than the detect voltage ($-V_{DET}$) is applied to V_{DD} , output (V_{OUT}) will be equal to the input at V_{DD} . Note that high impedance exists at V_{OUT} with the N-channel open drain configuration. If the pin is pulled up, V_{OUT} will be equal to the pull up voltage.

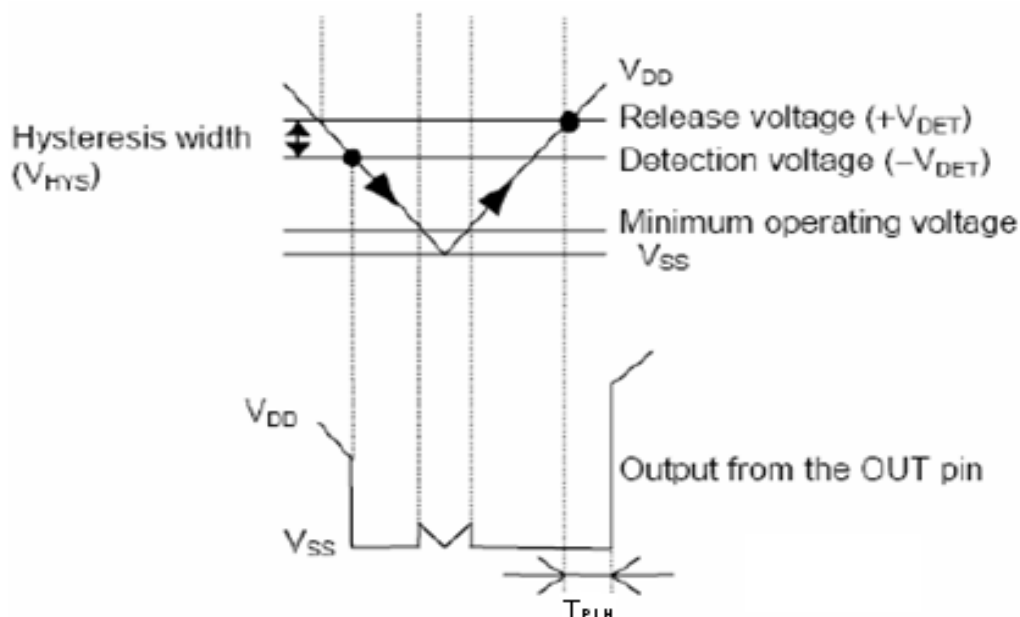
When V_{DD} falls below $-V_{DET}$, V_{OUT} will be equal to the ground voltage (V_{SS}) level (detect state). Note that this also applies to N-channel open drain configurations.

When V_{DD} falls to a level below that of the minimum operating voltage (V_{MIN}) output will become unstable. Because the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.

When V_{DD} rises above the V_{SS} level (excepting levels lower than minimum operating voltage), V_{OUT} will be equal to V_{SS} until V_{DD} reaches the $+V_{DET}$ level.

Although V_{DD} will rise to a level higher than $+V_{DET}$, V_{OUT} maintains ground voltage level via the delay circuit.

Following transient delay time, V_{DD} will be output at V_{OUT} . Note that high impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up



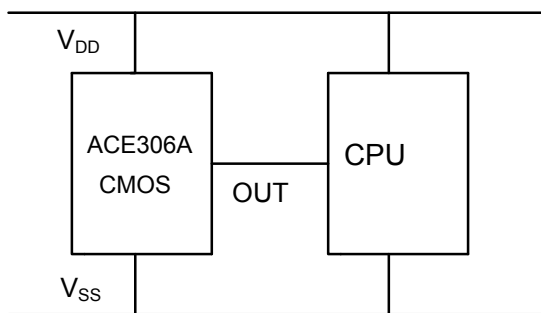


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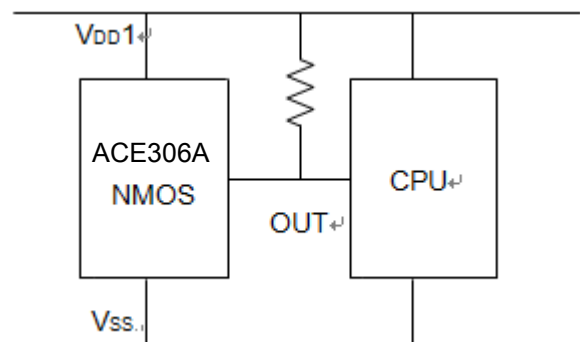
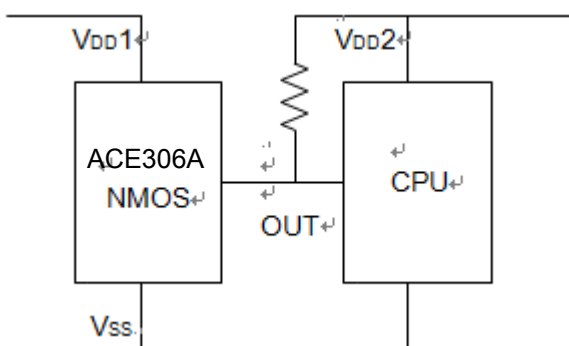
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Typical application Circuits

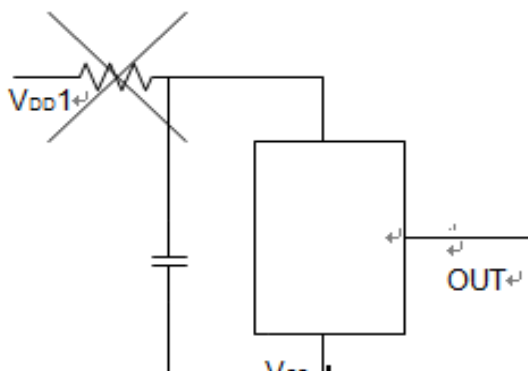
C:CMOS output:



NMOS open-drain:



Forbidden Circuits





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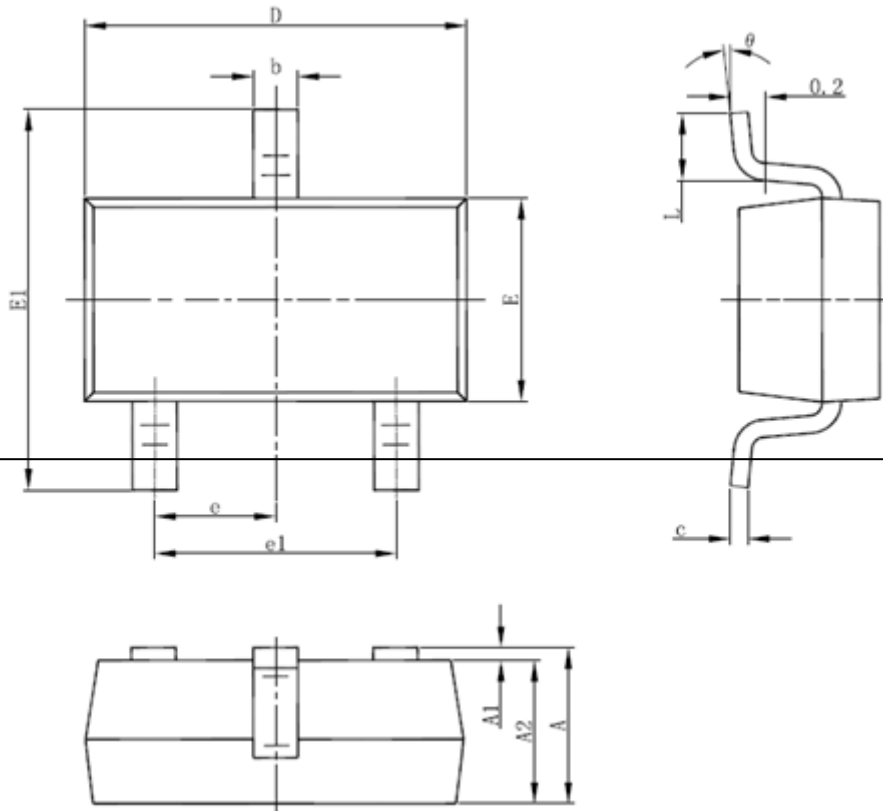
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Packing

SOT-23-3L

Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004



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A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
Θ	0°	8°	0°	8°



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Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD.

As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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