BL22P64 SPECIFICATION

8-bit OTP MCU

V1.3

Shanghai Belling Co., Ltd.

1. PRODUCT OVERVIEW

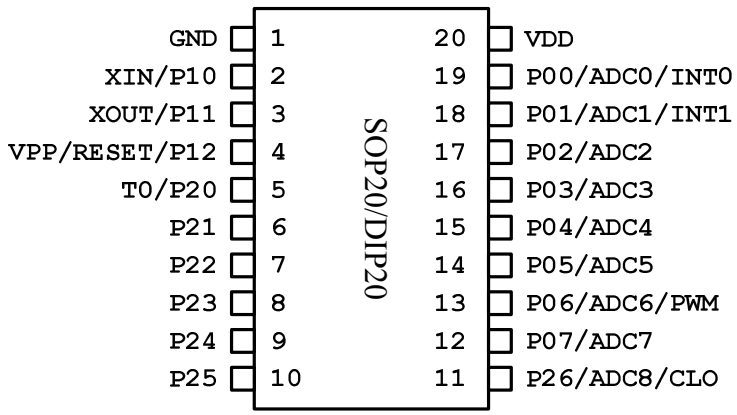
BL22P64 can be used for dedicated control functions in a variety of applications, such as induction cooker, microwave oven, soybean milk maker and so on.

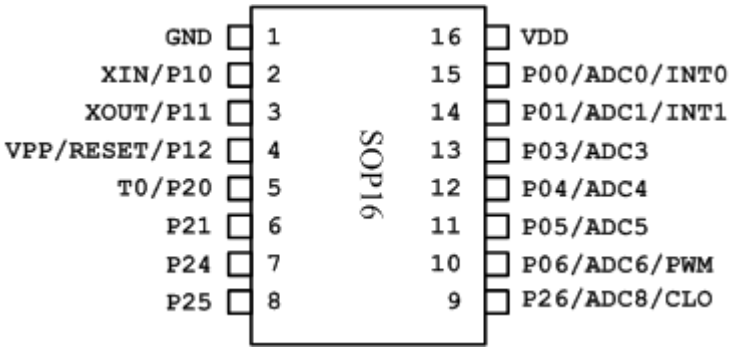
A dual address/data bus architecture and bit-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counter, A/D converter and PWM are designed for measure and control.

2. FEATURES

- 8-bit CISC core（compatible with Motorola HC05）
- 4K byte OTP ROM
- 208 byte RAM
- Three configurable I/O ports (18 pins)
- One 8-bit PWM output
- One 8-bit timer/counter with time interval mode
- A/D converter with nine input channels and 10-bit resolution
- Four interrupt sources (two external interrupt, timer interval interrupt, PWM interrupt)
- WATCH DOG
- 3V LVR
- Four configurable clock circuit:
  - Crystal/Ceramic oscillator (400K-4MHz)
  - External RC oscillator
  - 3.2MHz(VDD=5V) internal RC oscillator
  - 0.5MHz(VDD=5V) internal RC oscillator
- Operating Voltage: 2.7-5.5V
- Operating temperature: -40-85℃
- Package Types: SOP20/DIP20/SOP16
- 4KV EMC

3. PIN ASSIGNMENTS



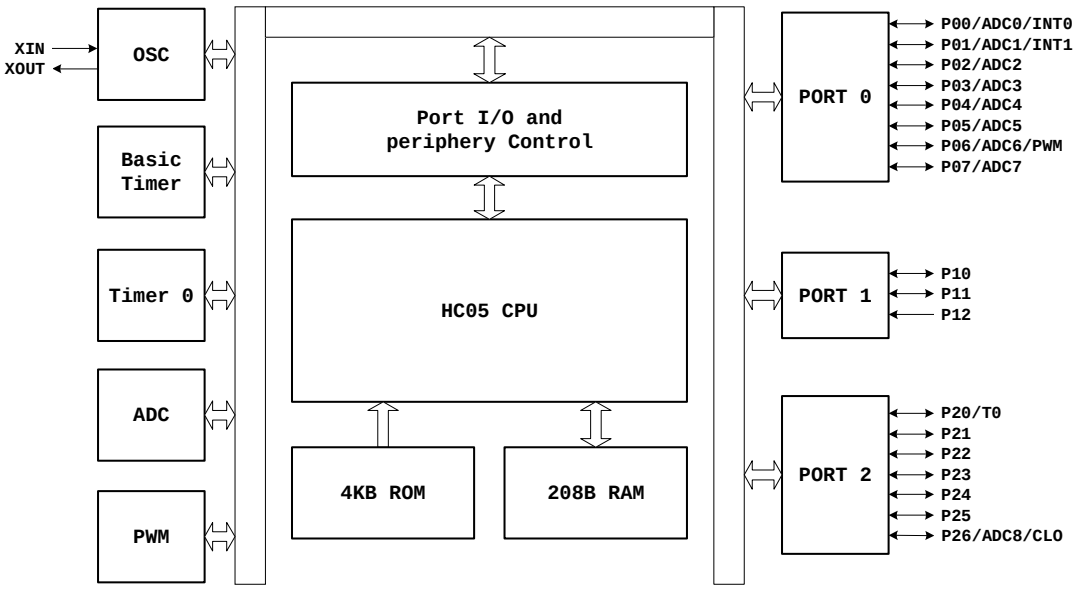


4. PIN DESCRIPTIONS

Pin name	In/Out	Pin Description	Share Description
GND	-	ground	-
P10	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors or pull-down resistors are assignable by software.	XIN
P11	I/O		XOUT
P12	IN	Schmitt trigger input port	RESET/VPP
P20	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors are assignable by software.	T0
P21	I/O		-
P22	I/O		-
P23	I/O		-
P24	I/O		-
P25	I/O		-
P26	I/O		ADC8/CLO
P00	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are assignable by software.	ADC0/INT0
P01	I/O		ADC1/INT1
P02	I/O		ADC2
P03	I/O		ADC3
P04	I/O		ADC4
P05	I/O		ADC5
P06	I/O		ADC6/PWM
P07	I/O		ADC7
VDD	-	Voltage input	-

5. FUNCTION DESCRIPTIONS

5.1 BLOCK DIAGRAM



Block Diagram

5.2 ADDRESS SPACES

$0000-$002F: Control registers

$0030-$00FF: RAM (208 bytes)

$0100-$0FFF: Reserved

$1000-$1FFF: OTP ROM (4096 bytes)

5.3 CONTROL REGISTERS

Control Registers

Register name	*Address*	*R/W*	*Reset Value*
T0CNT	$00	R	0000 0000
T0DATA	$01	R/W	1111 1111
T0CON	$02	R/W	00-- 0-00
MCR	$03	R/W	---- ---R
BTCON	$0C	R/W	0000 1000
BTCNT	$0D	R	0000 0000
P0	$10	R/W	0000 0000
P1	$11	R/W	---- -000
P2	$12	R/W	-000 0000
P0CONH	$16	R/W	0000 0000
P0CONL	$17	R/W	0000 0000
P0PND	$18	R/W	---- 0000
P1CON	$19	R/W	00-- 0000
P2CONH	$1A	R/W	-000 0000
P2CONL	$1B	R/W	0000 0000
PWMDATA	$22	R/W	0000 0000
PWMCON	$23	R/W	00-0 0000
ADCON	$27	R/W	0000 1000

ADDATAH	$28	R	XXXX XXXX
ADDATAL	$29	R	---- --XX

NOTE:

- -：Not used; X: Undefined; R: Determined by OPBIT[2]

5.3.1 T0CNT（TIMER 0 Counter Register）

T0CNT is a 8-bit counter register of Timer 0. T0CNT is read only.

5.3.2 T0DATA（TIMER 0 Data Register）

T0DATA is a 8-bit Data Register to set match data of Timer 0. When the counter value is identical to the value written to T0DATA, generates a Timer 0 match interrupt.

5.3.3 T0CON（TIMER 0 Control Register）

Timer 0 Control Register, is used to select the Timer 0 operating mode.

.7-.6 T0PS[1:0]　Timer 0 input clock selection

00: Fsys/4096

01: Fsys/256

10: Fsys/8

11: Fsys

（NOTE：Fsys is system frequency which is half of oscillator's）

.5-.4 Not used

.3 T0CLR　Timer 0 counter clear bit. Value is "0" when read.

0: No effect

1: Clear the Timer 0 counter (when write) 0

.2 Not used

.1 T0E Timer 0 interrupt enable bit

0: Disable T0 interrupt

1: Enable T0 interrupt

.0 T0F　Timer 0 interrupt pending bit

0: No T0 interrupt pending (when read)

0: Clear T0 pending bit (when write)

1: Interrupt is pending (when read)

1: No effect (when write)

5.3.4 MCR（Miscellaneous Control Register）

MCR is used to control LVR. The reset value is determined by OPBIT[2]。

.7-.1 Not used

.0　LVRE　LVR enable bit

0: LVR disable

1: LVR enable

5.3.5 BTCON（Basic Timer Control Register）

BTCON, is used to select the input clock frequency, to clear the basic timer counter and frequency dividers, and to control the watchdog timer.

.7-.4 WDTE[3:0]　Watchdog timer enable bits

1010: Disable watchdog function
Other value: Enable watchdog function
（NOTE：Watchdog function is enable when reset.）

.3-.2 BTPS[1:0] Basic timer input clock selection bits
00: Fsys/4096
01: Fsys/1024
10: Fsys/256
11: Fsys/128

.1 BTCLR Basic timer counter clear bits. Value is “0” when read.
0: No effect
1: Clear basic timer counter

.0 DVCLR Divider clear bit for basic timer and timer 0. Value is “0” when read.
0: No effect
1: Clear both dividers

5.3.6 BTCNT（Basic Timer Counter）

BTCNT is a 8-bit basic timer counter, and read only. BTCNT can be cleared by writing a "1" to BTCLR (BTCON.1).

5.3.7 P0（PORT 0 Data Register）

P0 is data register for Port 0.

5.3.8 P1（PORT 1 Data Register）

P1 is data register for Port 1.

5.3.9 P2（PORT 2 Data Register）

P2 is data register for Port 2.

5.3.10 P0CONH（Port 0 Control Register (High Byte)）

.7-.6 P07C[1:0] P07 Configuration Bits
00: Schmitt trigger input; pull-up enable
01: Schmitt trigger input
10: Push-pull output
11: A/D converter input (ADC7)

.5-.4 P06C[1:0] P06 Configuration Bits
00: Schmitt trigger input; pull-up enable
01: PWM output
10: Push-pull output
11: A/D converter input (ADC6)

.3-.2 P05C[1:0] P05 Configuration Bits
00: Schmitt trigger input; pull-up enable
01: Schmitt trigger input
10: Push-pull output
11: A/D converter input (ADC5)

.1-.0 P04C[1:0] P04 Configuration Bits

00: Schmitt trigger input; pull-up enable
01: Schmitt trigger input
10: Push-pull output
11: A/D converter input (ADC4)

5.3.11 P0CONL（Port 0 Control Register (Low Byte)）

.7-.6 P03C[1:0] P03 Configuration Bits
00: Schmitt trigger input
01: Schmitt trigger input; pull-up enable
10: Push-pull output
11: A/D converter input (ADC3)
.5-.4 P02C[1:0] P02 Configuration Bits
00: Schmitt trigger input
01: Schmitt trigger input; pull-up enable
10: Push-pull output
11: A/D converter input (ADC2)
.3-.2 P01C[1:0] P01 Configuration Bits
00: Schmitt trigger input / INT1 input
01: Schmitt trigger input; pull-up enable / INT1 input
10: Push-pull output
11: A/D converter input (ADC1)
.1-.0 P00C[1:0] P00 Configuration Bits
00: Schmitt trigger input / INT0 input
01: Schmitt trigger input; pull-up enable / INT0 input
10: Push-pull output
11: A/D converter input (ADC0)

5.3.12 P0PND（Port 0 Interrupt Pending Register）

.7-.4 Not used
.3 INT1E INT1 Interrupt Enable Bit
0: INT1 disable
1: INT1 enable
.2 INT1F INT1 Pending Bit
0: No interrupt pending (when read)
0: Pending bit clear (when write)
1: Interrupt is pending (when read)
1: No effect (when write)
.1 INT0E INT0 Interrupt Enable Bit
0: INT0 disable
1: INT0 enable
.0 INT0F INT0 Pending Bit
0: No interrupt pending (when read)
0: Pending bit clear (when write)
1: Interrupt is pending (when read)
1: No effect (when write)

5.3.13 P1CON（Port 1 Control Register）

.7 P11OD P11 Open-drain Enable Bit
0: P11 as a push-pull output
1: P11 as a n-channel open-drain output
.6 P10OD P10 Open-drain Enable Bit
0: P11 as a push-pull output
1: P11 as a n-channel open-drain output
.5-.4 Not used
.3-.2 P11C[1:0] P11 Configuration Bits
00: Schmitt trigger input
01: Schmitt trigger input; pull-up enable
10: Push-pull output
11: Schmitt trigger input; pull-down enable
.1-.0 P10C[1:0] P10 Configuration Bit
00: Schmitt trigger input
01: Schmitt trigger input; pull-up enable
10: Push-pull output
11: Schmitt trigger input; pull-down enable
（NOTE：When system clock comes from crystal/ceramic oscillator or external RC oscillator, P10 and P11 must be set as input and pull-up disable）

5.3.14 P2CONH（Port 2 Control Register (High Byte)）

.7 Not used
.6-.4 P26C[2:0] P26 Configuration Bits
000: Schmitt trigger input; pull-up enable
001: Schmitt trigger input
01x: A/D converter input (ADC8)
100: Open-drain output
101: Open-drain output; pull-up enable
110: Open-drain output
111: CLO output
.3-.2 P25C[1:0] P25 Configuration Bits
00: Schmitt trigger input; pull-up enable
01: Schmitt trigger input
10: Push-pull output
11: Open-drain output
.1-.0 P24C[1:0] P24 Configuration Bits
00: Schmitt trigger input; pull-up enable
01: Schmitt trigger input
10: Push-pull output
11: Open-drain output

5.3.15 P2CONL（Port 2 Control Register (Low Byte)）

.7-.6 P23C[2:0] P23 Configuration Bits

00: Schmitt trigger input; pull-up enable
01: Schmitt trigger input
10: Push-pull output
11: Open-drain output

.5-.4 P22C[2:0] P22 Configuration Bits
00: Schmitt trigger input; pull-up enable
01: Schmitt trigger input
10: Push-pull output
11: Open-drain output

.3-.2 P21C[1:0] P21 Configuration Bits
00: Schmitt trigger input; pull-up enable
01: Schmitt trigger input
10: Push-pull output
11: Open-drain output

.1-.0 P20C[1:0] P20 Configuration Bits
00: Schmitt trigger input; pull-up enable
01: Schmitt trigger input
10: Push-pull output
11: T0 match output

5.3.16 PWMDATA（PWM Data Register）

PWMDATA determines the duty of output clock generated by 8-bit PWM circuit.

5.3.17 PWMCON（PWM Control Register）

.7-.6 PWMPS[1:0] PWM Input Clock Selection Bits
00: Fsys/64
01: Fsys/8
10: Fsys/2
11: Fsys

.5 Not used

.4 PWMDRS PWMDATA Reload Interval Selection Bit
0: Reload from 8-bit up counter overflow
1: Reload from 6-bit up counter overflow

.3 PWMCLR PWM Counter Clear Bit. Value is “0” when read.
0: No effect
1: Clear the PWM counter (when write)

.2 PWMCE PWM Counter Enable Bit
0: Stop counter
1: Start (Resume countering)

.1 PWMIE PWM Overflow Interrupt Enable Bit (8-Bit Overflow)
0: Disable interrupt
1: Enable interrupt

.0 PWMIF PWM Overflow Interrupt Pending Bit
0: No interrupt pending (when read)
0: Clear pending bit (when write)

1: Interrupt is pending (when read)
1: No effect (when write)

5.3.18 ADCON（A/D Control Register）

.7-.4 ADCH[3:0] A/D Input Pin Selection Bits
0000: ADC0
0001: ADC1
0010: ADC2
0011: ADC3
0100: ADC4
0101: ADC5
0110: ADC6
0111: ADC7
1000: ADC8
1001: GND (for test)
1010: GND (for test)
1011: GND (for test)
1100: GND (for test)
1101: VDD (for test)
1110: VDD/4 (for test)
1111: VDD/2 (for test)

.3 EOC A/D End-of-Conversion Status Bit，read only
0: A/D conversion is in progress
1: A/D conversion complete

.2-.1 ADPS[1:0] Clock Source Selection Bit
00: Fsys/8
01: Fsys/4
10: Fsys/2
11: Fsys

.0 ADCE Conversion Start Bit. Value is “0” when read.
0: No meaning
1: A/D conversion start

5.3.19 ADDATAH（A/D Data Register(High 8-bit)）

5.3.20 ADDATAL（A/D Data Register(Low 2-bit)）

ADDATAH and ADDATAL are used to storage conversion data of A/D.

5.4 OPBIT

OPBIT is a special byte in OTP ROM and used to configure some initial functions for BL22P64. OPBIT is set when OTP written.

.7 ENCR
0: OTP read protection
1: OTP can be read

.3 P12F

0: P12 as normal I/O pin
1: P12 as external reset input pin

.2 LVREO
0: LVR disable
1: LVR enable

.0-.1 OSC/RC
00: Crystal/ceramic oscillator (400K-4MHz) as system clock
01: External RC oscillator as system clock
10: Internal RC oscillator(0.5MHz) as system clock
11: Internal RC oscillator(3.2MHz) as system clock

6. ELECTRICAL DATA

6.1 Absolute Maximum Ratings

(T_A=25℃)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	-	-0.3 to +6.5	V
Input voltage	V_I	All ports	-0.3 to VDD+0.5	V
Output voltage	V_O	All ouput ports	-0.3 to VDD+0.5	V
Output current high	I_{OH}	One I/O pin active	-25	mA
		All I/O pin active	-80	mA
Output current low	I_{OL}	One I/O pin active	+30	mA
		All I/O pin active	+150	mA
Operating temperature	T_A	-	-40 to +85	℃
Storage temperature	T_{STG}	-	-65 to +150	℃

6.2 DC Electrical Characteristics

(T_A=25℃ VDD=2.7-5.5V)

Parameter	Sym.	Condition		Min	Typ	Max	Unit
Input high voltage	V_{IH}	P0,P1,P2	VDD=2.7-5.5V	0.8VDD	-	VDD	V
Input low voltage	V_{IL}	P0,P1,P2	VDD=2.7-5.5V	0	-	0.2VDD	V
Output high voltage	V_{OH}	I_{OH}=-10mA P0,P1,P2	VDD=4.5-5.5V	VDD-1.5	VDD-0.4	-	V
Output low voltage	V_{OL}	I_{OL}=25mA P0,P1,P2	VDD=4.5-5.5V	-	0.5	2.0	V
Input high leakage current	I_{IH}	All input	V_{IN}=VDD	-	-	1	uA
Input low leakage current	I_{IL}	All input	V_{IN}=0	-	-	1	uA

Pull-up resistors	R_{PU}	P0,P1,P2	VDD=2.7-5.5V	15	30	100	KΩ
Pull-down resistors	R_{PD}	P0,P1,P2	VDD=2.7-5.5V	15	30	100	KΩ
Dynamic working current	I_{DD}	4MHz clock	VDD=4.5-5.5V	-	5	10	mA
Standby working current	I_{STD1}	STOP mode LVR disable	VDD=4.5-5.5V	-	0.1	1	uA
	I_{STD2}	STOP mode LVR enable	VDD=4.5-5.5V	-	10	20	

6.3 LVR Characteristics

(T_A=25℃ VDD=2.7-5.5V)

Parameter	Sym.	Condition	Min	Typ	Max	Unit
Low voltage reset	V_{LVR}	-	2.7	3.0	3.3	V

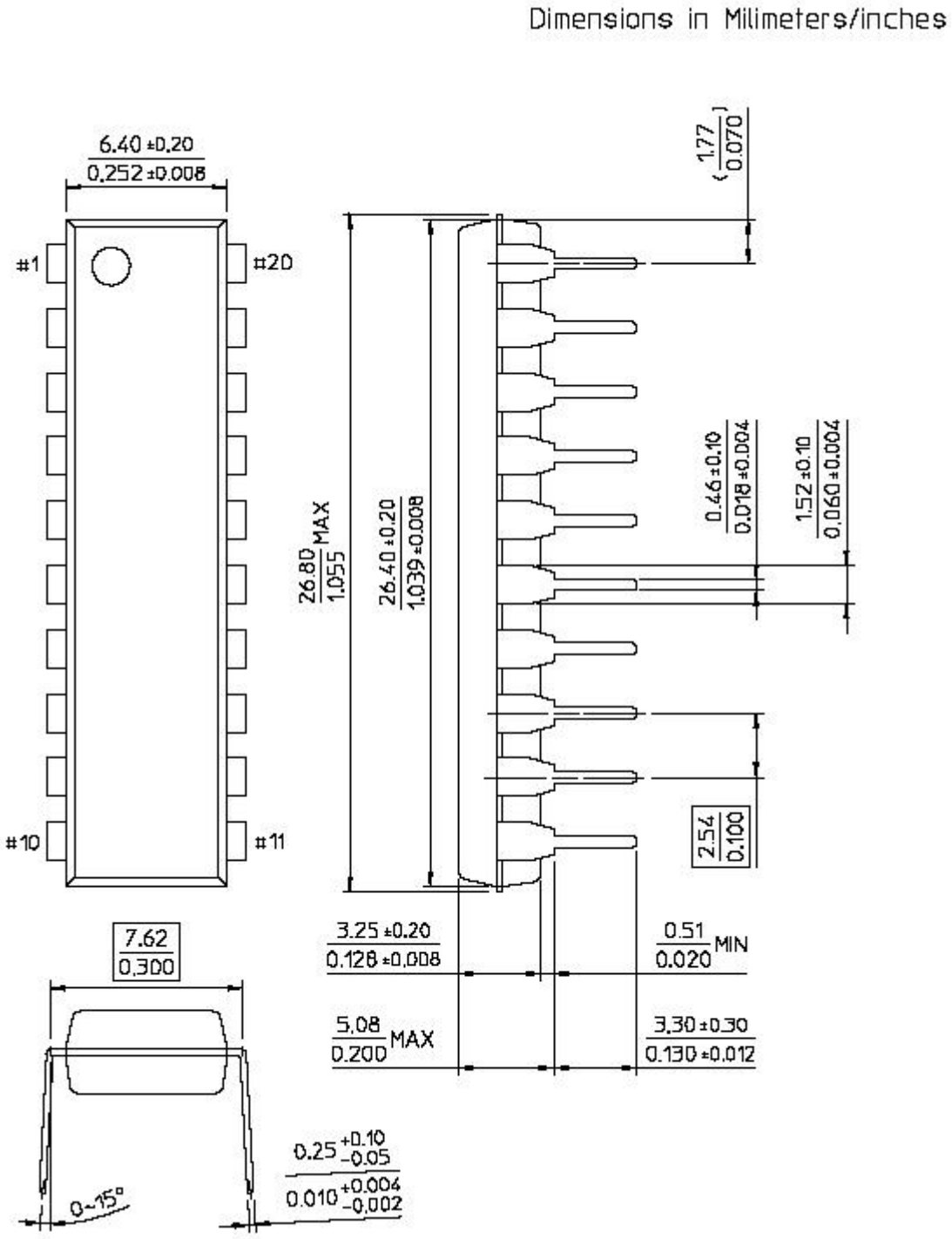
6.4 A/D Converter Characteristics

(T_A=25℃ VDD=5.0V)

Parameter	Sym.	Condition	Min	Typ	Max	Unit
Total accracy	-	VDD=5V fosc=4MHz	-	-	±3	LSB
Integral linearity error	ILE	VDD=5V fosc=4MHz	-	-	±2	LSB
Differential linearity error	DLE	VDD=5V fosc=4MHz	-	-	±1	LSB
Offset error of top	EOT	VDD=5V fosc=4MHz	-	±1	±3	LSB
Offset error of bottom	EOB	VDD=5V fosc=4MHz				
Conversion time	t_{CON}	VDD=5V fosc=4MHz	-	25	-	us
Analog input voltage	V_{IAN}	-	VSS	-	VDD	V
Analog input impedance	R_{AN}	-	2	-	-	MΩ
Analog input current	I_{ADIN}	VDD=5V	-	-	10	uA
Analog block current	I_{ADC}	VDD=5V	-	1	3	mA
		VDD=5V power down mode	-	0.1	0.5	uA

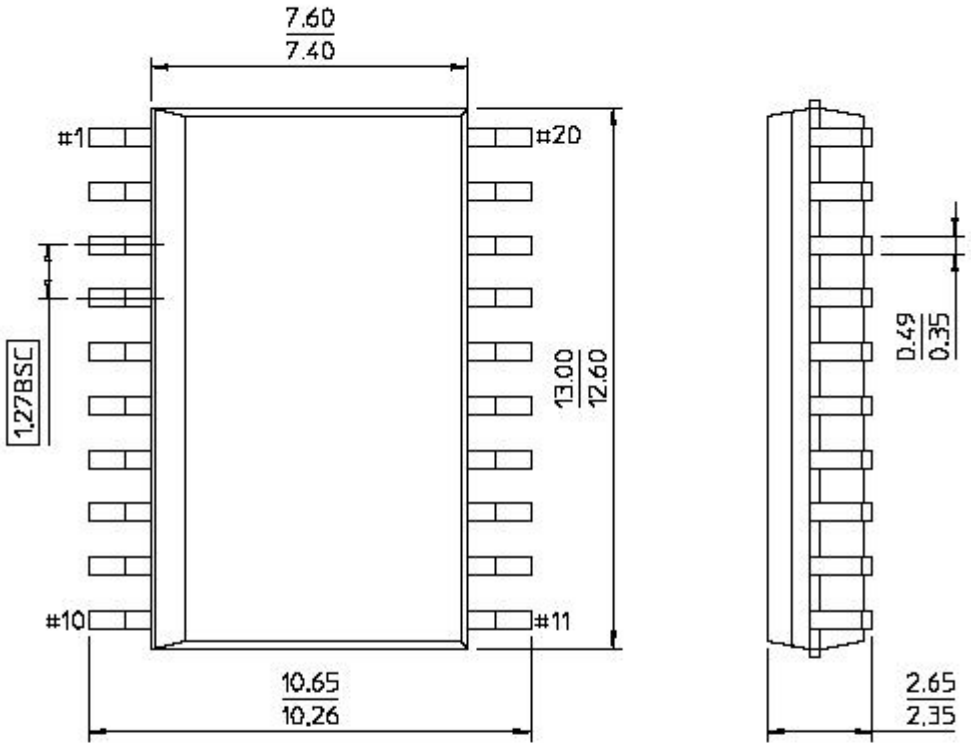
7. Package Dimensions

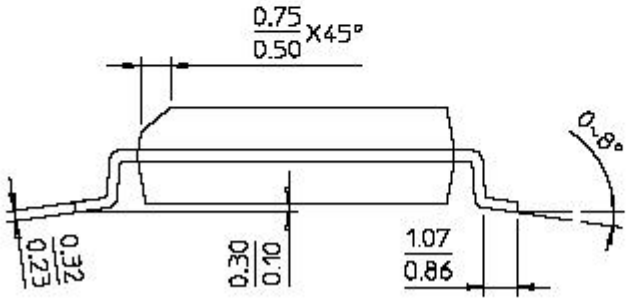
DIP20



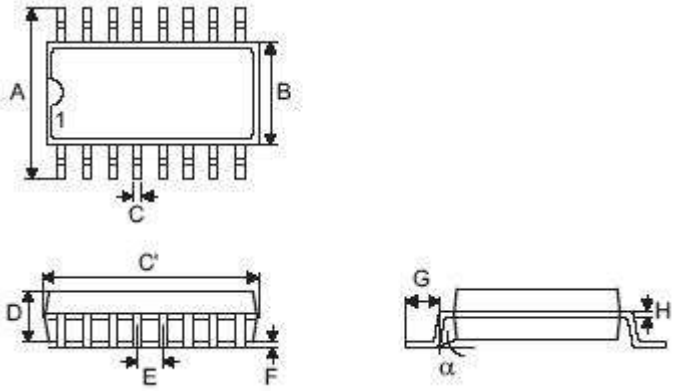
SOP20

Dimensions in Milimeters





SOP16（150mil）



Symbol	Dimensions in mil			Dimensions in milimeter		
	Max.	Nom.	Min.	Max.	Nom.	Min.
A	238	-	244	6.05	-	6.20
B	150	-	157	3.80	-	4.00
C	14	-	19	0.36	-	0.48
C'	386	-	398	9.80	-	10.10
D	53	-	62	1.35	-	1.57
E	-	50	-	-	1.27	-
F	4	-	-	0.10	-	-
G	22	-	32	0.56	-	0.82
H	4	-	12	0.10	-	0.30
α	0°	-	8°	0°	-	8°