Dual 800mA Low Quiescent Current 2.25MHz High Efficiency Synchronous Buck Regulator

ISL78228

The ISL78228 is a high efficiency, dual synchronous step-down DC/DC regulator that can deliver up to 800mA continuous output current per channel. The supply voltage range of 2.75V to 5.5V allows for the use of a 3.3V or 5V input. The current mode control architecture enables very low duty cycle operation at high frequency with fast transient response and excellent loop stability. The ISL78228 operates above the AM radio band as well as the 2.25MHz switching frequency, allowing for the use of small, low cost inductors and capacitors. Each channel is optimized for generating an output voltage as-low-as 0.6V.

The ISL78228 has a user configurable mode of operation-forced PWM mode and PFM mode. The forced PWM mode operation reduces noise and RF interference while the PFM mode operation provides high efficiency by reducing switching losses at light loads. In PFM mode of operation, both channels draw a total quiescent current of only 30µA, hence enabling high light load efficiency in order to maximize battery life.

The ISL78228 offers a 1ms power-good (PG) to monitor both outputs at power-up. When shutdown, ISL78228 discharges the outputs capacitor. Other features include internal digital soft-start, enable for power sequence, overcurrent protection, and thermal shutdown. The ISL78228 is offered in a 3mmx3mm 10 Ld DFN package with 1mm maximum height. The complete converter occupies less than 1.8cm^2 area.

The ISL78228 is AEC-Q100 rated. The ISL78228 is rated for the automotive temperature range (-40°C to +105°C).

Features

- Internal current mode compensation
- 100% maximum duty cycle for lowest dropout
- Selectable forced PWM mode and PFM mode
- External synchronization up to 4MHz
- Start-up with pre-biased output
- Soft-stop output discharge during disabled
- Internal digital soft-start - 2ms
- Power-good (PG) output with 1ms delay
- AEC-Q100 tested
- Pb-free (RoHS compliant)

Applications

- DC/DC POL modules
- µC/µP, FPGA and DSP power
- Rear camera systems
- Navigation systems
- Infotainment systems

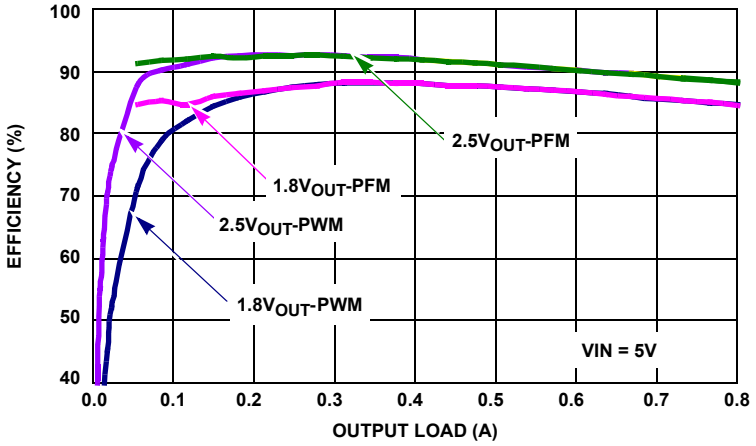
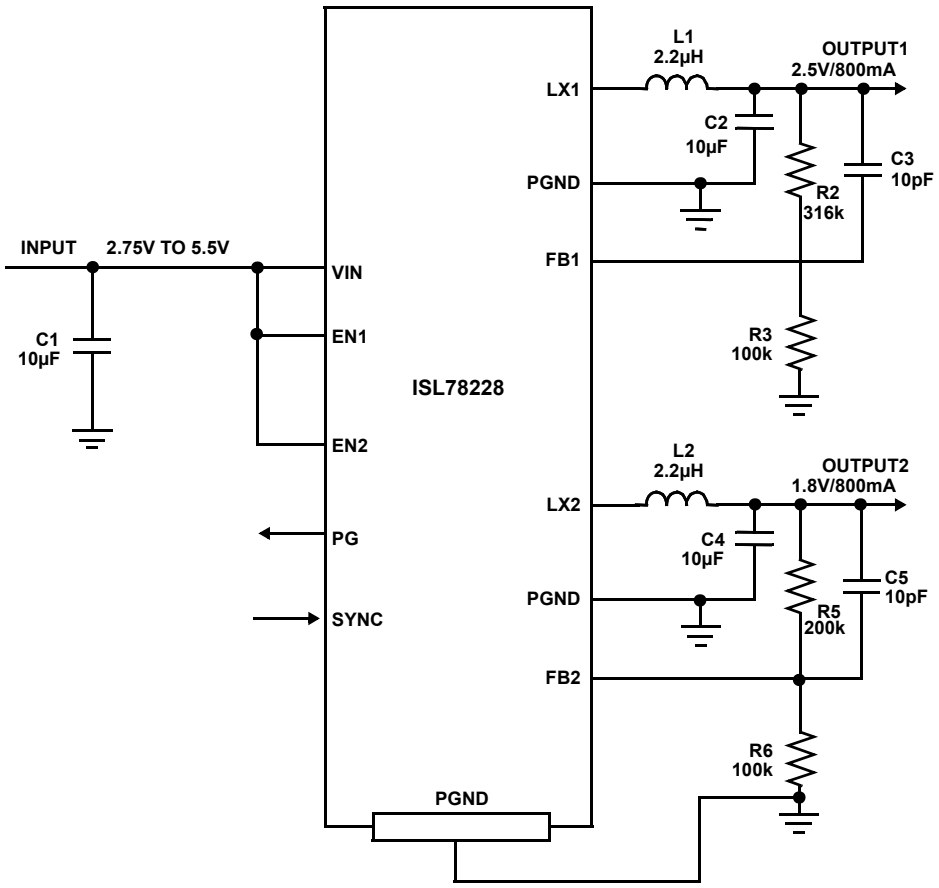


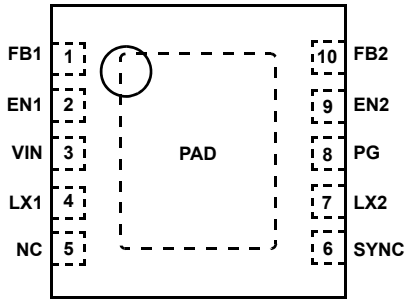
FIGURE 1. EFFICIENCY CHARACTERISTICS CURVE

Typical Application



Pin Configuration

ISL78228
(10 LD 3X3 DFN)
TOP VIEW



Pin Descriptions

PIN#	PIN NAME	DESCRIPTION
1	FB1	The feedback network of the Channel 1 regulator. FB1 is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB1. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. There is an internal compensation to meet a typical application. In addition, the regulator power-good and undervoltage protection circuitry use FB1 to monitor the Channel 1 regulator output voltage.
2	EN1	Regulator Channel 1 enable pin. Enable the output, V_{OUT1}, when driven to high. Shutdown the V_{OUT1} and discharge output capacitor when driven to low. Do not leave this pin floating.
3	VIN	Input supply voltage. Connect 10µF ceramic capacitor to power ground.
4	LX1	Switching node connection for Channel 1. Connect to one terminal of inductor for V_{OUT1}.
5	NC	Recommended to connect this pin to the exposed pad.
6	SYNC	Mode Selection pin. Connect to logic high or input voltage VIN for PFM mode; connect to logic low or ground for forced PWM mode. Connect to an external function generator for synchronization, and negative edge trigger. Do not leave this pin floating.
7	LX2	Switching node connection for Channel 2. Connect to one terminal of inductor for V_{OUT2}.
8	PG	1ms timer output. At power-up or EN_ HI, this output is a 1ms delayed Power-Good signal for both the V_{OUT1} and V_{OUT2} voltages. There is an internal 1MΩ pull-up resistor.
9	EN2	Regulator Channel 2 enable pin. Enable the output, V_{OUT2}, when driven to high. Shutdown the V_{OUT2} and discharge output capacitor when driven to low. Do not leave this pin floating.
10	FB2	The feedback network of the Channel 2 regulator. FB2 is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB2. With a properly selected divider, the output voltage can be set to any voltage between the power-rail (reduced by converter losses) and the 0.6V reference. There is an internal compensation to meet a typical application. In addition, the regulator power-good and undervoltage protection circuitry use FB2 to monitor the Channel 2 regulator output voltage.
-	PAD	The exposed pad must be connected to PGND for proper electrical performance. Add as much vias as possible for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL78228ARZ	8228	-40 to +105	10 Ld 3x3 DFN	L10.3x3C

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78228. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (Reference to GND)

Supply Voltage (V_{IN}) . . . . . -0.3V to 6.5V
V_{IN} . . . . . -0.3V to 7V (20ms)
EN1, EN2, PG, SYNC . . . . . -0.3V to V_{IN} + 0.3V
LX1, LX2 . . . . . -1.5V to 6.5V
LX1, LX2 . . . . . -1.5V (100ns)
. . . . . -0.3V (DC) to 7V (20ms)
FB1, FB2 . . . . . -0.3V to 2.7V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD-A115-A) 300V
Charge Device Model (Tested per AEC-Q100-011) 2kV
Latch-Up (Tested per JESD78C; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package (Notes 4, 5)	49	4

Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

V_{IN} Supply Voltage Range . . . . . 2.75V to 5.5V
Load Current Range Per Channel . . . . . 0mA to 800mA
Ambient Temperature Range . . . . . -40°C to +105°C
Junction Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameter limits are established over the recommended operating conditions: T_A = -40°C to +105°C, V_{IN} = 2.75V to 5.5V, EN1 = EN2 = V_{IN}, SYNC = 0V, L = 2.2µH, C_1 = 10µF, C_2 = C_4 = 10µF, I_{OUT1} = I_{OUT2} = 0A to 800mA. (Typical values are at T_A = +25°C, V_{IN} = 3.6V). **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising		2.5	2.75	V
		Falling	**2.1**	2.4		V
Quiescent Supply Current	I_Q	SYNC = V_{IN}, EN1 = EN2 = V_{IN}, no load at the output and no switches switching. VFB1 = VFB2 = 0.7V		30	**50**	µA
		SYNC = GND, EN1 = EN2 = V_{IN}, F_S = 2.25MHz, no load at the output		0.1	**1**	mA
Shut Down Supply Current	I_{SD}	V_{IN} = 5.5V, EN1 = EN2 = GND		6.5	**12**	µA
OUTPUT REGULATION						
FB1, FB2 Regulation Voltage	$V_{FB\_}$		**0.590**	0.6	**0.610**	V
FB1, FB2 Bias Current	$I_{FB\_}$	VFB = 0.55V		0.1		µA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.75V, I_{OUT} = 0A)		0.2		%/V
Soft-Start Ramp Time Cycle				2		ms
OVERCURRENT PROTECTION						
Peak Overcurrent Limit	I_{pk1}		**0.95**	1.2	**1.6**	A
	I_{pk2}		**0.95**	1.2	**1.6**	A
Peak SKIP Limit	I_{skip1}	V_{IN} = 3.6V	**180**	250	**360**	mA
	I_{skip2}		**180**	250	**360**	mA
LX1, LX2						
P-Channel MOSFET ON-Resistance		V_{IN} = 5.5V, I_O = 200mA		180	**350**	mΩ
		V_{IN} = 2.75V, I_O = 200mA		320	**450**	mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5.5V, I_O = 200mA		180	**350**	mΩ
		V_{IN} = 2.75V, I_O = 200mA		320	**450**	mΩ

Electrical Specifications Unless otherwise noted, all parameter limits are established over the recommended operating conditions: T_A = -40°C to +105°C, V_{IN} = 2.75V to 5.5V, EN1 = EN2 = V_{IN}, SYNC = 0V, L = 2.2µH, C_1 = 10µF, C_2 = C_4 = 10µF, I_{OUT1} = I_{OUT2} = 0A to 800mA. (Typical values are at T_A = +25°C, V_{IN} = 3.6V). **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
LX_ Maximum Duty Cycle				100		%
PWM Switching Frequency	F_S		**1.8**	2.25	**2.7**	MHz
Synchronization Range			**2.7**		**4**	MHz
LX Minimum On-Time		SYNC = 0 (forced PWM mode)			**100**	ns
Soft Discharge Resistance	$R_{DIS\_}$	EN = LOW	**80**	100	**130**	Ω
PG						
Output Low Voltage		Sinking 1mA, VFB = 0.5V			**0.3**	V
PG Pull-up Resistor				1		mΩ
Internal PGOOD Low Rising Threshold		Percentage of nominal regulation voltage	**88**	92	**96**	mΩ
Internal PGOOD Low Falling Threshold		Percentage of nominal regulation voltage	**82**	89	**91**	%
Delay Time (Rising Edge)				1		ms
Internal PGOOD Delay Time (Falling Edge)				1	**2**	µs
EN1, EN2, SYNC						
Logic Input Low					**0.4**	V
Logic Input High			**1.4**			V
SYNC Logic Input Leakage Current	I_{SYNC}	Pulled up to 5.5V		0.1	**1**	µA
Enable Logic Input Leakage Current	$I_{EN\_}$			0.1	**1**	µA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				25		°C

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.75V to 5.5V, EN = V_{IN}, L_1 = L_2 = 2.2µH, C_1 = 10µF, C_2 = C_4 = 10µF, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 800mA.

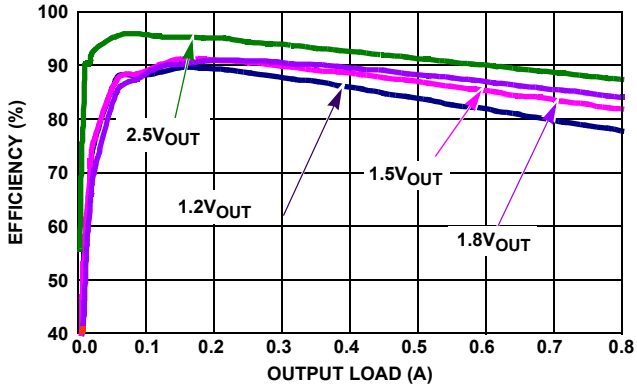


FIGURE 2. EFFICIENCY vs LOAD 2.25MHz 3.3V_{IN} PWM

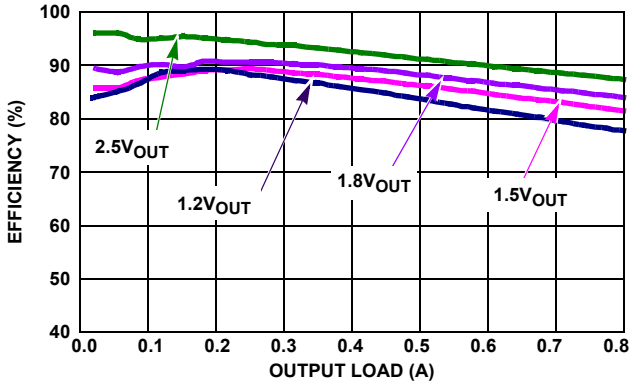


FIGURE 3. EFFICIENCY vs LOAD 2.25MHz 3.3V_{IN} PFM

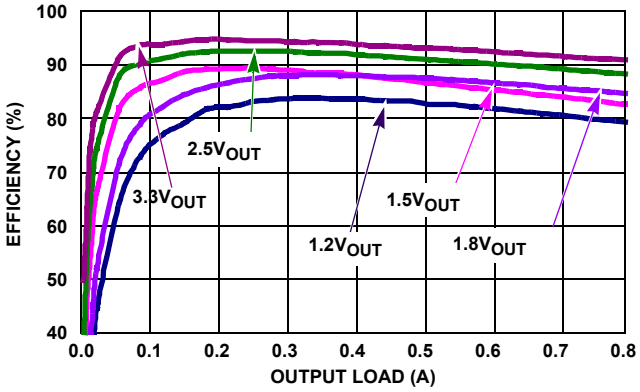


FIGURE 4. EFFICIENCY vs LOAD 2.25MHz 5V_{IN} PWM

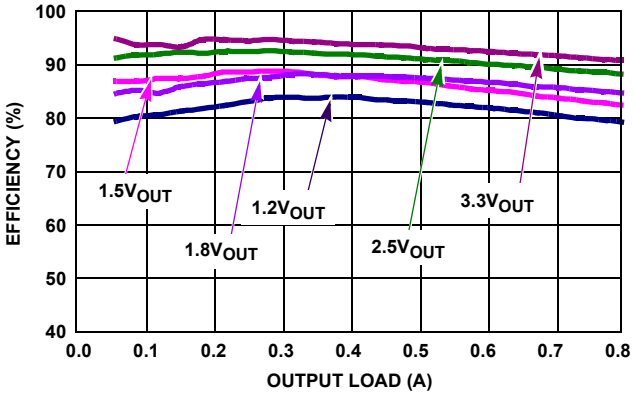


FIGURE 5. EFFICIENCY vs LOAD 2.25MHz 5V_{IN} PFM

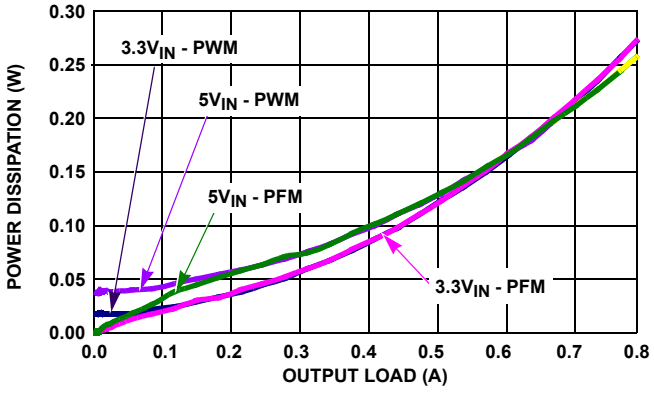


FIGURE 6. POWER DISSIPATION vs LOAD 2.25MHz, 1.8V_{OUT} PWM

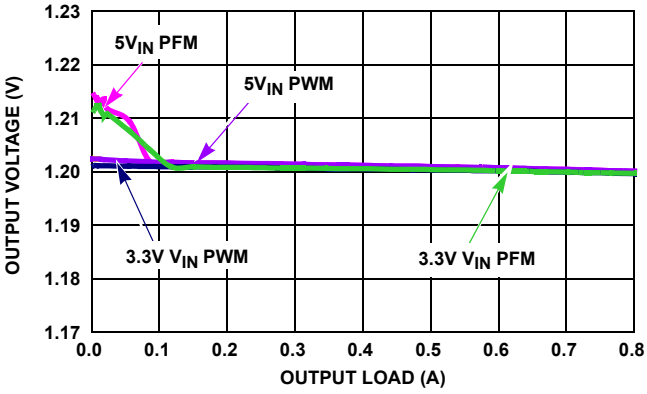


FIGURE 7. V_{OUT} REGULATION vs LOAD 2.25MHz, 1.2V_{OUT} PFM

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.75V to 5.5V, EN = V_{IN}, L_1 = L_2 = 2.2µH, C_1 = 10µF, C_2 = C_4 = 10µF, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 800mA. **(Continued)**

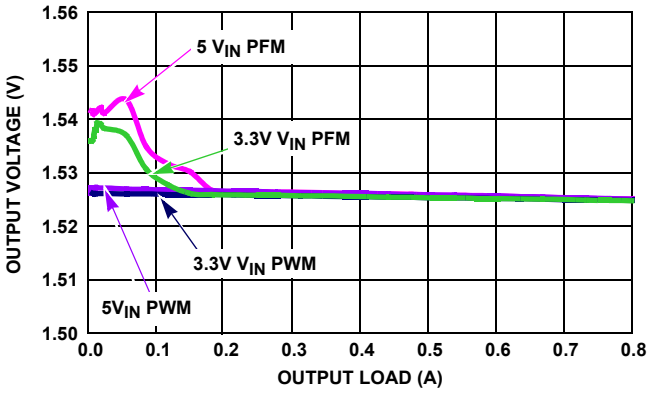


FIGURE 8. V_{OUT} REGULATION vs LOAD 2.25MHz, 1.5V_{OUT}

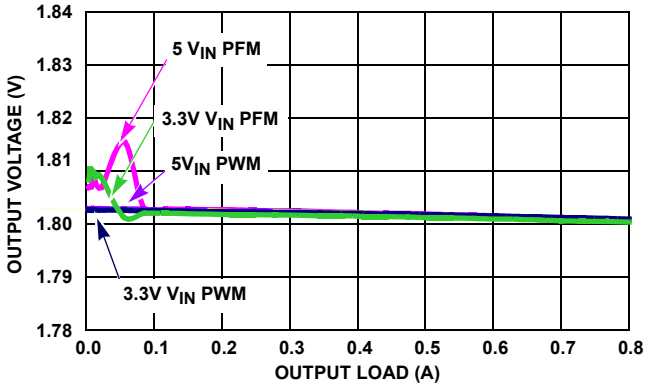


FIGURE 9. V_{OUT} REGULATION vs LOAD 2.25MHz, 1.8V_{OUT}

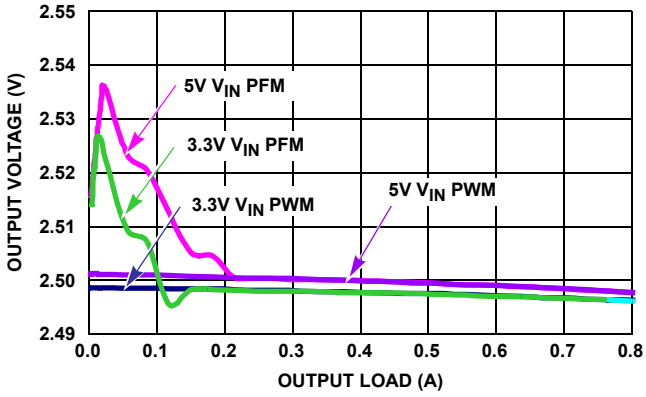


FIGURE 10. V_{OUT} REGULATION vs LOAD 2.25MHz, 2.5V_{OUT}

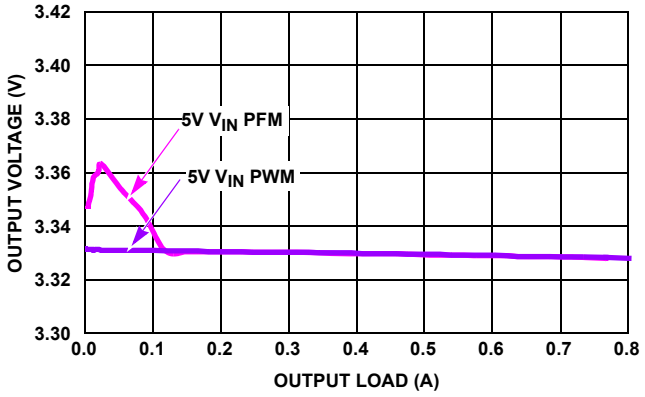


FIGURE 11. V_{OUT} REGULATION vs LOAD 2.25MHz, 3.3V_{OUT}

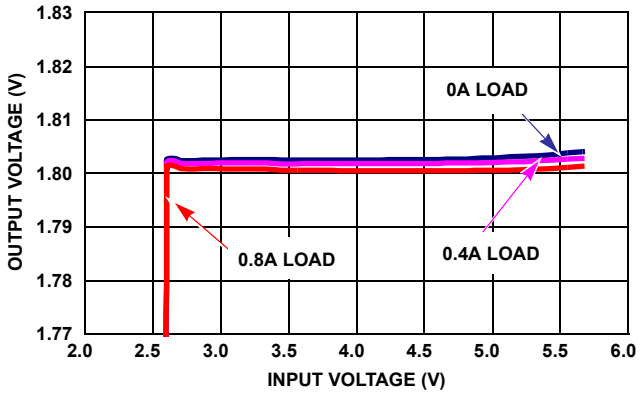


FIGURE 12. OUTPUT VOLTAGE REGULATION vs V_{IN} 1.8V_{OUT} PWM MODE

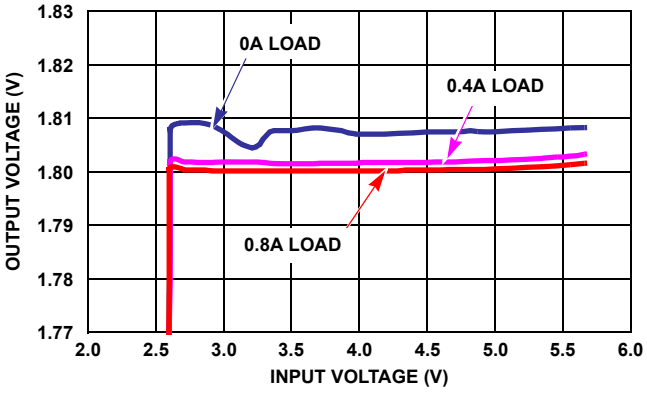


FIGURE 13. OUTPUT VOLTAGE REGULATION vs V_{IN} 1.8V_{OUT} PFM MODE

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.75V to 5.5V, EN = V_{IN}, L_1 = L_2 = 2.2µH, C_1 = 10µF, C_2 = C_4 = 10µF, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 800mA. **(Continued)**

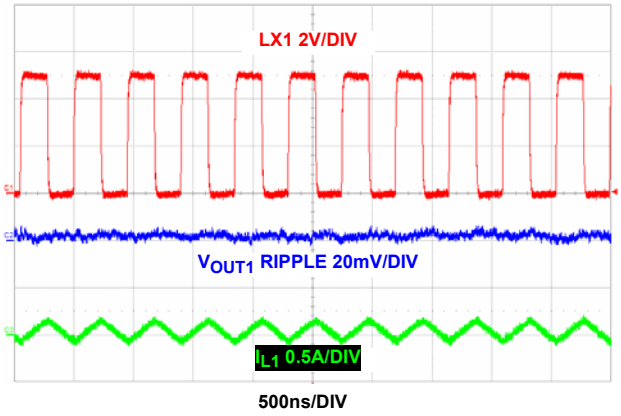


FIGURE 14. STEADY STATE OPERATION AT NO LOAD CHANNEL 1 (PWM)

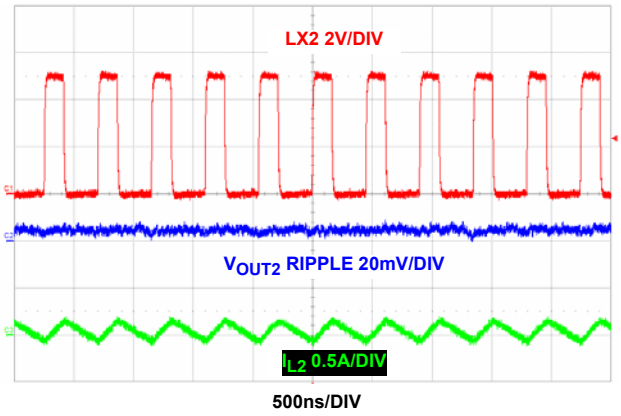


FIGURE 15. STEADY STATE OPERATION AT NO LOAD CHANNEL 2 (PWM)

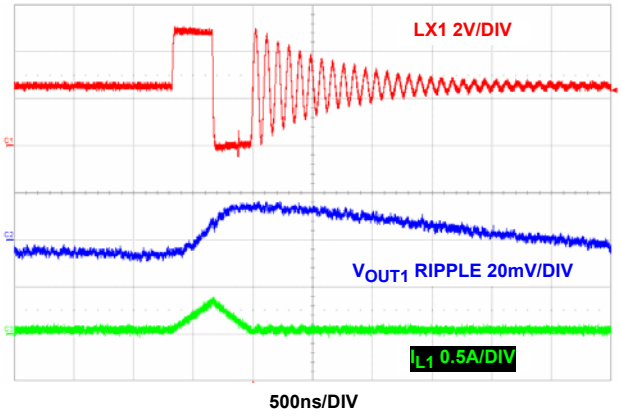


FIGURE 16. STEADY STATE OPERATION AT NO LOAD CHANNEL 1 (PFM)

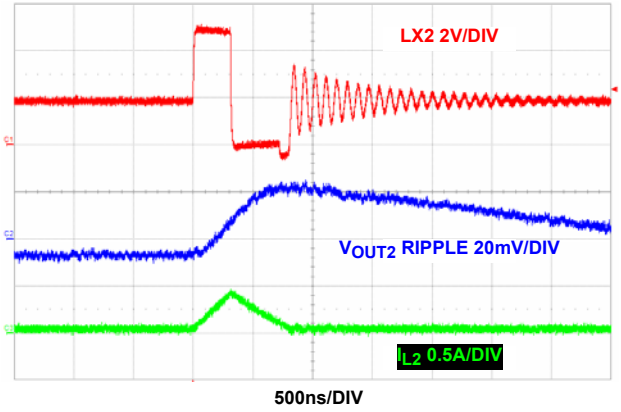


FIGURE 17. STEADY STATE OPERATION AT NO LOAD CHANNEL 2 (PFM)

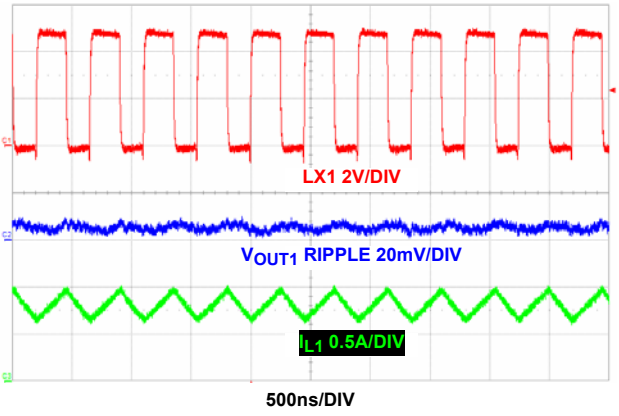


FIGURE 18. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 1

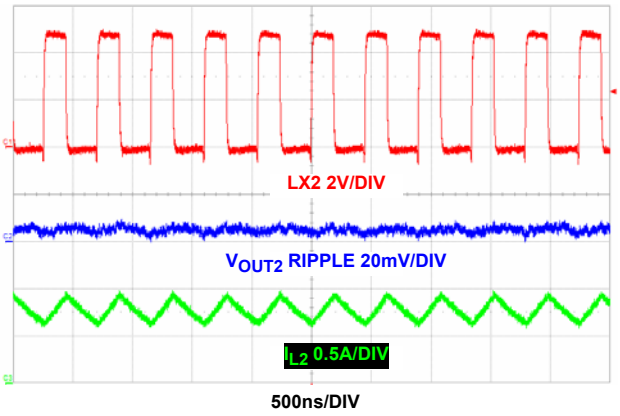


FIGURE 19. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 2

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.75V to 5.5V, EN = V_{IN}, L_1 = L_2 = 2.2µH, C_1 = 10µF, C_2 = C_4 = 10µF, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 800mA. **(Continued)**

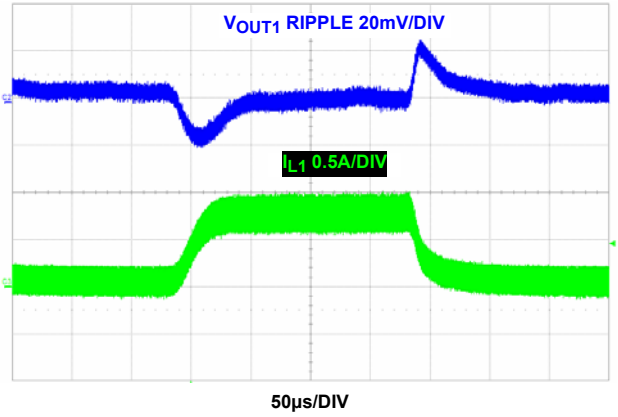


FIGURE 20. LOAD TRANSIENT CHANNEL 1 (PWM)

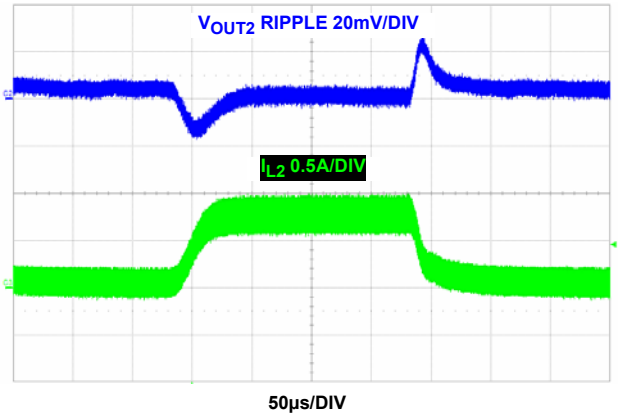


FIGURE 21. LOAD TRANSIENT CHANNEL 2 (PWM)

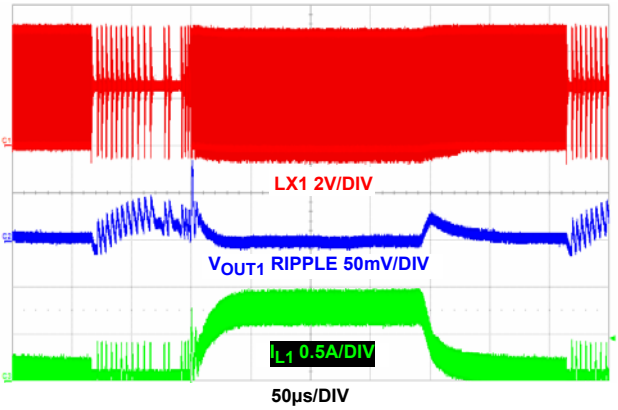


FIGURE 22. LOAD TRANSIENT CHANNEL 1 (PFM)

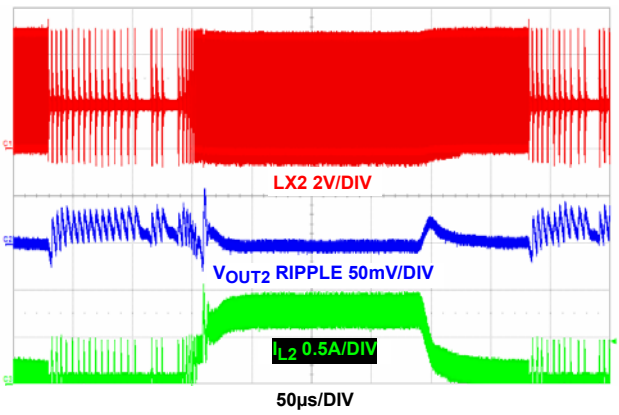


FIGURE 23. LOAD TRANSIENT CHANNEL 2 (PFM)

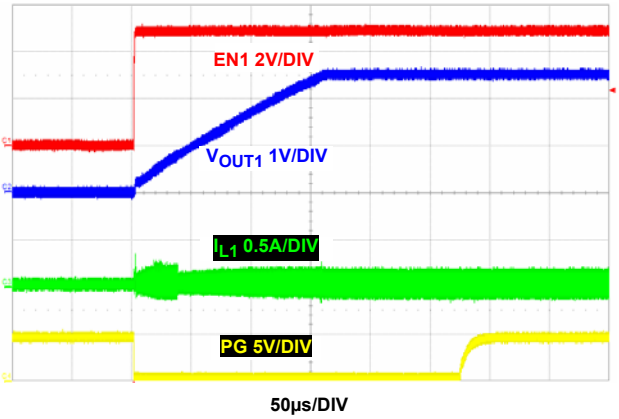


FIGURE 24. SOFT-START WITH NO LOAD CHANNEL 1 (PWM)

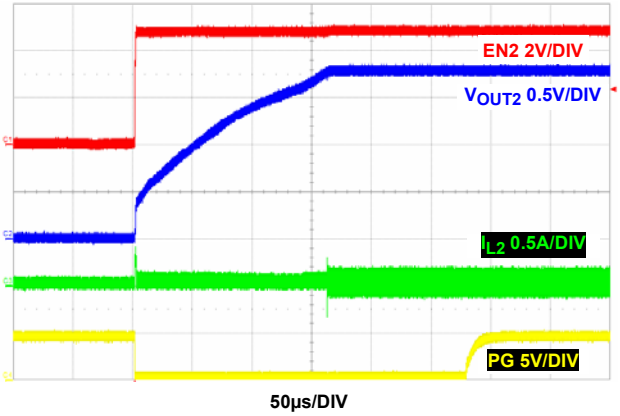


FIGURE 25. SOFT-START WITH NO LOAD CHANNEL 2 (PWM)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.75V to 5.5V, EN = V_{IN}, L_1 = L_2 = 2.2µH, C_1 = 10µF, C_2 = C_4 = 10µF, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 800mA. **(Continued)**

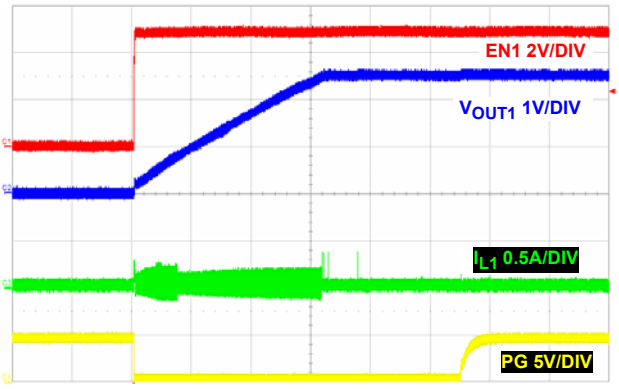


FIGURE 26. SOFT-START AT NO LOAD CHANNEL 1 (PFM)

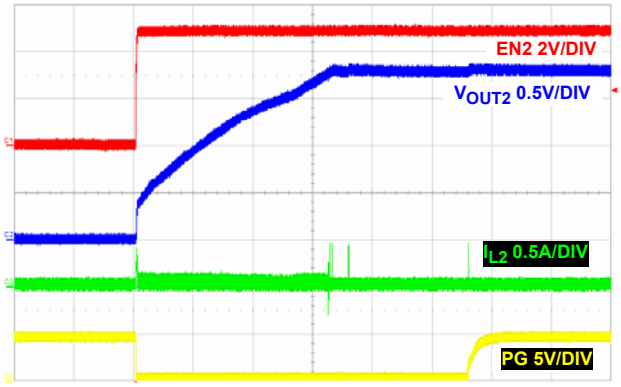


FIGURE 27. SOFT-START AT NO LOAD CHANNEL 2 (PFM)

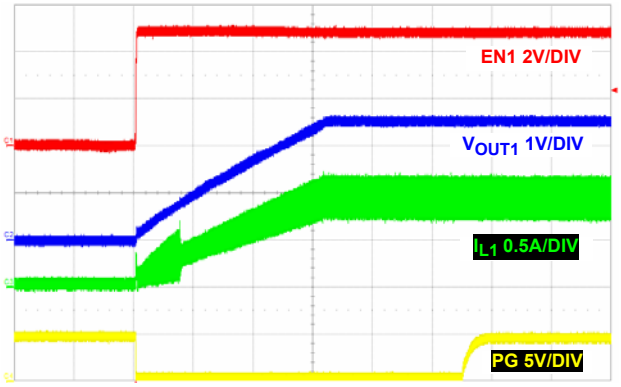


FIGURE 28. SOFT-START AT FULL LOAD CHANNEL 1

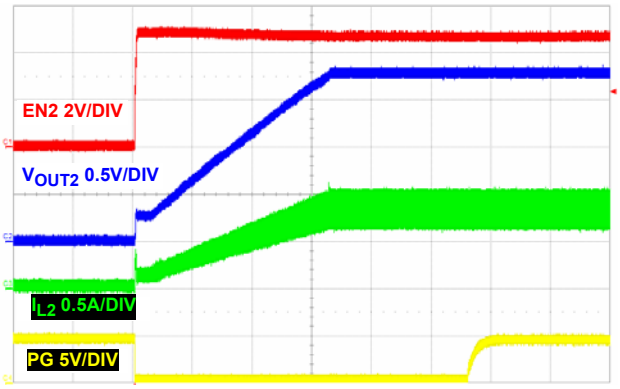


FIGURE 29. SOFT-START AT FULL LOAD CHANNEL 2

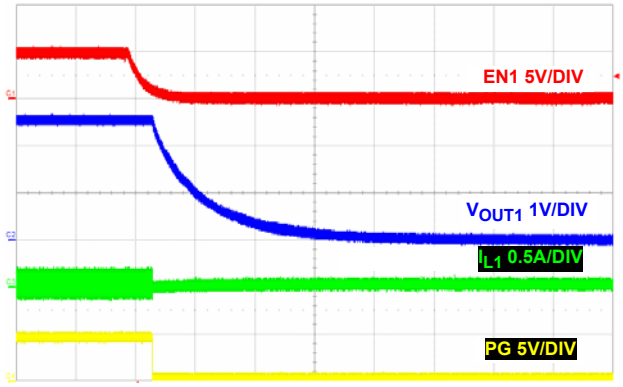


FIGURE 30. SOFT-DISCHARGE SHUTDOWN CHANNEL 1

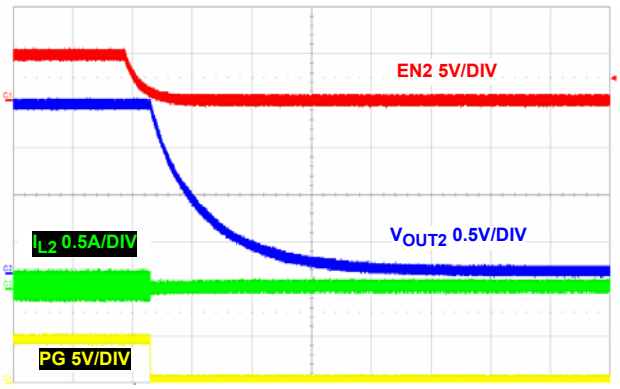


FIGURE 31. SOFT-DISCHARGE SHUTDOWN CHANNEL 2

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.75V to 5.5V, EN = V_{IN}, L_1 = L_2 = 2.2µH, C_1 = 10µF, C_2 = C_4 = 10µF, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 800mA. **(Continued)**

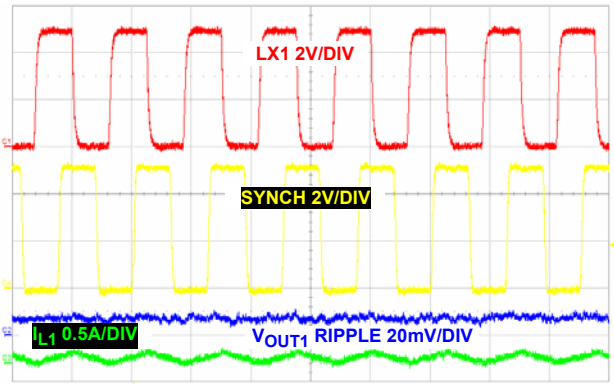


FIGURE 32. CH1 STEADY STATE OPERATION AT NO LOAD (PFM) WITH FREQUENCY = 4MHz

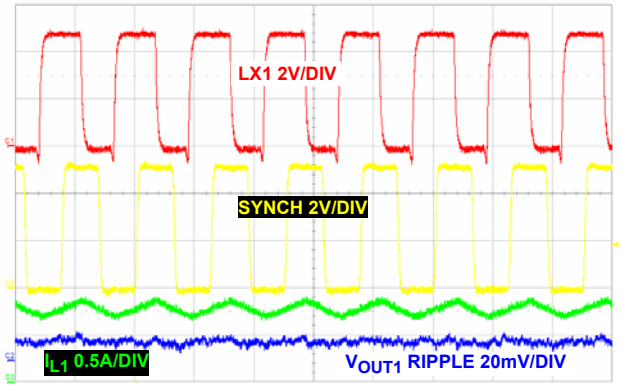


FIGURE 33. CH1 STEADY STATE OPERATION AT FULL LOAD (PFM) WITH FREQUENCY = 4MHz

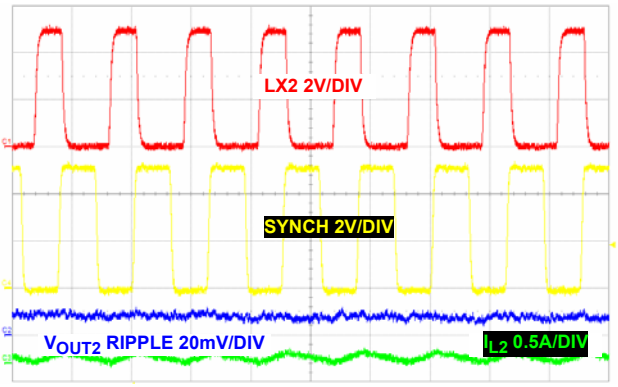


FIGURE 34. CH2 STEADY STATE OPERATION AT NO LOAD (PFM) WITH FREQUENCY = 4MHz

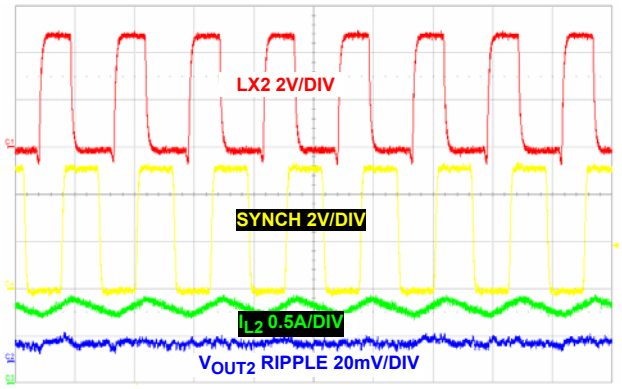


FIGURE 35. CH2 STEADY STATE OPERATION AT FULL LOAD (PFM) WITH FREQUENCY = 4MHz

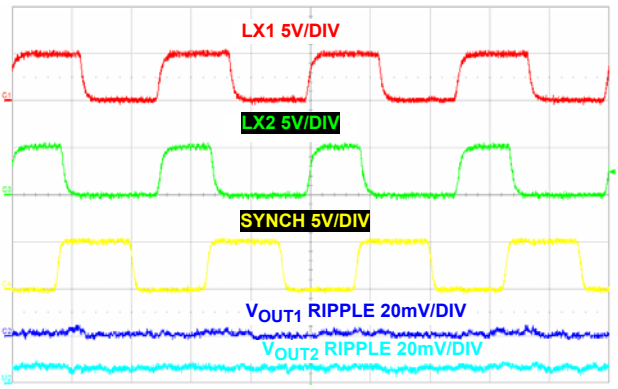


FIGURE 36. CH1 AND CH2 STEADY STATE OPERATION AT NO LOAD (PFM) WITH FREQUENCY = 4MHz

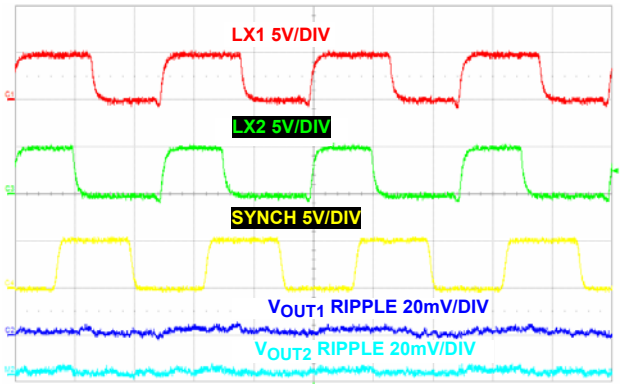


FIGURE 37. CH1 AND CH2 STEADY STATE OPERATION AT FULL LOAD (PFM) WITH FREQUENCY = 4MHz

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.75V to 5.5V, EN = V_{IN}, L_1 = L_2 = 2.2µH, C_1 = 10µF, C_2 = C_4 = 10µF, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 800mA. **(Continued)**

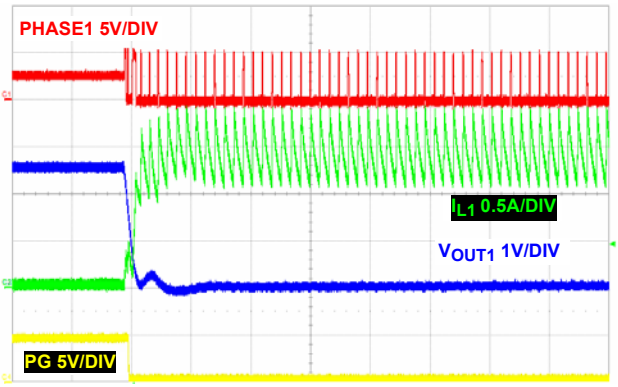


FIGURE 38. OUTPUT SHORT CIRCUIT CHANNEL 1

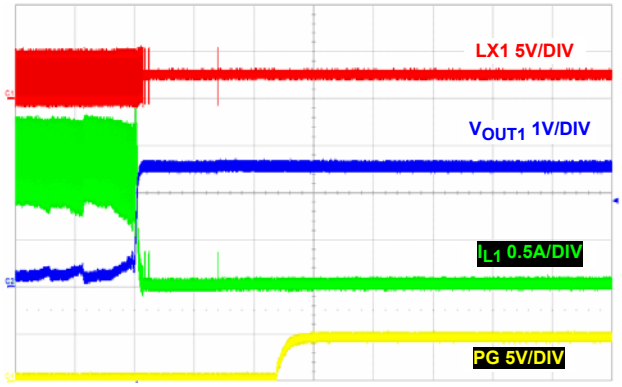


FIGURE 39. OUTPUT SHORT CIRCUIT RECOVERY CHANNEL 1

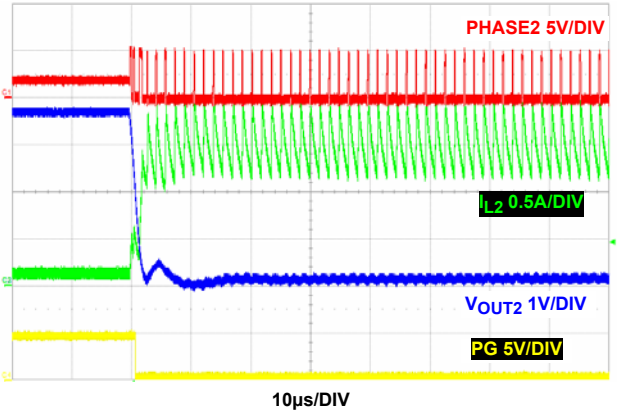


FIGURE 40. OUTPUT SHORT CIRCUIT CHANNEL 2

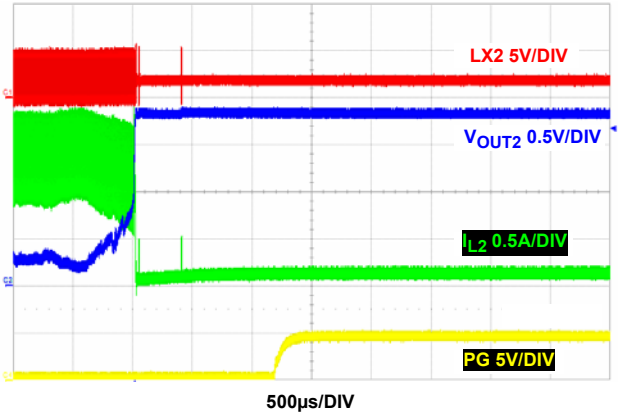


FIGURE 41. OUTPUT SHORT CIRCUIT RECOVERY CHANNEL 2

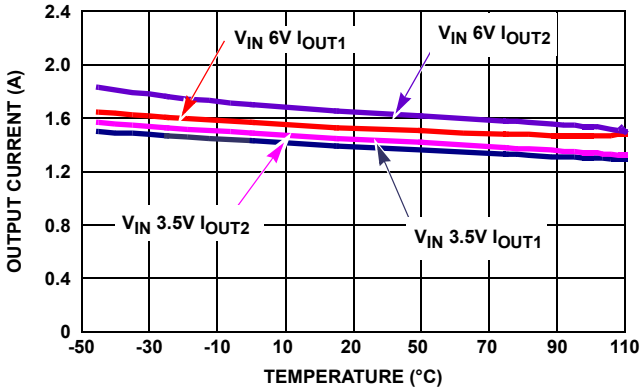
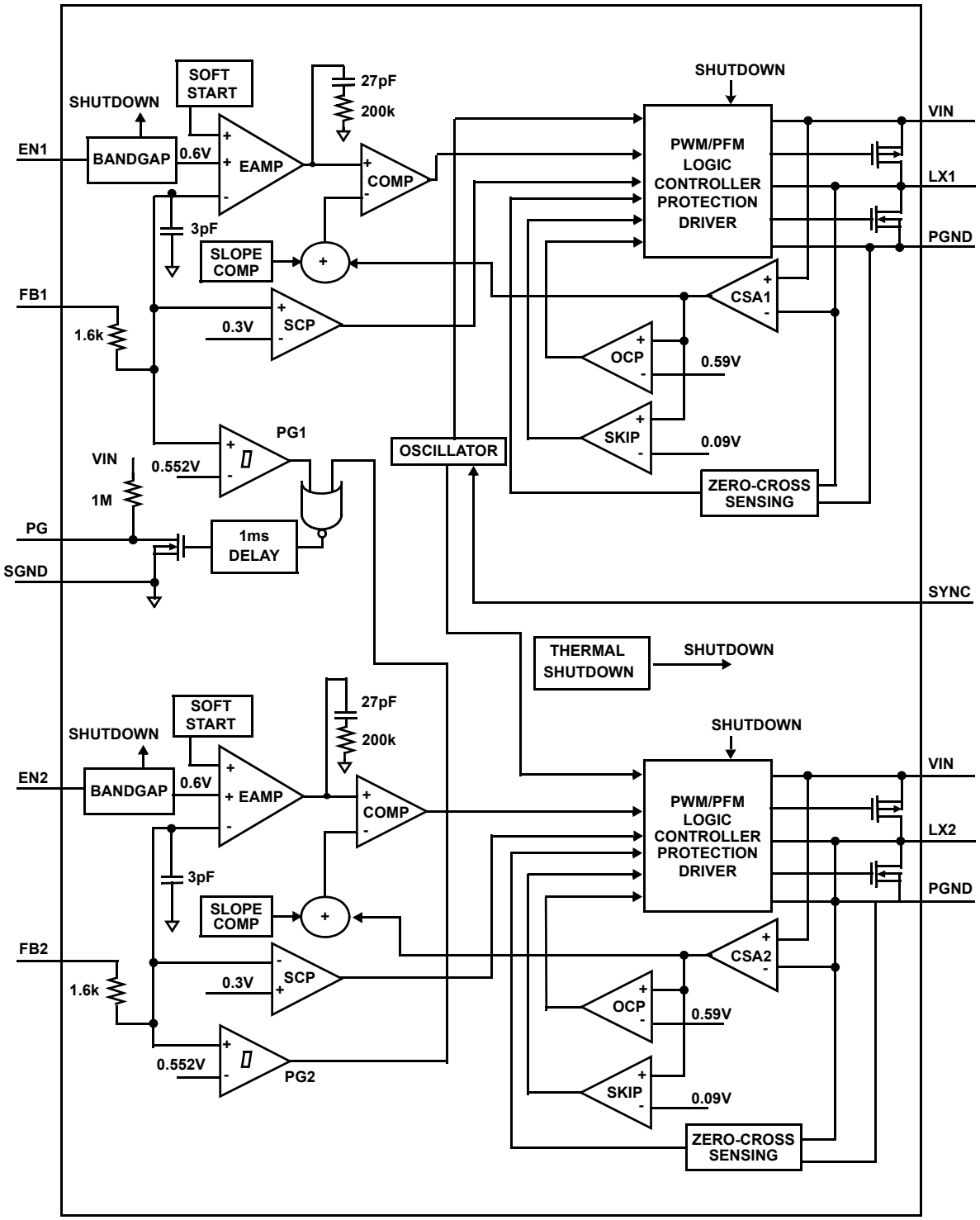


FIGURE 42. OUTPUT CURRENT LIMIT vs TEMPERATURE

Block Diagram



Theory of Operation

The ISL78228 is a dual 800mA step-down switching regulator optimized for battery-powered or mobile applications. The regulator operates at a 2.25MHz fixed switching frequency under heavy load conditions to allow small external inductor and capacitors to be used for minimal printed-circuit board (PCB) area. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The two channels are in-phase operation. The quiescent current when the outputs are not loaded is typically only 30µA. The supply current is typically only 6.5µA when the regulator is shut down.

PWM Control Scheme

Pulling the SYNC pin LOW (<0.4V) forces the converter into PWM mode in the next switching cycle regardless of output current. Each of the channels of the ISL78228 employ the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting shown in the "Block Diagram" on page 13. The current loop consists of the oscillator, the PWM comparator COMP, current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-Channel MOSFET when it is turned on and the current sense amplifier CSA1 (or CSA2 on Channel 2). The gain for the current sensing circuit is typically 0.285V/A. The control reference for the current loops comes from the error amplifier EAMP of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp-up. When the sum of the current amplifier CSA1 (or CSA2) and the compensation slope (0.33V/µs) reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-MOSFET and to turn on the N-Channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 43 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier CSA_output.

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage control loop. The feedback signal comes from the V_{FB} pin. The soft-start block only affects the operation during the start-up and will be discussed separately shortly. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 200kΩ RC network. The maximum EAMP voltage output is precisely clamped to 0.8V.

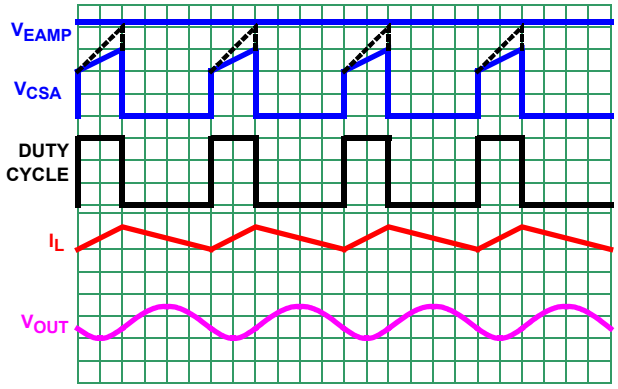


FIGURE 43. PWM OPERATION WAVEFORMS

SKIP Mode

Pulling the SYNC pin HIGH (>2.0V) forces the converter into PFM mode. The ISL78228 enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 44 illustrates the skip-mode operation. A zero-cross sensing circuit shown in the "Block Diagram" on page 13 monitors the N-MOSFET current for zero crossing. When 8 consecutive cycles of the N-MOSFET crossing zero are detected, the regulator enters the skip mode. During the 8 detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

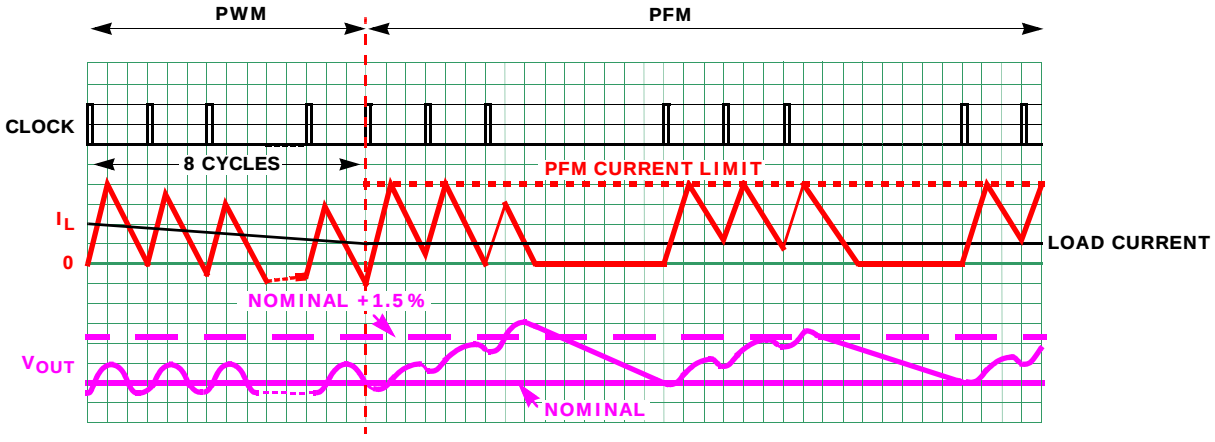


FIGURE 44. SKIP MODE OPERATION WAVEFORMS

Once the skip mode is entered, the pulse modulation starts being controlled by the SKIP comparator shown in the "Block Diagram" on page 13. Each pulse cycle is still synchronized by the PWM clock. The P-MOSFET is turned on at the clock and turned off when its current reaches the threshold of 250mA. As the average inductor current in each cycle is higher than the average current of the load, the output voltage rises cycle over cycle. When the output voltage reaches 1.5% above the nominal voltage, the P-MOSFET is turned off immediately. Then the inductor current is fully discharged to zero and stays at zero. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-MOSFET will be turned on again at the clock, repeating the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.5% below the nominal voltage.

Synchronization Control

The frequency of operation can be synchronized up to 4MHz by an external signal applied to the SYNC pin. The falling edge on the SYNC triggered the rising edge of the PWM ON pulse.

Overcurrent Protection

The CSA1 and CSA2 are used to monitor output 1 and output 2 channels respectively. The overcurrent protection is realized by monitoring the CSA_ output with the OCP threshold logic, as shown in the "Block Diagram" on page 13. The current sensing circuit has a gain of 0.285V/A, from the P-MOSFET current to the CSA_output. When the CSA_ output reaches the threshold of 590mV, the OCP comparator is tripped to turn off the P-MOSFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFETs.

Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle.

PG

The power-good signal, (PG) monitors both of the output channels. When powering up, the open-collector power-on-reset output holds low for about 1ms after V_{OUT1} and V_{OUT2} reaches the preset voltages. The PG output also serves as a 1ms delayed Power-Good signal. If one of the output is disabled, then PG only monitors the active channels. There is an internal 1MΩ pull-up resistor.

TABLE 1. POWER-GOOD

EN1	EN2	PG1 INTERNAL	PG2 INTERNAL	PG
0	0	X	X	0
0	1	X	1	1
1	0	1	X	1
1	1	1	1	1

UVLO

When the input voltage is below the undervoltage lock out (UVLO) threshold, the regulator is disabled.

Enable

The enable (EN1, EN2) input allows the user to control the turning on or off of the regulator for purposes such as power-up sequencing. The regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference, then the soft start-up begins.

Soft-Start-Up

The soft-start-up eliminates the in-rush current during the start-up. The soft-start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage speed so that the output voltage rises in a controlled fashion. At the very beginning of the start-up, the output voltage is less than 0.2V; hence the PWM operating frequency is 1/3 of the normal frequency.

In force PWM mode, the IC will continue to start-up in PFM mode to support pre-biased load applications.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs, or the output undervoltage fault latch is set, the outputs discharge to GND through an internal 100Ω switch.

Power MOSFETs

The power MOSFETs are optimized for best efficiency. The ON-resistance for the P-MOSFET and N-MOSFET is typically 180mΩ.

100% Duty Cycle

The ISL78228 features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL78228 can no longer maintain the regulation at the output, the regulator completely turns on the P-MOSFET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-MOSFET.

Thermal Shut-Down

The ISL78228 has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops to +130°C, the ISL78228 resumes operation by stepping through a soft-start-up.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operation, the ISL78228 typically uses a 2.2µH output inductor. Higher or lower inductor values can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V applications, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. The inductor ripple current can be expressed as shown in Equation 1:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 1)}$$

The inductor's saturation current rating needs to be at least larger than the peak current. The ISL78228 protects the typical peak current 1.2A. The saturation current needs to be over 1.8A for maximum output current application.

The ISL78228 uses internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended minimum output capacitor values are shown in Table 2 for the ISL78228.

TABLE 2. OUTPUT CAPACITOR VALUE vs V_{OUT}

V_{OUT} (V)	C_{OUT} (µF)	L (µH)
0.8	10	1.0~2.2
1.2	10	1.0~2.2
1.6	10	1.0~2.2
1.8	10	1.5~3.3
2.5	10	1.5~3.3
3.3	6.8	1.5~4.7
3.6	8.6	1.5~4.7

In Table 2, the minimum output capacitor value is given for different output voltages to make sure the whole converter system is stable.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier. Refer to "Typical Application" on page 2.

The output voltage programming resistor, R_2 (or R_5 in Channel 2), will depend on the desired output voltage of the regulator. The value for the feedback resistor is typically between 0Ω and 750kΩ, as shown in Equation 2.

Let R_3 = 100kΩ, then R_2 will be:

$$R_2 = R_3\left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad \text{(EQ. 2)}$$

If the output voltage desired is 0.6V, then R_3 is left unpopulated and short R_2. For faster response performance, add 47pF in parallel to R_2.

Input Capacitor Selection

The main functions of the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. One 10µF X5R or X7R ceramic capacitor is a good starting point for the input capacitor selection for both channels.

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For ISL78228, the power loop is composed of the output inductor (L's), the output capacitor (C_{OUT1} and C_{OUT2}), the LX's pins, and the GND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the LX_ pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as closely as possible to the VIN pin. The ground of input and output capacitors should be connected as closely as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 5 vias ground connection within the pad for the best thermal relief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
April 13, 2015	FN7849.3	"Absolute Maximum Ratings (Reference to GND)" on page 4: Updated CDM testing from: Charged Device Model (Tested per JESD22-C101E) to Charged Device Model (Tested per AEC-Q100-011). Updated POD L10.3x3C to most current revision with changes as follows: Tiebar Note 4 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
December 4, 2013	FN7849.2	Page 1: changed last paragraph in description from: "The ISL78228 is rated for the automotive temperature range (-40°C to +105°C)." to: "The ISL78228 is AEC-Q100 rated. The ISL78228 is rated for the automotive temperature range (-40°C to +105°C)." Features bullet changed from: "Qualified for automotive applications" to: "AEC-Q100 Tested"
October 22, 2013	FN7849.1	Page 1 - Added the words "Qualified for automotive applications" under the Features section
May 2, 2011	FN7849.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

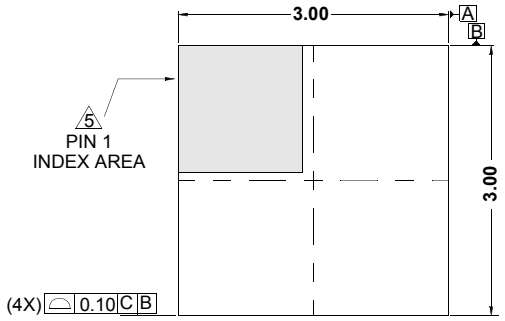
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

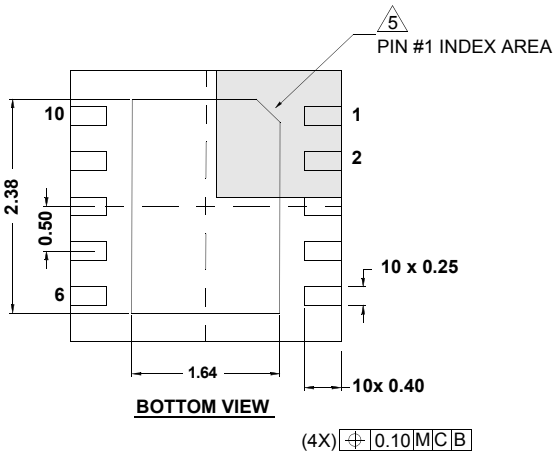
L10.3x3C

10 LEAD DUAL FLAT PACKAGE (DFN)

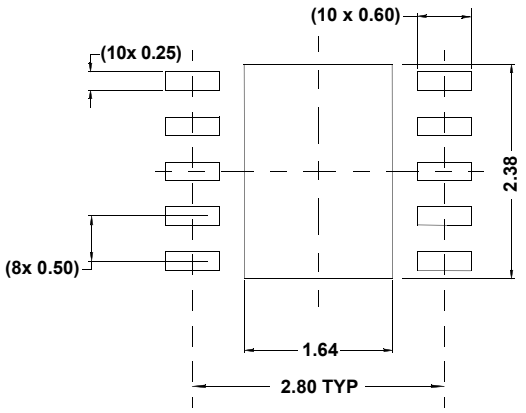
Rev 4, 3/15



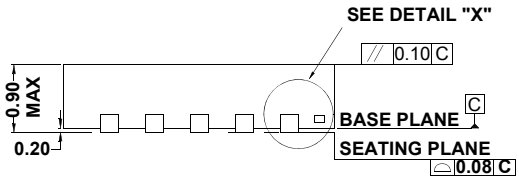
TOP VIEW



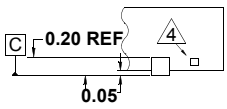
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Compliant to JEDEC MO-229-WEED-3 except for E-PAD dimensions.