To request the full datasheet, please visit www.intersil.com/products/isl78600

Multi-Cell Li-Ion Battery Manager

ISL78600

The ISL78600 Li-ion battery manager IC supervises up to 12 series connected cells. The part provides accurate monitoring, cell balancing and extensive system diagnostics functions. Three cell balancing modes are incorporated: Manual Balance mode, Timed Balance mode, and Auto Balance mode. The auto balance mode terminates balancing functions when a charge transfer value specified by the host microcontroller has been met.

The ISL78600 communicates to a host microcontroller via an SPI interface and to other ISL78600 devices using a robust, proprietary, two-wire Daisy Chain system.

The ISL78600 is offered in a 64 Ld TQFP package and is specified for operation at a temperature range of -40°C to +105°C.

Applications

- Hybrid Electric Vehicle (HEV), Plug-in Hybrid Electric Vehicle (PHEV) and Electric Vehicle (EV) battery packs
- Electric motorcycle battery packs
- Backup battery and energy storage systems requiring high accuracy management and monitoring
- Portable and semiportable equipment

Features

- Up to 12-cell voltage monitors, support Li-ion CoO_2, Li-ion Mn_2O_4, and Li-ion FePO4 chemistries
- Cell voltage measurement accuracy ±2.5mV
- 13-bit cell voltage measurement
- Pack voltage measurement accuracy ±100mV
- 14-bit pack voltage and temperature measurements
- Cell voltage scan rate of 19.5µs per cell (234µs to scan 12 cells)
- Internal and external temperature monitoring
- Up to four external temperature inputs
- Robust Daisy Chain communications system
- Integrated system diagnostics for all key internal functions
- Hardwired and communications based fault notification
- Integrated watchdog shuts down device if communication is lost
- 7µA shutdown current: Enable = V_{SS}
- 2Mbps SPI

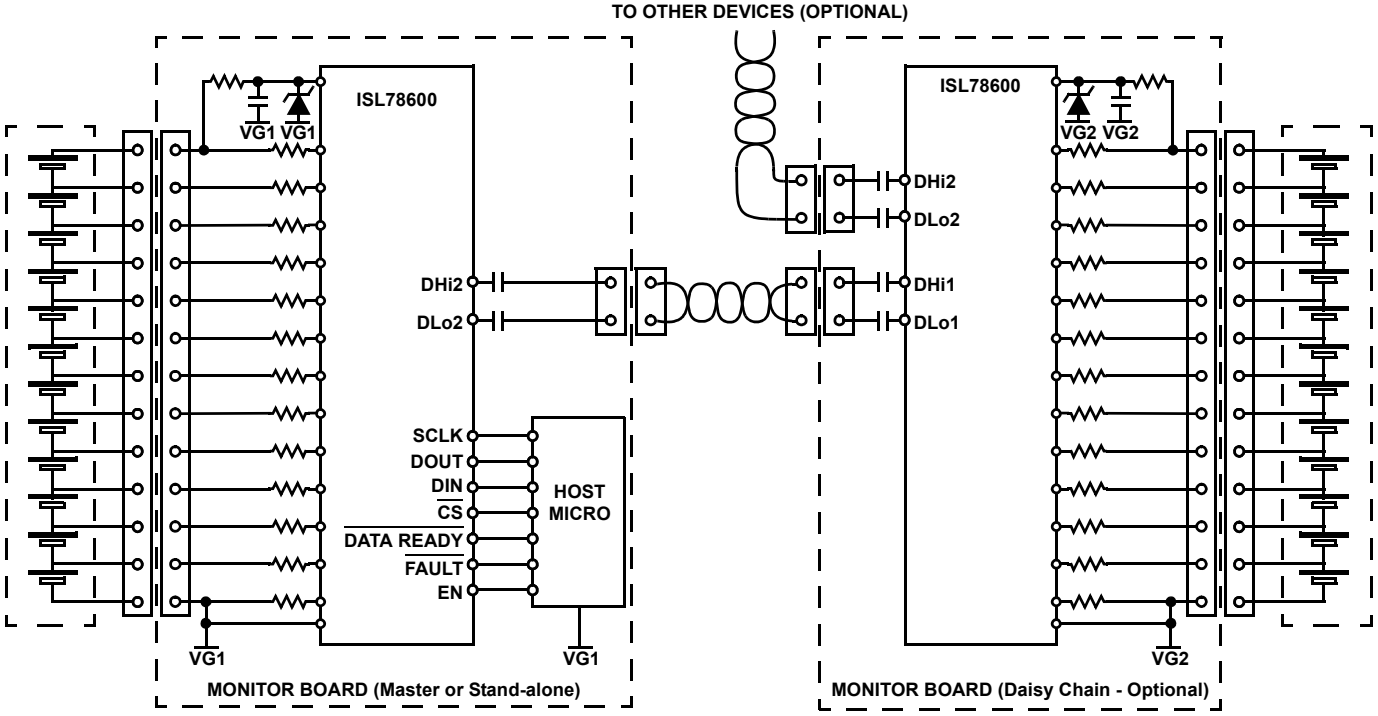

FIGURE 1. TYPICAL APPLICATION

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Ordering Information

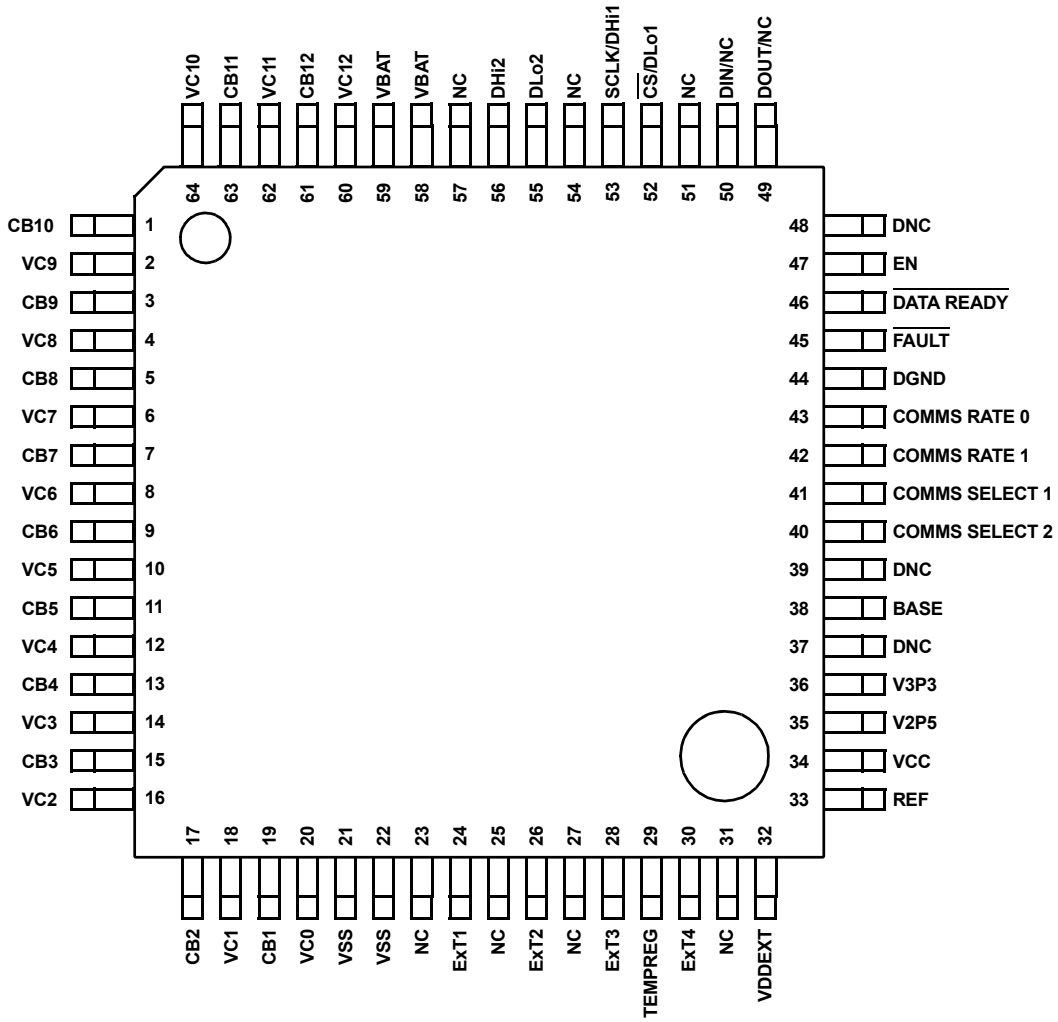
PART NUMBER (Notes 1, 2, 3, 4)	PART MARKING	TRIM VOLTAGE, V_{NOM} (V)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL78600ANZ	ISL78600ANZ	3.3	-40 to +105	64 Ld TQFP	Q64.10x10D
ISL78600/601EVAL1Z	Evaluation Board for ISL78600				

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For more information on handling and processing moisture sensitive devices, please see Techbrief TB363.
4. For other trim options, please contact Intersil Automotive Marketing.

Pin Configuration

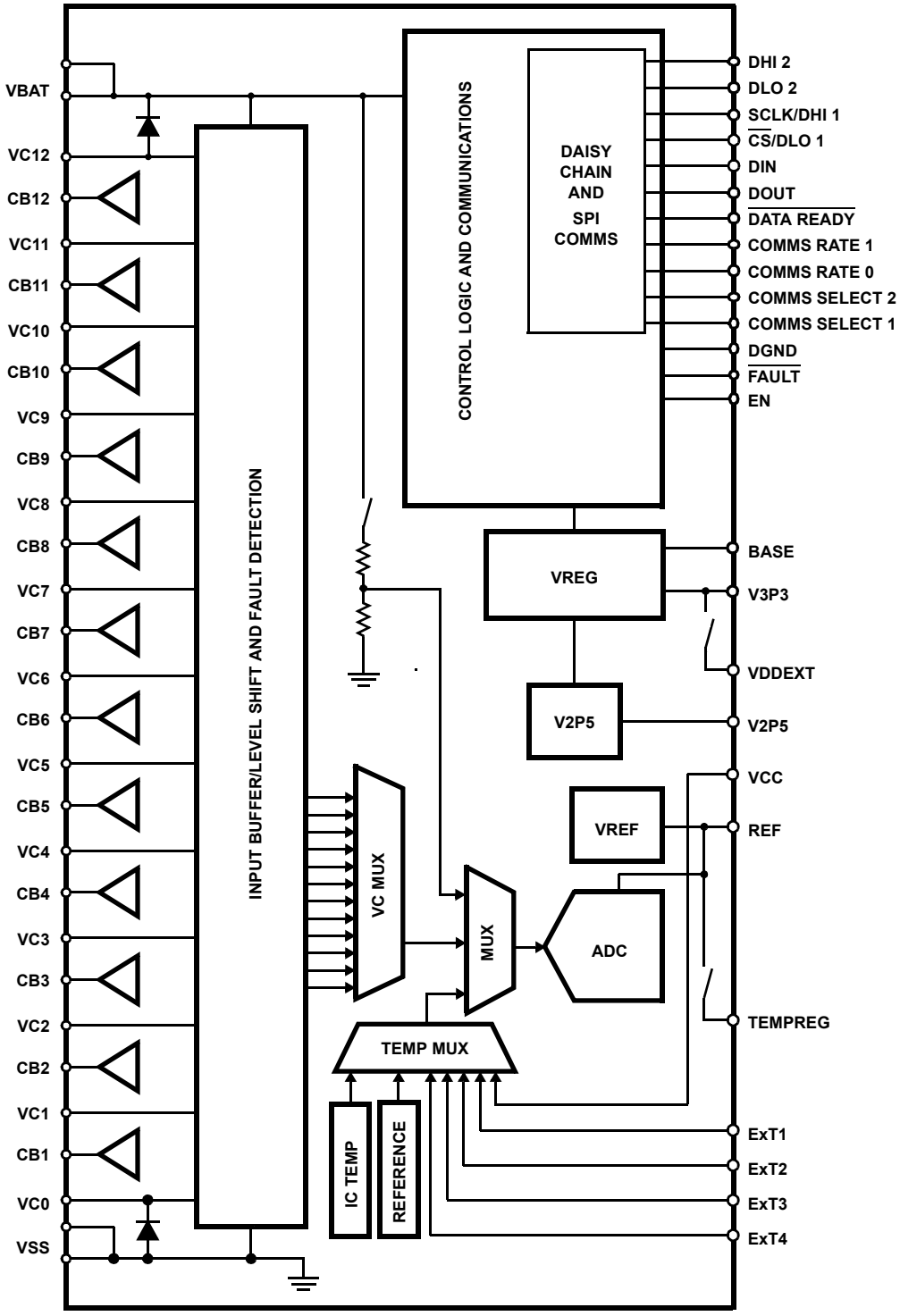
ISL78600
(64 LD 10x10 TQFP)
TOP VIEW



Pin Descriptions

SYMBOL	PIN NUMBER	DESCRIPTION
VC0, VC1, VC2, VC3, VC4, VC5, VC6, VC7, VC8, VC9, VC10, VC11, VC12	20, 18, 16, 14, 12, 10, 8, 6, 4, 2, 64, 62, 60	Battery cell voltage inputs. VCn connects to the positive terminal of CELLn and the negative terminal of CELLn+1. (VC12 connects only to the positive terminal of CELL12 and VC0 only connects with the negative terminal of CELL1.)
CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12	19, 17, 15, 13, 11, 9, 7, 5, 3, 1, 63, 61	Cell Balancing FET control outputs. Each output controls an external FET which provides a current path around the cell for balancing.
VBAT	58, 59	Main IC Supply pins. Connect to the most positive terminal in the battery string.
VSS	21, 22	Ground. These pins connect to the most negative terminal in the battery string.
ExT1, ExT2, ExT3, ExT4	24, 26, 28, 30	External temperature monitor or general purpose inputs. The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements but may also be used as general purpose analog inputs at the user's discretion. 0V to 2.5V input range.
TEMPREG	29	Temperature monitor voltage regulator output. This is a switched 2.5V output which supplies a reference voltage to external NTC thermistor circuits to provide ratiometric ADC inputs for temperature measurement.
VDDEXT	32	External V3P3 supply input/output. Connected to the V3P3 pin via a switch, this pin may be used to power external circuits from the V3P3 supply. The switch is open when the ISL78600 is placed in **Sleep mode**.
REF	33	2.5V voltage reference decoupling pin. Connect a 2.0µF to 2.5µF X7R capacitor to VSS. Do not connect any additional external load to this pin.
VCC	34	Analog supply voltage input. Connect to V3P3 via a 33Ω resistor. Connect a 1µF capacitor to ground.
V2P5	35	Internal 2.5V digital supply decoupling pin. Connect a 1µF capacitor to DGND.
V3P3	36	3.3V digital supply voltage input. Connect the emitter of the external NPN regulator transistor to this pin. Connect a 1µF capacitor to DGND.
BASE	38	Regulator control pin. Connect the external NPN transistor's base. Do not let this pin float.
DNC	37, 39, 48	Do not connect. Leave pins floating.
COMMS SELECT 1	41	Communications port 1 mode select pin. Connect via a 1kΩ resistor to V3P3 for Daisy Chain communications on port 1 or to DGND for SPI operation on port 1.
COMMS SELECT 2	40	Communications port 2 mode select pin. Connect via a 1kΩ resistor to V3P3 to enable port 2 or to DGND to disable this port.
COMMS RATE 0, COMMS RATE 1	43, 42	Daisy Chain communications data rate setting. Connect via a 1kΩ resistor to DGND ('0') or to V3P3 ('1') to select between various communication data rates.
DGND	44	Digital Ground.
$\overline{\text{FAULT}}$	45	Logic fault output. Asserted low if a fault condition exists.
$\overline{\text{DATA READY}}$	46	SPI data ready. Asserted low when the device is ready to transmit data to the host microcontroller.
EN	47	Enable input. Tie to V3P3 to enable the part. Tie to DGND to disable (all IC functions are turned off).
DOUT/NC	49	Serial Data Output (SPI) or NC (Daisy Chain). 0V to 3.3V push-pull output.
DIN/NC	50	Serial Data Input (SPI) or NC (Daisy Chain). 0V to 3.3V input.
$\overline{\text{CS}}$/DLo1	52	Chip-Select, active low 3.3V input (SPI) or Daisy Chain port 1 Lo connection.
SCLK/DHi1	53	Serial-Clock Input (SPI) or Daisy Chain port 1 Hi connection.
DHi2	56	Daisy Chain port 2 Hi connection.
DLo2	55	Daisy Chain port 2 Lo connection.
NC	23, 25, 27, 31, 51, 54, 57	No internal connection.

Block Diagram



Absolute Maximum Ratings

Unless otherwise specified. With respect to VSS.

DIN, SCLK, $\overline{CS}$, DOUT, $\overline{DATA\ READY}$, COMMS SELECT n, ExTn, TEMPREG, REF, V3P3, VCC, $\overline{FAULT}$, COMMS RATE n, BASE, EN, VDDEXT . . . . . -0.2V to 4.1V
V2P5. . . . . -0.2V to 2.9V
VBAT . . . . . -0.5V to 63V
Dhi1, DLo1, DHi2, DLo2 . . . . . -0.5V to (VBAT + 0.5V)
VC0 . . . . . -0.5V to +9.0V
VC1 . . . . . -0.5V to +18V
VC2 . . . . . -0.5V to +18V
VC3 . . . . . -0.5V to +27V
VC4 . . . . . -0.5V to +27V
VC5 . . . . . -0.5V to +36V
VC6 . . . . . -0.5V to +36V
VC7 . . . . . -0.5V to +45V
VC8 . . . . . -0.5V to +45V
VC9 . . . . . -0.5V to +54V
VC10 . . . . . -0.5V to +63V
VC11 . . . . . -0.5V to +63V
VC12 . . . . . -0.5V to +63V
VCn (for n = 0 to 12). . . . . -0.5 to VBAT +0.5V
CBn (for n = 1 to 12) . . . . . -0.5 to VBAT +0.5V
CBn (for n = 1 to 9) . . . . . V(VCn-1) -0.5V to V(VCn-1) +9V
CBn (for n = 10 to 12). . . . . V(VCn) -9V to V(VCn) +0.5V
Current into VCn, VBAT, VSS (Latch-up Test) . . . . . ±100mA
ESD Rating
  Human Body Model (Tested per JESD22-A114F) 2kV
  Capacitive Discharge Model (Tested per JESD22-C101D). 500V
Latch-up (Tested per JESD-78B; Class 2, Level A) 100mA

NOTE: DOUT, $\overline{DATA\ READY}$, and $\overline{FAULT}$ are digital outputs and should not be driven from external sources. V2P5, REF, TEMPREG and BASE are analog outputs and should not be driven from external sources.

Thermal Information

Thermal Resistance (Typical)	θ_{JA}(C/W)	θ_{JC}(C/W)
64 Ld TQFP Package (Notes 5, 6)	49	9

Max Continuous Package Power Dissipation 400mW
Storage Temperature . . . . . -55°C to +125°C
Max Operating Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . Refer to JEDEC J STD 020D

Recommended Operating Conditions

T_A, Ambient Temperature Range . . . . . -40°C to +105°C
V_{BAT} . . . . . 6V to 60V
V_{BAT} (Daisy Chain Operation) . . . . . 10V to 60V
VCn (for n = 1 to 12) . . . . . V(VCn-1) to V(VCn-1) + 5V
VC0 . . . . . -0.1V to 0.1V
CBn (for n = 1 to 9) . . . . . V(VCn-1) to V(VCn-1) + 9V
CBn (for n = 10 to 12). . . . . V(VCn) -9V to V(VCn)
DIN, SCLK, $\overline{CS}$, COMMS SELECT 1, COMMS SELECT 2, V3P3, VCC, COMMS RATE 0, COMMS RATE 1, EN. . . . . 0V to 3.6V
ExT1, ExT2, ExT3, ExT4 . . . . . 0V to 2.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Power-Up Condition Threshold	V_{POR}	V_{BAT} voltage (rising)	4.8	5.1	5.6	V
Power-Up Condition Hysteresis	V_{PORhys}			400		mV
Initial Power-Up Delay	t_{POR}	Time after VPOR condition V_{REF} from 0V to 0.95 x V_{REF}(nom) (EN tied to V3P3) Device can now communicate			27.125	ms
Enable Pin Power-Up Delay	t_{PUD}	Delay after EN = 1 to V_{REF} from 0V to 0.95 x V_{REF}(nom) (V_{BAT} = 39.6V) - Device can now communicate			27.125	ms

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{BAT} Supply Current	I_{VBAT}	Non Daisy Chain configuration. Device enabled. No communications, ADC, measurement, balancing or open wire detection activity.				
		6V	7	35	80	µA
		39.6V	0	64	241	µA
		60V	0	90	250	µA
		-40°C to +105°C (Note 9)	0		280	µA
	$I_{VBATMASTER}$	Daisy Chain configuration – master device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.				
		6V	400	530	660	µA
		39.6V	500	680	900	µA
		60V	550	750	1000	µA
		-40°C to +105°C (Note 9)			1150	µA
		Peak current when Daisy Chain transmitting		18		mA
	$I_{VBATMID}$	Daisy Chain configuration – MIDDLE stack device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.				
		6V	700	1020	1210	µA
		39.6V	900	1250	1560	µA
		60V	1000	1400	1700	µA
		-40°C to +105°C (Note 9)			1850	µA
		Peak current when Daisy Chain transmitting		18		mA
	$I_{VBATTOP}$	Daisy Chain configuration – top device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.				
		6V	400	530	660	µA
		39.6V	500	680	900	µA
		60V	550	750	1000	µA
		-40°C to +105°C (Note 9)			1150	µA
		Peak Current when Daisy Chain transmitting		18		mA
	$I_{VBATSLEEP1}$ (Note 9)	Sleep mode (EN = 1, Daisy Chain configuration)				
		6V	14	18	23	µA
		39.6V	18	23	29	µA
		60V	20	25	30	µA
		-40°C to +105°C			41	µA
	$I_{VBATSLEEP2}$ (Note 9)	Sleep mode (EN = 1, Stand-alone, non-Daisy Chain)	3.5	8	16	µA
		-40°C to +105°C	3		70	µA
	$I_{VBATSHDN}$ (Note 9)	Shutdown. device “off” (EN = 0) (Daisy Chain and Non-Daisy Chain configurations)				
		6V	1.5	7	15.5	µA
		39.6V	3	7	18	µA
		60V	5	7	23	µA
		-40°C to +105°C	1		77	µA
V_{BAT} Supply Current Tracking. Sleep Mode.	$I_{VBAT\Delta SLEEP}$ (Note 9)	EN = 1, Daisy Chain Sleep Mode configuration. V_{BAT} current difference between any two devices operating at the same temperature and supply voltage.	0	4	8	µA
		-40°C to +105°C	0		17	µA

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{BAT} Incremental Supply Current, Balancing	$I_{VBATBAL}$	All balancing circuits on. Incremental current: Add to nonbalancing V_{BAT} current. V_{BAT} = 39.6V	250	300	350	µA
		-40°C to +105°C (Note 9)	200	300	400	µA
V3P3 Regulator Voltage (Normal)	V_{3P3N}	EN = 1, Load current range 0 to 5mA. V_{BAT} = 39.6V	3.25	3.35	3.45	V
		-40°C to +105°C (Note 9)	3.2		3.5	V
V3P3 Regulator Voltage (Sleep)	V_{3P3S}	EN = 1, Load current range. No load. (SLEEP). V_{BAT} = 39.6V	2.45	2.7	2.95	V
		-40°C to +105°C (Note 9)	2.4		3.05	V
V3P3 Regulator Control Current	I_{BASE}	Current sourced from BASE output. V_{BAT} = 6V	1	1.5		mA
		-40°C to +105°C (Note 9)	1			mA
V3P3 Supply Current	I_{V3P3}	Device Enabled No measurement activity, Normal Mode	0.8	1	1.2	mA
		-40°C to +105°C (Note 9)	0.8		1.3	mA
V_{REF} Reference Voltage	V_{REF}	EN = 1, No Load, Normal Mode		2.5		V
VDDEXT Switch Resistance	R_{VDDEXT}	Switch "On" resistance, V_{BAT} = 39.6V	8	12	17	Ω
		-40°C to +105°C (Note 9)	5		22	Ω
VCC Supply Current	I_{VCC}	Device enabled (EN = 1). Stand-Alone or Daisy Configuration. No ADC or Daisy Chain communications active.	2.0	3.25	4.5	mA
		-40°C to +105°C (Note 9)	2.0		5.0	mA
	$I_{VCCACTIVE1}$	Device enabled (EN = 1). Stand-Alone or Daisy Configuration. Average current during 16ms Scan Continuous operation. V_{BAT} = 39.6V		6.0		mA
	$I_{VCCSLEEP}$	Device enabled (EN = 1). Sleep mode. V_{BAT} = 39.6V		2.4		µA
	$I_{VCCSHDN}$	Device disabled (EN = 0). Shutdown mode.	0	1.2	4.1	µA
		-40°C to +105°C (Note 9)			9.0	µA
MEASUREMENT SPECIFICATIONS						
Cell Voltage Input Measurement Range	V_{CELL}	VC(n) - VC(n-1). For Design Reference.	0		5	V
Cell Monitor Voltage Resolution	$V_{CELLRES}$	[VC(n)-VC(n-1)] LSB step size (13-bit signed number), 5V full scale value		0.61		mV
ISL78600 Initial Cell Monitor Voltage Error (Note 10) V_{NOM} = nominal calibration voltage. Note: Cell measurement accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12).	ΔV_{CELL}	$V_{CELL} = V_{NOM}$ - 0.3V < V_{CELL} < V_{NOM} + 0.3V	-2.5		2.5	mV
		$V_{CELL} = V_{NOM}$ - 0.7V < V_{CELL} < V_{NOM} + 0.7V	-3.5		3.5	mV
		V_{CELL} = 4.95	-10		10	mV
		V_{CELL} = 0.5	-15		15	mV
		$V_{CELL} = V_{NOM}$ - 0.7V < V_{CELL} < V_{NOM} + 0.7V -40°C to +85°C (Note 9)	-9.5		9.0	mV
		-40°C to +105°C (Note 9)	-26.5		26.5	mV
		V_{CELL} = 4.95, -40°C to +85°C (Note 9)	-11		11	mV
		-40°C to +105°C (Note 9)	-26.5		26.5	mV
		V_{CELL} = 0.5, -40°C to +85°C (Note 9)	-18		18	mV
		-40°C to +105°C (Note 9)	-37		37	mV

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Cell Input Current. Note: Cell accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12)	I_{VCELL}	VC0 Input				
		VC0 ≥ 0.5 and VC0 ≤ 4.0V	-1.5	-1	-0.5	µA
		VC0 > 4.0V	-1.75		-0.5	µA
		-40°C to +105°C (Note 9)	-2.0	-1	-0.5	µA
		VC1, VC2, VC3 Inputs				
		VCn - VC(n-1) ≥ 0.5 and VCn-VC(n-1) ≤ 4.0V	-2.7	-2	-1.3	µA
		VCn - VC(n-1) > 4.0V	-2.85		-1.0	µA
		-40°C to +105°C (Note 9)	-3.0	-2	-0.84	µA
		VC4 Input				
		VCn - VC(n-1) ≥ 0.5 and VCn-VC(n-1) ≤ 4.0V	-0.6	0	0.71	µA
		VCn - VC(n-1) > 4.0V	-0.8		1.15	µA
		-40°C to +105°C (Note 9)	- 0.84	0	1.31	µA
		VC5, VC6, VC7, VC8, VC9, VC10, VC11 Inputs				
		VCn - VC(n-1) < 2.6V	0.5	2	2.7	µA
		VCn - VC(n-1) ≥ 2.6V and VCn-VC(n-1) ≤ 4.0V	1.32	2	2.89	µA
		VCn - VC(n-1) > 4.0V	1.16	2	3.33	µA
		-40°C to +105°C (Note 9)	0.5	2	3.43	µA
		VC12 Input				
		VC12 - VC11 ≥ 0.5 and VC12-VC11 ≤ 4.0V	0.37	1	1.85	µA
		VC12 - VC11 > 4.0V	0.19		2.3	µA
		-40°C to +105°C (Note 9)	0.15	1	2.47	µA
V_{BAT} Monitor Voltage Resolution	$VBAT_{RES}$	ADC resolution referred to input (V_{BAT}) level. 14-bit unsigned number. Full scale value = 79.67V.		4.863		mV
Initial V_{BAT} monitor Voltage Error (Note 10)	ΔV_{BAT}	Measured at V_{BAT} = 36V to 43.2V	-100		100	mV
		Measured at V_{BAT} = 31.2V to 48V	-125		125	mV
		Measured at V_{BAT} = 31.2V to 59.4V	-250		250	mV
		Measured at V_{BAT} = 6V to 59.4V	-320		332	mV
		Measured at V_{BAT} = 6V to 59.4V -40°C to +105°C (Note 9)	-490		490	mV
External Temperature Monitoring Regulator	V_{TEMP}	Voltage on TEMPREG output. (0 to 2mA load)	2.475	2.5	2.525	V
External Temperature Output Impedance	R_{TEMP}	Output Impedance at TEMPREG pin. (Note 9)	0	0.1	0.2	Ω
External Temperature Input Range	V_{EXT}	Effective ExTn input voltage range. For design reference. This is the input voltage range that does not trigger an open input condition.	0		2344	mV
External Temperature Input Pull-up	$R_{EXTTEMP}$	Pull-up resistor to $V_{TEMPREG}$ applied to each input during measurement		10		MΩ
External Temperature Input Offset	V_{EXTOFF}	V_{BAT} = 39.6V	-7.0		7.0	mV
		V_{BAT} = 39.6V, -40°C to +105°C (Note 9)	-10		10	mV
External Temperature Input INL	V_{EXTINL}	(Note 9)	-0.65		0.65	mV
External Temperature Input Gain Error	V_{EXTG}	Error at 2.5V input	-7.5		11	mV
		-40°C to +105°C (Note 9)	-13.4		19.3	mV
Internal Temperature Monitor Error	V_{INTMON}			±10		°C

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Internal Temperature Monitor Resolution	T_{INTRES}	Output resolution (LSB/°C). 14-bit number.		31.9		LSB/°C
Internal Temperature Monitor Output	T_{INT25}	Output count at +25°C		9180		Decimal
OVER-TEMPERATURE PROTECTION SPECIFICATIONS						
Internal Temperature Limit Threshold	T_{INTSD}	Balance stops and auto scan stops. Temperature rising or Falling.		150		°C
External Temperature Limit Threshold	T_{XT}	Corresponding to 0V (min) and $V_{TEMPREG}$ (max) External temperature input voltages higher than 15/16 $V_{TEMPREG}$ are registered as open input faults.	0		16383	Decimal
FAULT DETECTION SYSTEM SPECIFICATIONS						
Undervoltage Threshold	V_{UV}	Programmable. Corresponding to 0V (min) and 5V (max)	0		8191	Decimal
Overvoltage Threshold	V_{OV}	Programmable. Corresponding to 0V (min) and 5V (max)	0		8191	Decimal
V3P3 Power-good Window	V_{3PH}	3.3V power-good window high threshold. V_{BAT} = 39.6V	3.79	3.89	3.99	V
		-40°C to +105°C (Note 9)	3.7		4.05	V
	V_{3PL}	3.3V power-good window low threshold. V_{BAT} = 39.6V	2.57	2.64	2.71	V
		-40°C to +105°C (Note 9)	2.5		2.8	V
V2P5 Power-good Window	V_{2PH}	2.5V power-good window high threshold. V_{BAT} = 39.6V	2.62	2.7	2.766	V
		-40°C to +105°C (Note 9)	2.616		2.77	V
	V_{2PL} (Note 9)	2.5V power-good window low threshold. V_{BAT} = 39.6V	1.96	2.02	2.08	V
		-40°C to +105°C	1.90		2.14	V
VCC Power-good Window	V_{VCCH}	VCC power-good window high threshold. V_{BAT} = 39.6V	3.6	3.74	3.9	V
		-40°C to +105°C (Note 9)	3.6		4.0	V
	V_{VCCL}	VCC power-good window low threshold. V_{BAT} = 39.6V	2.6	2.7	2.8	V
		-40°C to +105°C (Note 9)	2.55		2.85	V
V_{REF} Power-good Window	V_{RPH}	V_{REF} power-good window high threshold. V_{BAT} = 39.6V	2.525	2.7	2.9	V
		-40°C to +105°C (Note 9)	2.525		2.9	V
	V_{RPL}	V_{REF} power-good window low threshold. V_{BAT} = 39.6V	2.15	2.30	2.465	V
		-40°C to +105°C (Note 9)	2.0		2.5	V
V_{REF} Reference Accuracy Test	V_{RACC}	V_{REF} value calculated using stored coefficients. V_{BAT} = 39.6V		2.500		V
Voltage Reference Check Timeout	t_{VREF}	Time to check voltage reference value from power-on, enable or wakeup		20		ms
Oscillator Check Timeout	t_{OSC}	Time to check main oscillator frequency from power-on, enable or wakeup		20		ms
Oscillator Check Filter Time	t_{OSCF}	Minimum duration of fault required for detection		100		ms
CELL OPEN WIRE DETECTION						
Open Wire Current	I_{OW}	ISCN bit = 0; V_{BAT} = 39.6V	0.125	0.15	0.185	mA
		ISCN bit = 1; V_{BAT} = 39.6V	0.85	1.0	1.15	mA
Open Wire Detection Time	t_{OW}	Open wire current source “on” time		4.6		ms
Open VC0 Detection Threshold	V_{VC0}	CELL1 negative terminal (with respect to VSS) V_{BAT} = 39.6V (Note 9)	1.2	1.5	1.8	V
Open VC1 Detection Threshold	V_{VC1}	CELL1 positive terminal (with respect to VSS) V_{BAT} = 39.6V (Note 9)	0.6	0.7	0.8	V

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Primary Detection Threshold, VC2 to VC12	V_{VC2_12P}	V(VC(n - 1))-V(VCn), n = 2 to 12 V_{BAT} = 39.6V (Note 9)	-2	-1.5	0	V
Secondary Detection Threshold, VC2 to VC12	V_{VC2_12S}	Via ADC. VC2 to VC12 only V_{BAT} = 39.6V (Note 9)	-100	-30	50	mV
Open V_{BAT} Fault Detection Threshold	V_{VBO}	VC12 - V_{BAT}		200		mV
Open VSS Fault Detection Threshold	V_{VSSO}	VSS - VC0		250		mV
MEASUREMENT FUNCTION TIMING (Note 8)						
Cell Sample Time Start		Time to sample the first cell (CELL12) following $\overline{CS}$ going High. Scan voltages command		65	71.5	µs
Cell Sample Time Duration		Time to scan all 12 cells (sample of CELL12 to sample of CELL1) scan voltages command.		233	257	µs
Scan Voltages Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		770	847	µs
Scan Temperatures Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		2690	2959	µs
Scan Mixed Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		830	913	µs
Scan Wires Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		59.4	65.3	ms
Scan All Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		63.2	69.5	ms
Measure Cell Voltage Processing Time		Time from start of measurement to register(s) loaded to $\overline{DATA\ READY}$ going low		180	198	µs
Measure V_{BAT} Voltage Processing Time		Time from start of measurement to register(s) loaded to $\overline{DATA\ READY}$ going low		130	143	µs
Measure Internal Temperature Processing Time		Time from start of measurement to register(s) loaded to $\overline{DATA\ READY}$ going low		110	121	µs
Measure External Temperature Input Processing Time		Time from start of measurement to register(s) loaded to $\overline{DATA\ READY}$ going low		2520	2772	µs
Measure Secondary Voltage Reference Time		Time from start of measurement to register(s) loaded to $\overline{DATA\ READY}$ going low		2520	2772	µs
CELL BALANCE OUTPUT SPECIFICATIONS						
Cell Balance Pin Output Impedance	R_{CBL}	CBn output off impedance between CB(n) to VC(n-1): cells 1 to 9, and between CB(n) to VC(n): cells 10 to 12	3	4	5	MΩ
Cell Balance Output Current	I_{CBH1}	CBn output on. (CB1-CB9); V_{BAT} = 39.6V; device sinking current	-28	-25	-21	µA
	I_{CBH2}	CBn output on. (CB10-CB12); V_{BAT} = 39.6V; device sourcing current	21	25	28	µA
Cell Balance Output Leakage in Shutdown	I_{CBSD}	EN = GND. V_{BAT} = 39.6V	-500	10	700	nA
External Cell Balance FET Gate Voltage	VGS	CBn Output on; External 320kΩ between VCn and CBn (n = 10 to 12) and between CBn and VCn-1 (n = 1 to 9)	7.04	8.0	8.96	V
Internal Cell Balance Output Clamp	VCBCL	I_{CB} = 100µA	8.94			V
LOGIC INPUTS: SCLK, $\overline{CS}$, DIN						
Low Level Input Voltage	VIL				0.8	V

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
High Level Input Voltage	VIH		1.75			V
Input Hysteresis	VHYS	(Note 9)	100			mV
Input Current	IIN	0V < V_{IN} < V3P3	-1		+1	µA
Input Capacitance (Note 9)	CIN				10	pF
LOGIC INPUTS: EN, COMMS SELECT1, COMMS SELECT2, COMMS RATE 0, COMMS RATE 1						
Low Level Input Voltage	VIL				0.3*V3P3	V
High Level Input Voltage	VIH		0.7*V3P3			V
Input Hysteresis	VHYS	(Note 9)	0.05*V3P3			V
Input Current	IIN	0V < V_{IN} < V3P3	-1		+1	µA
Input Capacitance (Note 9)	CIN				10	pF
LOGIC OUTPUTS: DOUT, $\overline{\text{FAULT}}$, $\overline{\text{DATA READY}}$						
Low Level Output Voltage	VOL1	At 3mA sink current	0		0.4	V
	VOL2	At 6mA sink current	0		0.6	V
High Level Output Voltage	VOH1	At 3mA source current	V3P3 – 0.4		V3P3	V
	VOH2	At 6mA source current	V3P3 – 0.6		V3P3	V
SPI INTERFACE TIMING - See Figures 1 and 2.						
SCLK Clock Frequency	f_{SCLK}				2	MHz
Pulse Width of Input Spikes Suppressed	t_{IN1}		50		200	ns
Enable Lead Time	t_{LEAD}	Chip select low to ready to receive clock data	200			ns
Clock High Time	t_{HIGH}	(Note 9)	200			ns
Clock Low Time	t_{LOW}	(Note 9)	200			ns
Enable Lag Time	t_{LAG}	Last data read clock edge to Chip Select high (Note 9)	250			ns
CHIP SELECT High Time	$t_{CS:WAIT}$	Minimum high time for $\overline{\text{CS}}$ between bytes	200			ns
Slave Access Time	t_A	Chip Select low to DOUT active. (Note 9)			200	ns
Data Valid Time	t_V	Clock low to DOUT valid			350	ns
Data Output Hold Time (Note 9)	t_{HO}	Data hold time after falling edge of SCLK	0			ns
DOUT Disable Time	t_{DIS}	DOUT disabled following rising edge of $\overline{\text{CS}}$ (Note 9)			240	ns
Data Setup Time	t_{SU}	Data input valid prior to rising edge of SCLK	100			ns
Data Input Hold Time	t_{HI}	Data input to remain valid following rising edge of SCLK	80			ns
$\overline{\text{DATA READY}}$ Start Delay Time	$t_{DR:ST}$	Chip select high to $\overline{\text{DATA READY}}$ low. (Note 9)	100			ns
$\overline{\text{DATA READY}}$ Stop Delay Time	$t_{DR:SP}$	Chip select high to $\overline{\text{DATA READY}}$ high. (Note 9)			750	ns
$\overline{\text{DATA READY}}$ High Time	$t_{DR:WAIT}$	Time between bytes. (Note 9)	0.6			µs
SPI Communications Timeout	$t_{SPI:TO}$	Time the $\overline{\text{CS}}$ remains high before SPI communications time out - requiring the start of a new command		100		µs
DOUT Rise Time	t_R	Up to 50pF load			30	ns
DOUT Fall Time	t_F	Up to 50pF load			30	ns

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DAISY CHAIN COMMUNICATIONS INTERFACE: DHi1, DLo1, DHi2, DLo2						
Daisy Chain Clock Frequency		Comms Rate (0, 1) = 11	450	500	550	kHz
		Comms Rate (0, 1) = 10	225	250	275	kHz
		Comms Rate (0, 1) = 01	112.5	125	137.5	kHz
		Comms Rate (0, 1) = 00	56.25	62.5	68.75	kHz
Common Mode Reference Voltage				$V_{BAT}/2$		V

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Scan and Measurement start times are synchronised by the receiver to the falling edge of the 24^{th} clock pulse (Daisy Chain systems) or to the falling edge of the 16^{th} clock pulse (non-Daisy Chain, single device systems) of the Scan or *Measure* command. Clock pulses are at the SCLK pin for Master and Stand-alone devices, and at the DHi/DLo1 pins for middle and top Daisy Chain devices. Maximum values are based on characterization of the internal clock and are not 100% tested.
9. These MIN and/or MAX values are based on characterization data and are not 100% tested.
10. Stresses may be induced in the ISL78600 during soldering or other high temperature events that affect measurement accuracy. Initial accuracy does not include effects due to this. See Figure 4B for cell reading accuracy obtained after soldering to Intersil evaluation boards. When soldering the ISL78600 to a customized circuit board with a layout or construction significantly differing from the Intersil evaluation board, design verification tests should be applied to determine drift due to soldering and over lifetime.

Timing Diagrams

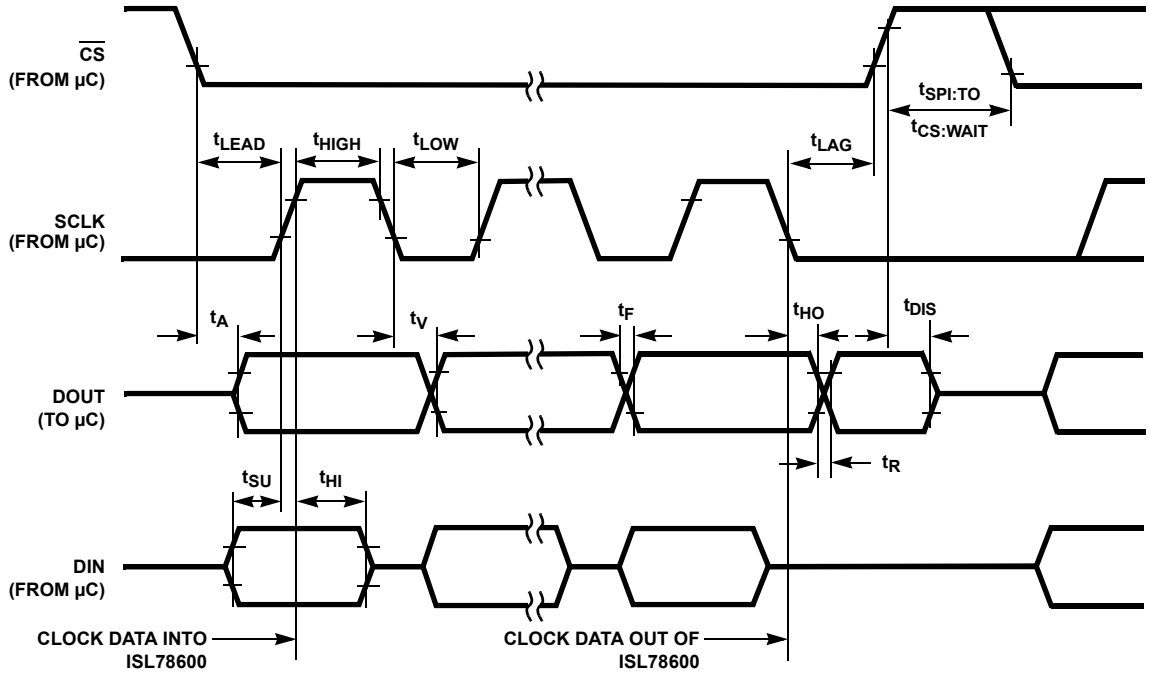


FIGURE 1. SPI FULL DUPLEX (4-WIRE) INTERFACE TIMING

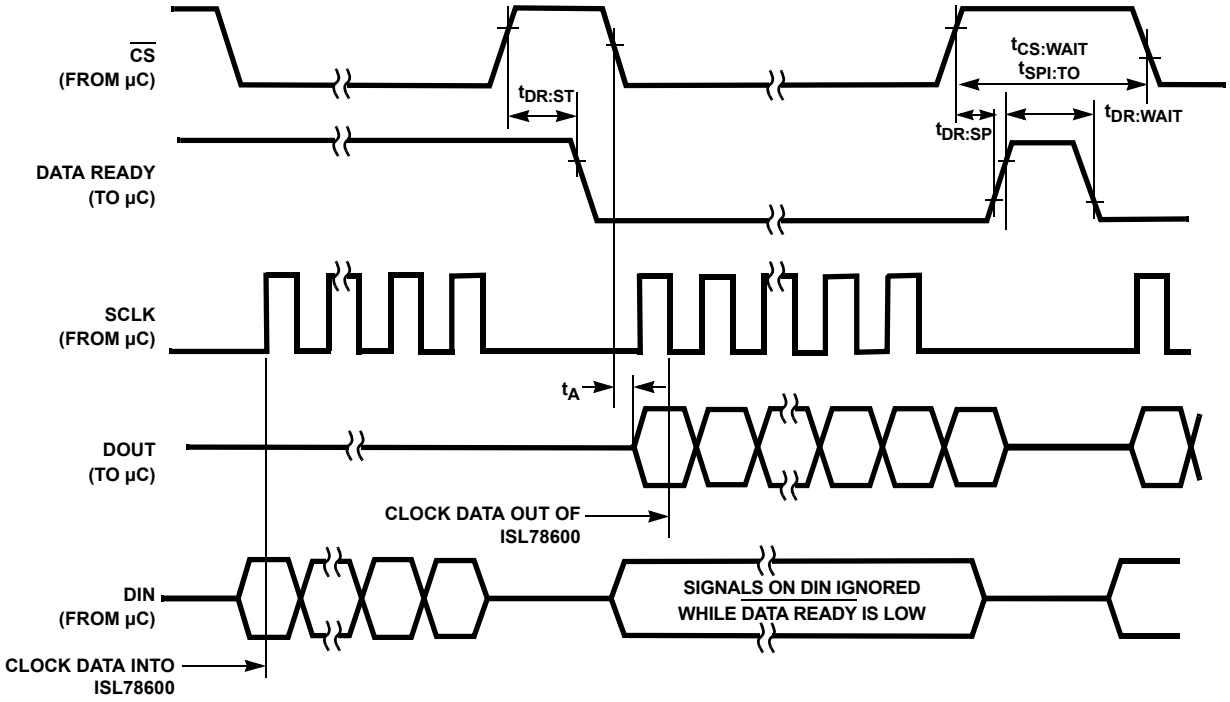


FIGURE 2. SPI HALF DUPLEX (3-WIRE) INTERFACE TIMING

Typical Performance Curves

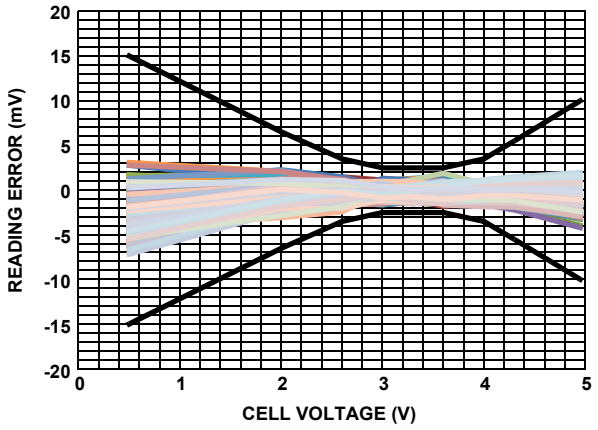


FIGURE 3A. CELL VOLTAGE READING ERROR FROM -20°C TO +60°C

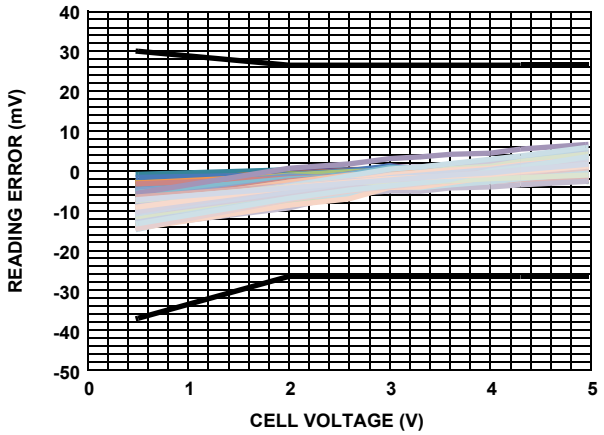


FIGURE 3B. CELL VOLTAGE READING ERROR FROM -40°C to +105°C

Typical Performance Curves (Continued)

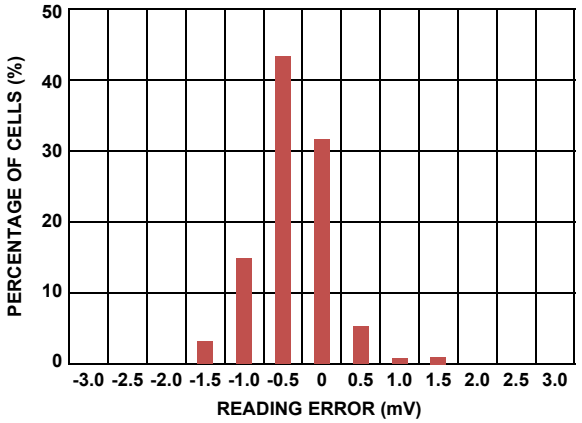


FIGURE 4A. INITIAL CELL VOLTAGE ACCURACY AT 3.3V, +25°C HISTOGRAM

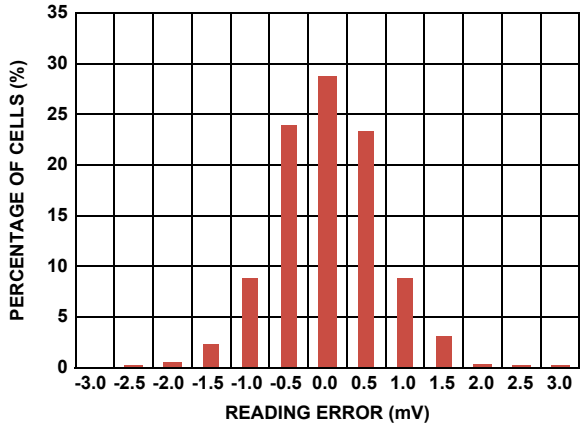


FIGURE 4B. CELL READING ERROR FROM 114 EVALUATION BOARDS AT 3.3V, +25°C HISTOGRAM

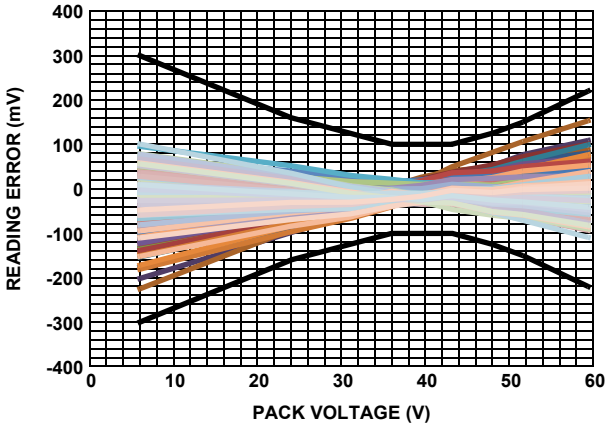


FIGURE 5A. PACK VOLTAGE READING ERROR FROM -20°C TO +60°C

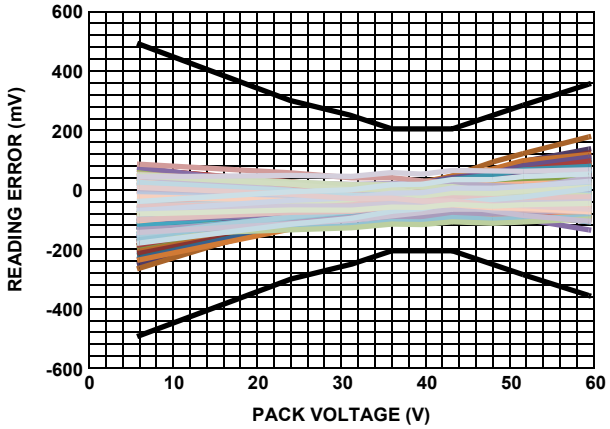


FIGURE 5B. PACK VOLTAGE READING ERROR FROM -40°C TO +105°C

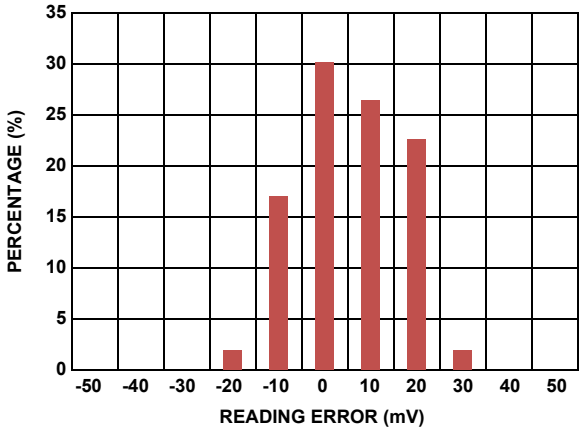


FIGURE 6. INITIAL PACK VOLTAGE ACCURACY AT 39.6V, +25°C HISTOGRAM

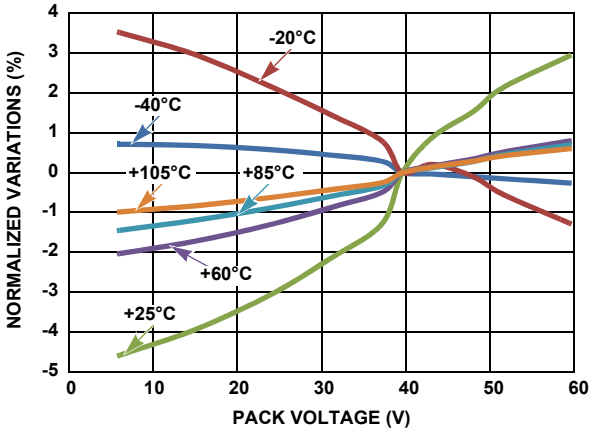


FIGURE 7. IC TEMPERATURE ERROR vs PACK VOLTAGE

Typical Performance Curves (Continued)

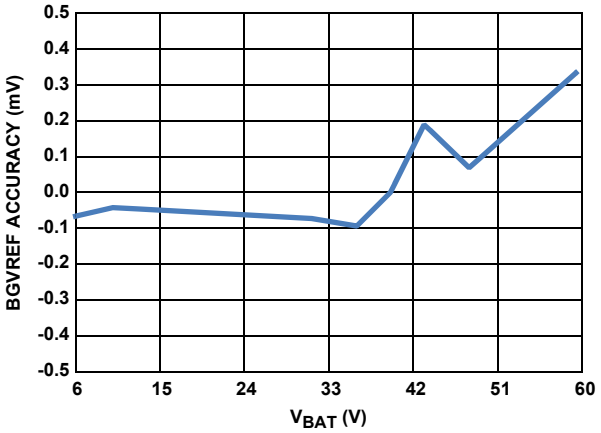


FIGURE 8. VOLTAGE REFERENCE CHECK FUNCTION vs PACK VOLTAGE (AT +25°C)

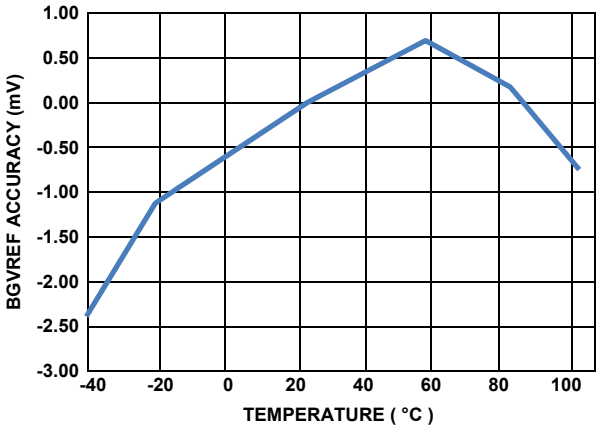


FIGURE 9. VOLTAGE REFERENCE CHECK FUNCTION vs TEMPERATURE (V_{BAT} = 39.6)

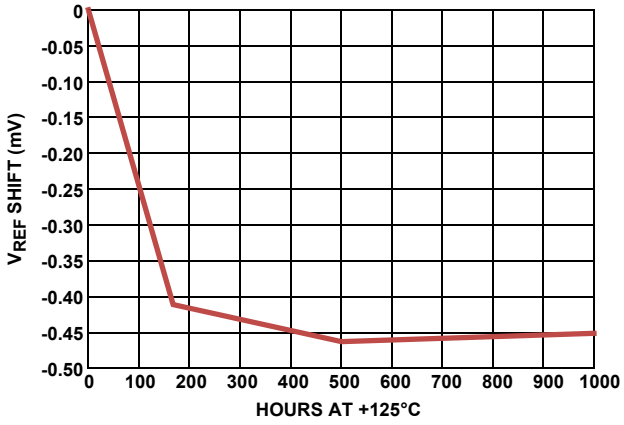


FIGURE 10. V_{REF} SHIFT OVER HTOL

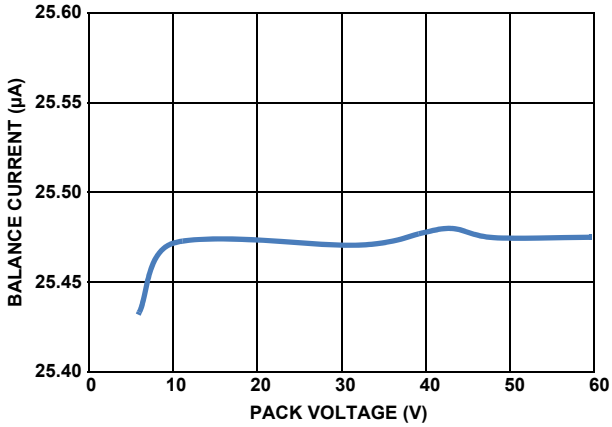


FIGURE 11. BALANCE CURRENT vs PACK VOLTAGE

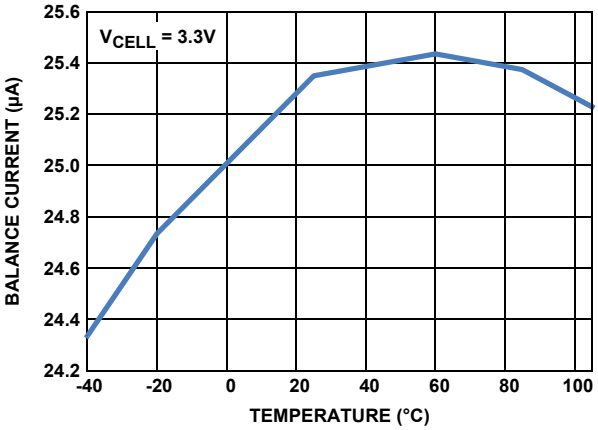


FIGURE 12. BALANCE CURRENT vs TEMPERATURE

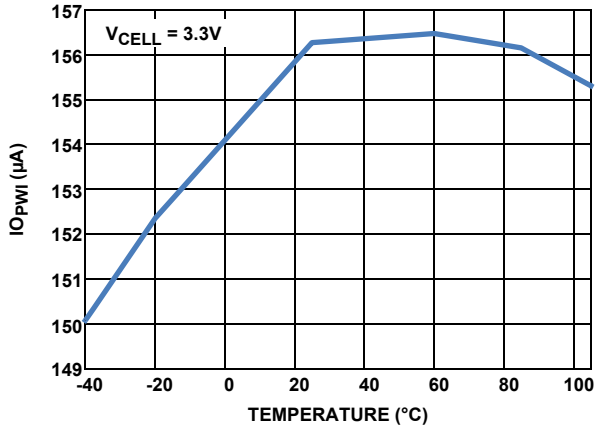


FIGURE 13. OPEN WIRE TEST CURRENT vs TEMPERATURE (150µA SETTING)

Typical Performance Curves (Continued)

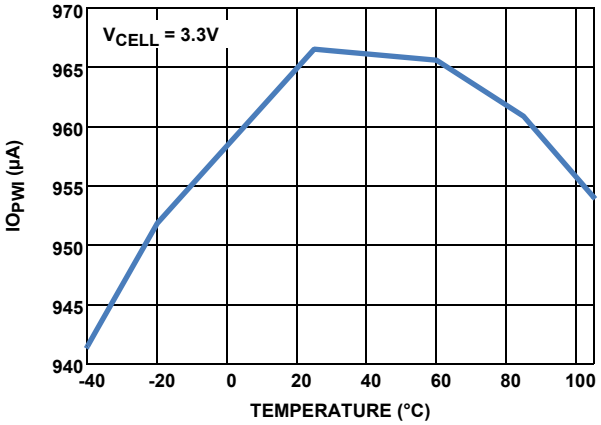


FIGURE 14. OPEN WIRE TEST CURRENT vs TEMPERATURE (1mA SETTING)

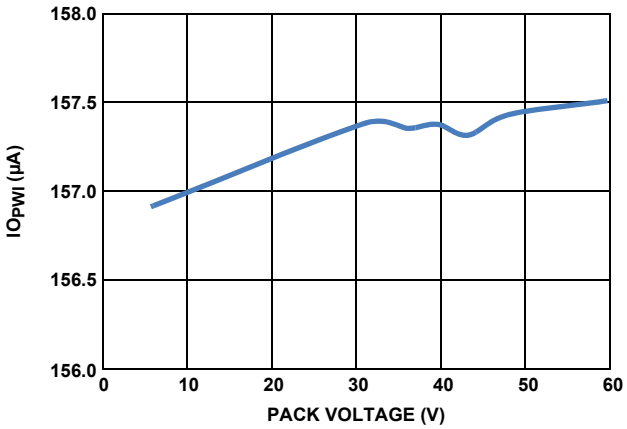


FIGURE 15. OPEN WIRE TEST CURRENT vs PACK VOLTAGE (150µA SETTING)

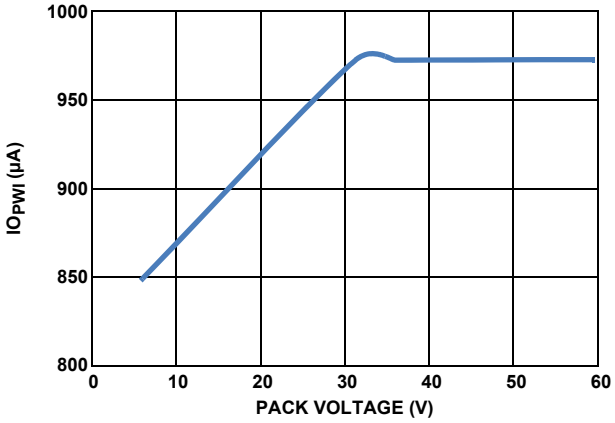


FIGURE 16. OPEN WIRE TEST CURRENT vs PACK VOLTAGE (1mA SETTING)

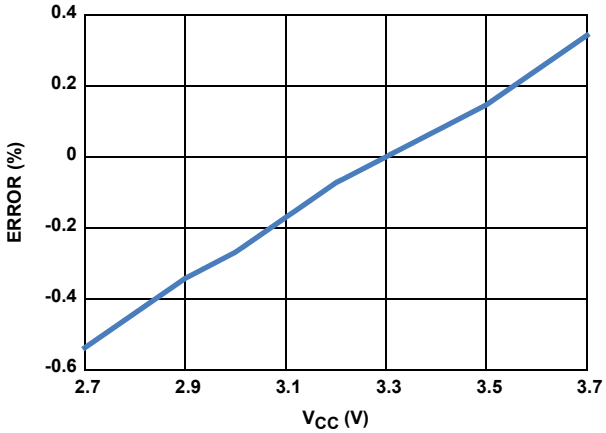


FIGURE 17. 4MHz OSCILLATOR ERROR vs V_{CC}

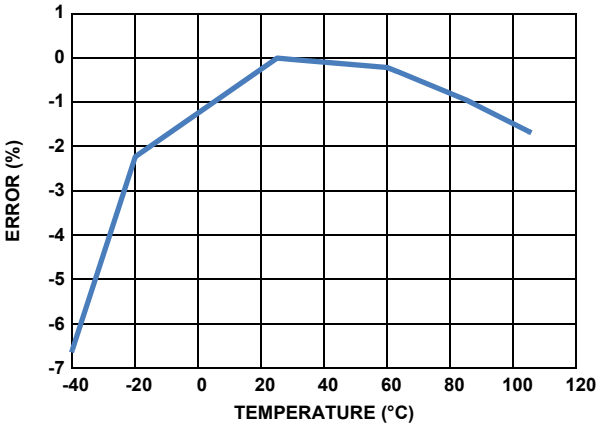


FIGURE 18. 4MHz OSCILLATOR ERROR vs TEMPERATURE

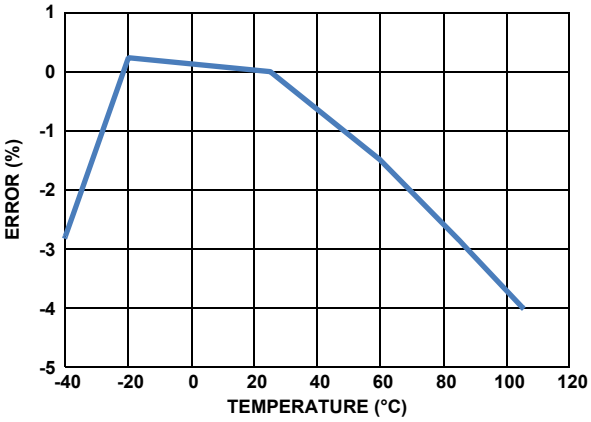


FIGURE 19. 32kHz OSCILLATOR ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

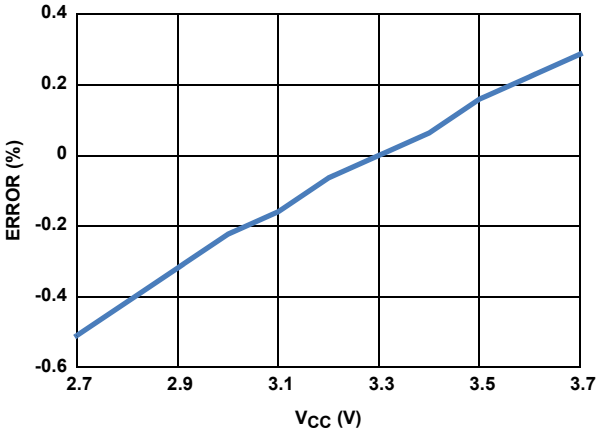


FIGURE 20. 32kHz OSCILLATOR ERROR vs V_{CC}

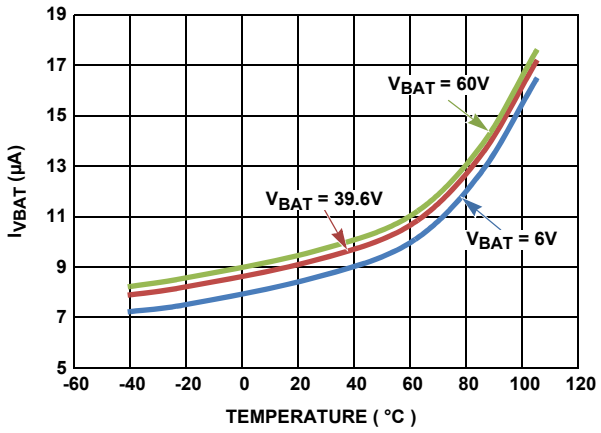


FIGURE 21A. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (STANDALONE MODE)

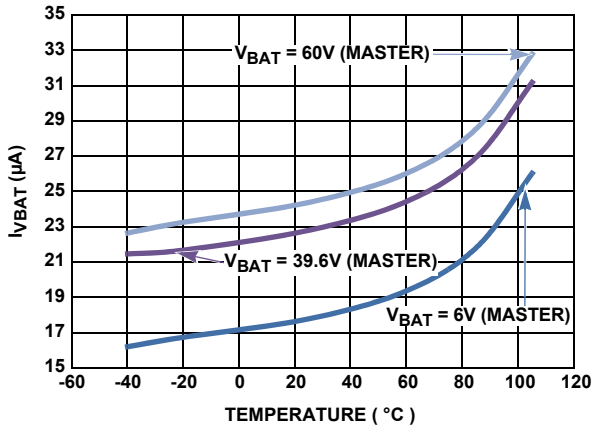


FIGURE 21B. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MODE)

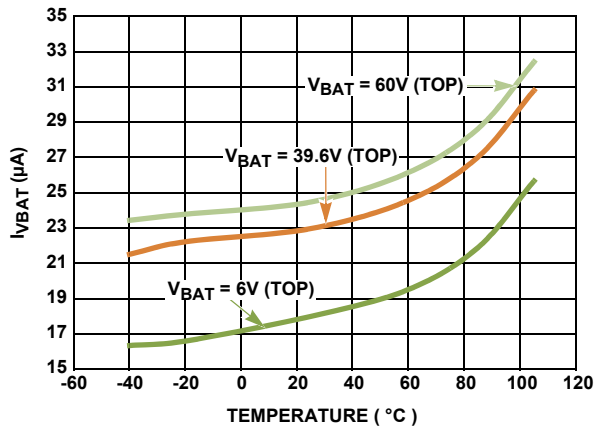


FIGURE 21C. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MODE)

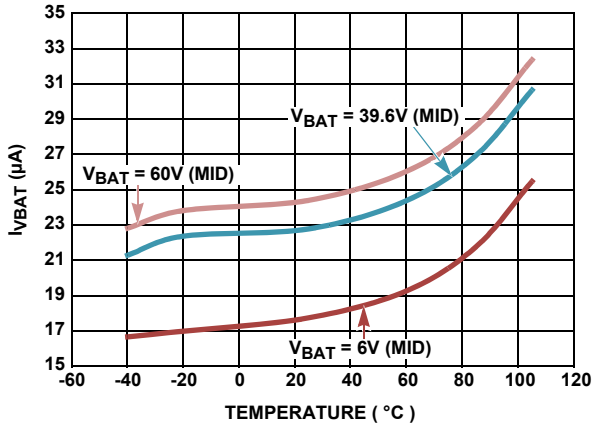


FIGURE 21D. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MODE)

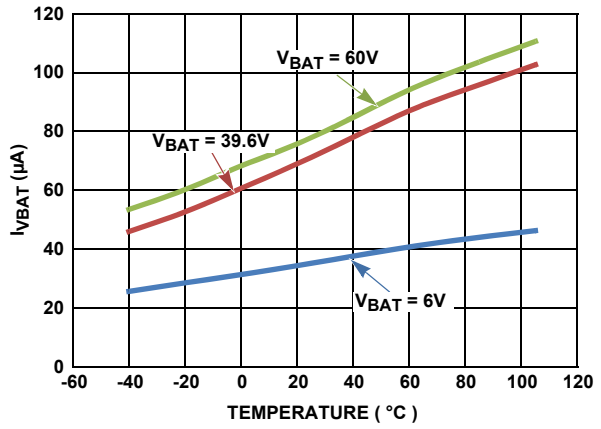


FIGURE 22A. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (STANDALONE MODE)

Typical Performance Curves (Continued)

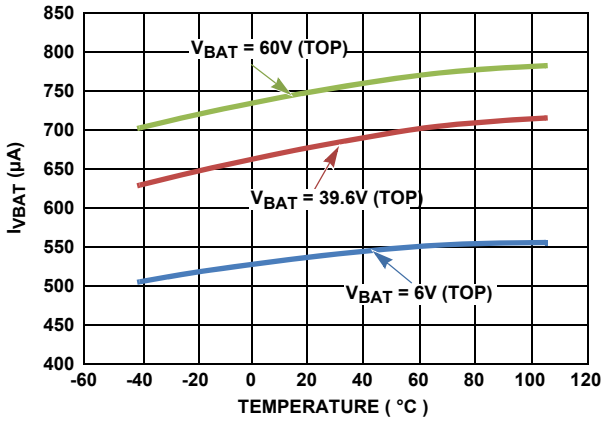


FIGURE 22B. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN TOP)

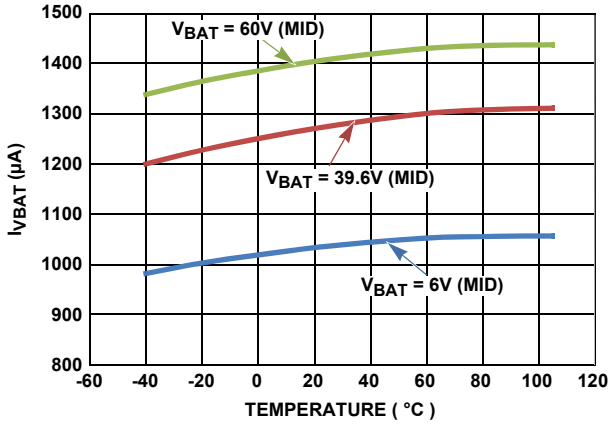


FIGURE 22C. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MIDDLE)

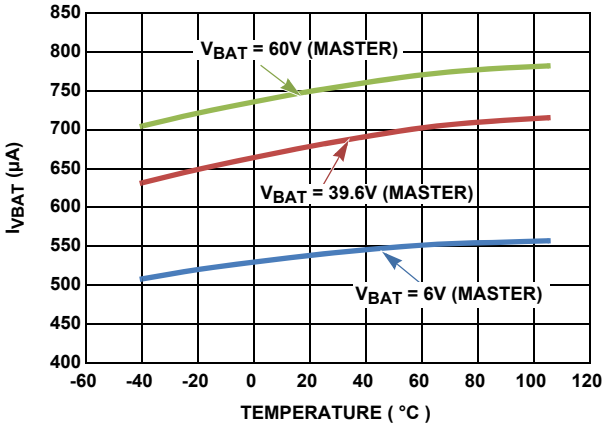


FIGURE 22D. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MASTER)

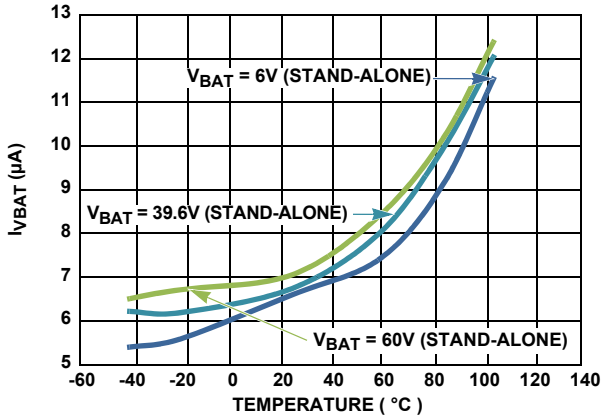


FIGURE 23A. PACK VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

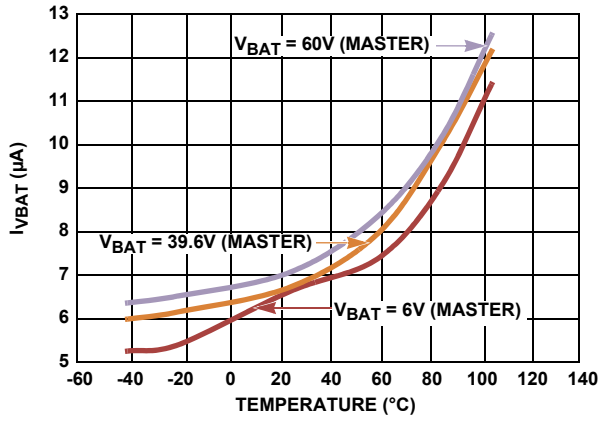


FIGURE 23B. V_{BAT} SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

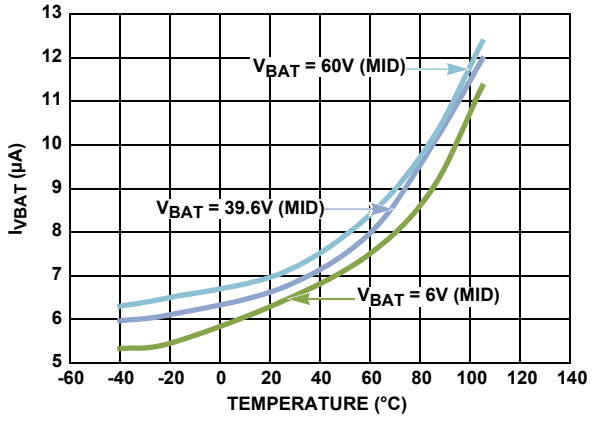


FIGURE 23C. V_{BAT} VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

Typical Performance Curves (Continued)

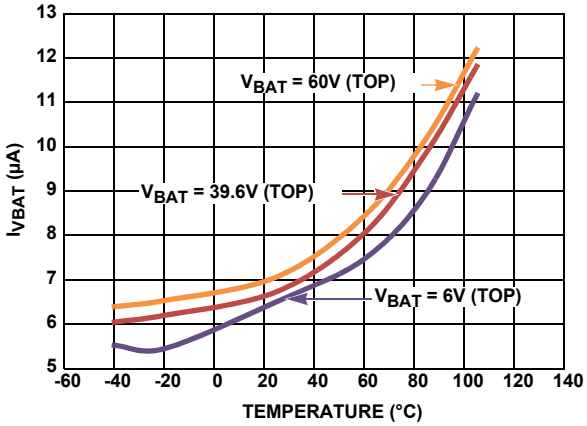


FIGURE 23D. V_{BAT} VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

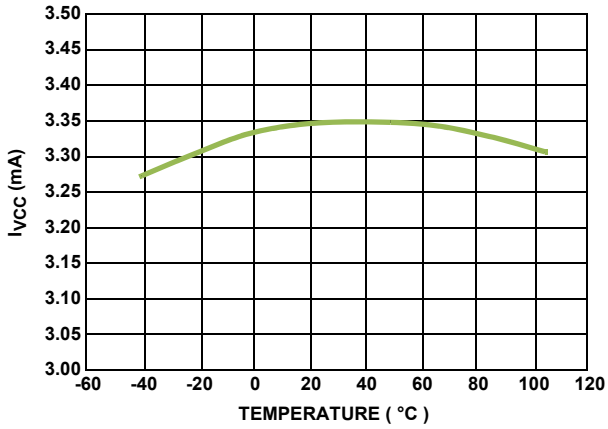


FIGURE 24. V_{CC} SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V

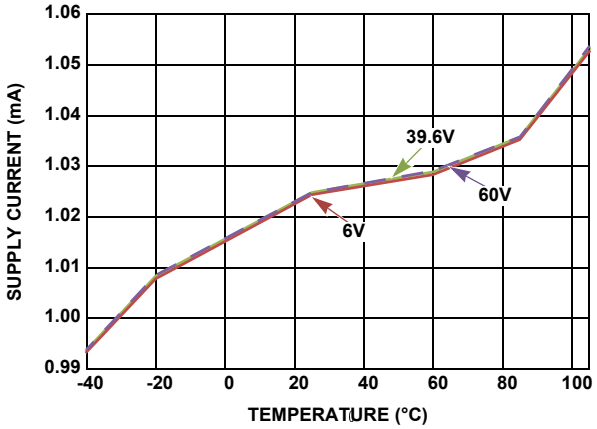


FIGURE 25. V3P3 SUPPLY CURRENT vs TEMPERATURE

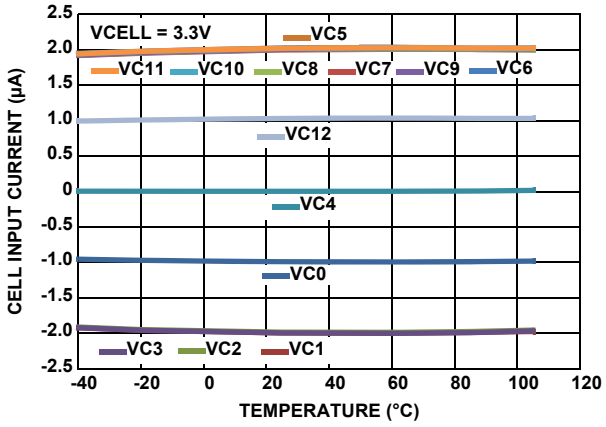


FIGURE 26. CELL INPUT CURRENT vs TEMPERATURE

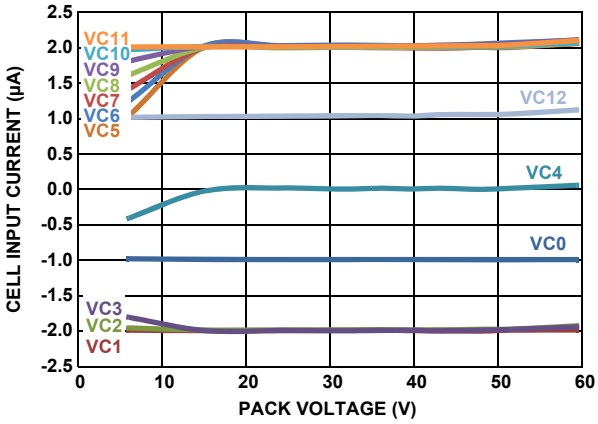


FIGURE 27. CELL INPUT CURRENT vs PACK VOLTAGE (+25°C)

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Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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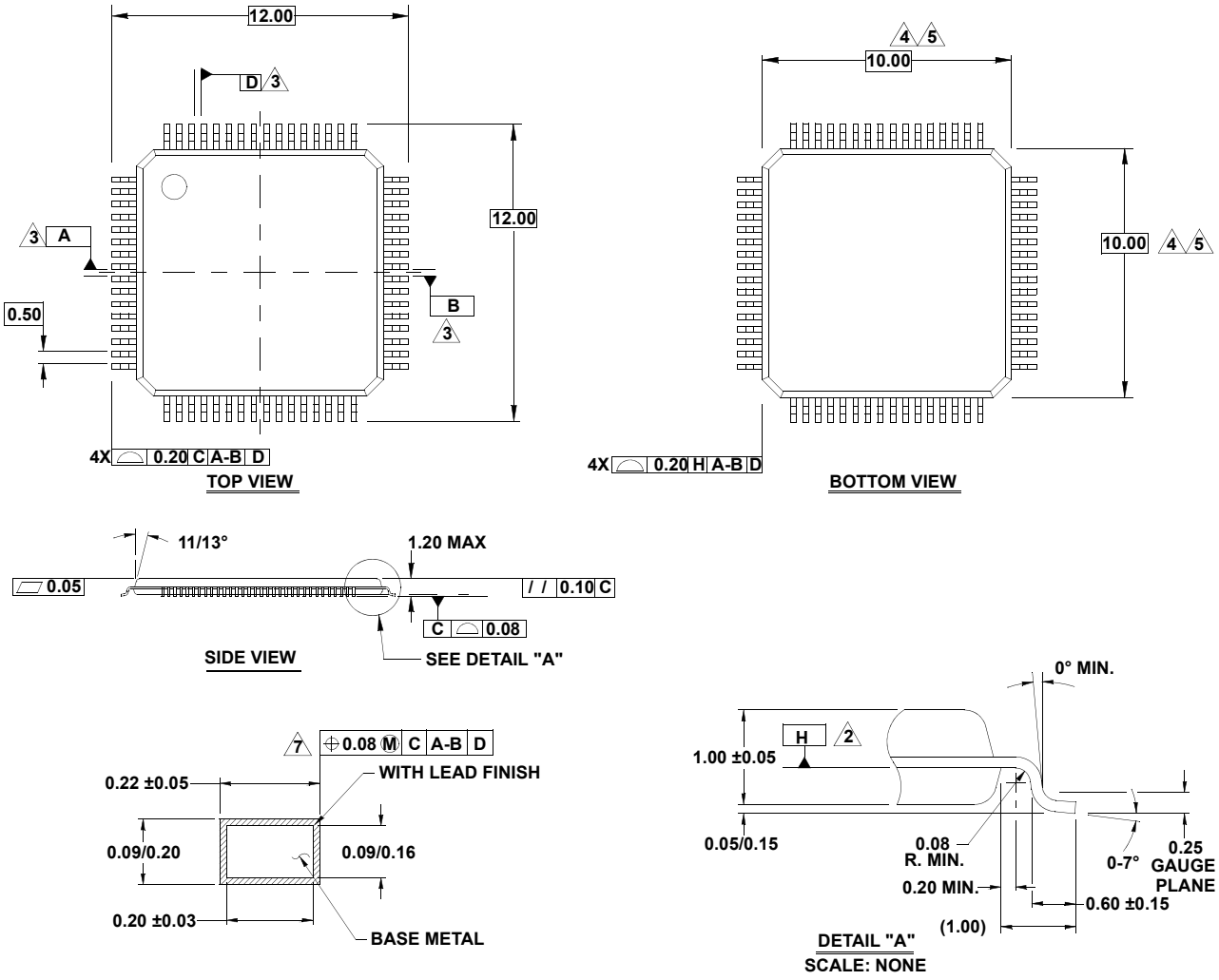
Package Outline Drawing
Q64.10x10D
64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

Rev 2, 9/12



NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.254mm.
5. These dimensions to be determined at datum plane H.
6. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
7. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total at maximum material condition. Dambar cannot be located on the lower radius or the foot.
8. Controlling dimension: millimeter.
9. This outline conforms to JEDEC publication 95 registration MS-026, variation ACD.
10. Dimensions in ( ) are for reference only.