PD - 97787

International
IOR Rectifier

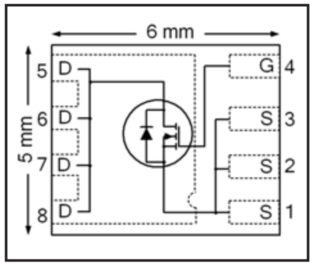
StrongIRFET™

IRFH7004PbF

HEXFET® Power MOSFET

Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters



V_{DSS}		40V
$R_{DS(on)}$	typ.	1.1mΩ
	max.	1.4mΩ
I_D (Silicon Limited)		259A①
I_D (Package Limited)		100A

PQFN 5X6 mm

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- RoHS Compliant containing no Lead, no Bromide, and no Halogen

Ordering Information

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFH7004TRPBF	PQFN 5mm x 6mm	Tape and Reel	4000	
IRFH7004TR2PBF	PQFN 5mm x 6mm	Tape and Reel	400	

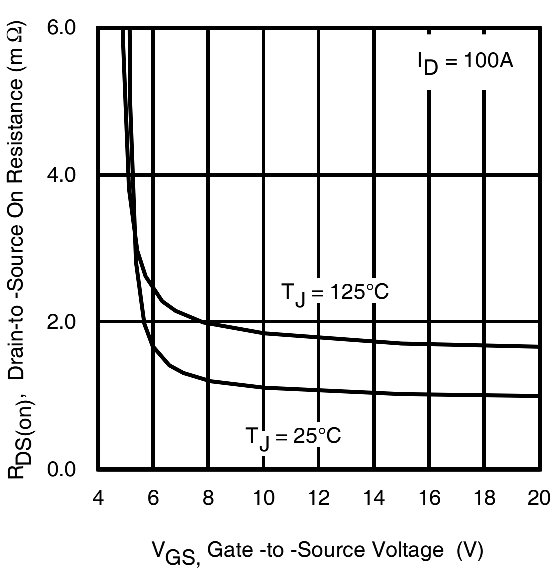


Fig 1. Typical On-Resistance vs. Gate Voltage

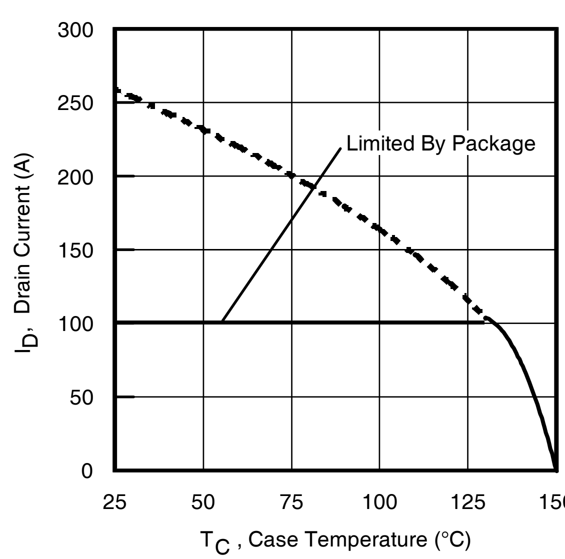


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	259①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	164①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	100	
I_{DM}	Pulsed Drain Current ②	1247	
P_D @T_C = 25°C	Maximum Power Dissipation	156	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	191	mJ
$E_{AS\ (tested)}$	Single Pulse Avalanche Energy Tested Value ⑩	314	
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ⑨	–––	0.8	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ⑨	–––	15	
$R_{\theta JA}$	Junction-to-Ambient ⑧	–––	34	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑧	–––	21	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.033	–––	V/°C	Reference to 25°C, I_D = 1.0mA ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	1.1	1.4	mΩ	V_{GS} = 10V, I_D = 100A ⑤
		–––	1.7	–––	mΩ	V_{GS} = 6.0V, I_D = 50A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	V_{DS} = V_{GS}, I_D = 150μA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	1.0	μA	V_{DS} = 40V, V_{GS} = 0V
		–––	–––	150		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
R_G	Internal Gate Resistance	–––	2.4	–––	Ω	

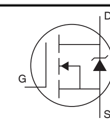
Notes:

① Calculated continuous current based on maximum allowable junction temperature. Package is limited to 100A by production test capability. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
② Repetitive rating; pulse width limited by max. junction temperature.
③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.038mH R_G = 50Ω, I_{AS} = 100A, V_{GS} =10V.
④ $I_{SD} \leq$ 100A, di/dt ≤ 1366A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C.
⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑧ When mounted on 1 inch square 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.
⑨ R_θ is measured at T_J approximately 90°C.
⑩ This value determined from sample failure population, starting T_J = 25°C, L= 0.038mH, R_G = 50Ω, I_{AS} = 100A, V_{GS} =10V.

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	117	—	—	S	V_{DS} = 10V, I_D = 100A
Q_g	Total Gate Charge	—	129	194	nC	I_D = 100A
Q_{gs}	Gate-to-Source Charge	—	34	—		V_{DS} =20V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	40	—		V_{GS} = 10V ⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	—	169	—		I_D = 100A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	V_{DD} = 20V
t_r	Rise Time	—	51	—		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	—	73	—		R_G = 2.7Ω
t_f	Fall Time	—	49	—		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	—	6419	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	952	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	656	—		ƒ = 1.0 MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	1161	—		V_{GS} = 0V, V_{DS} = 0V to 32V ⑦
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	—	1305	—		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	100①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	1247	A	
V_{SD}	Diode Forward Voltage	—	0.95	1.3	V	T_J = 25°C, I_S = 100A, V_{GS} = 0V ⑤
dv/dt	Peak Diode Recovery ④	—	2.5	—	V/ns	T_J = 175°C, I_S = 100A, V_{DS} = 40V
t_{rr}	Reverse Recovery Time	—	35	—	ns	T_J = 25°C V_R = 34V,
		—	35	—		T_J = 125°C I_F = 100A
Q_{rr}	Reverse Recovery Charge	—	26	—	nC	T_J = 25°C di/dt = 100A/μs ⑤
		—	27	—		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	1.5	—	A	T_J = 25°C

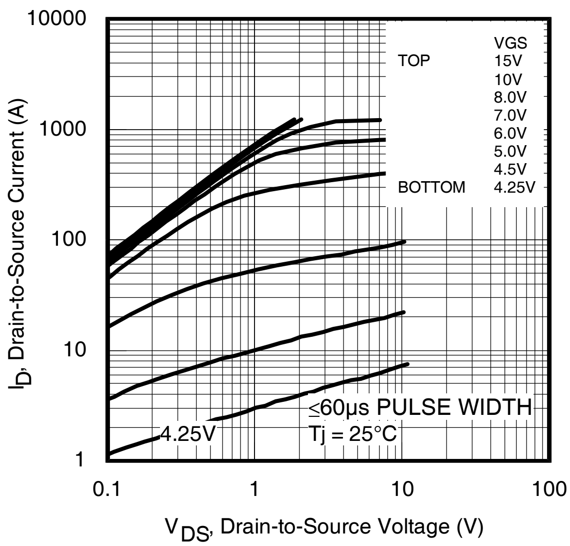


Fig 3. Typical Output Characteristics

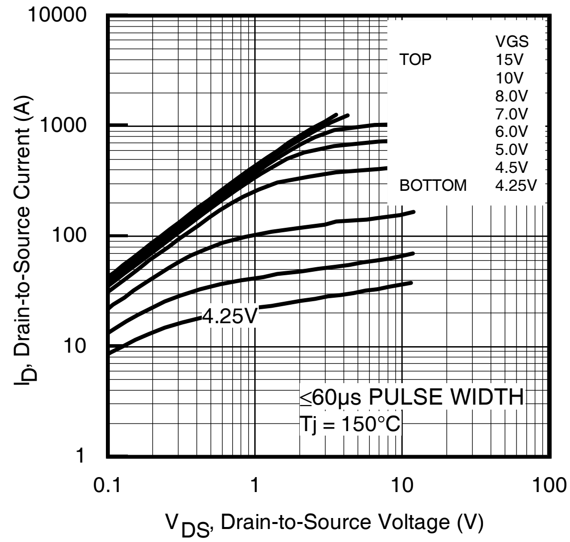


Fig 4. Typical Output Characteristics

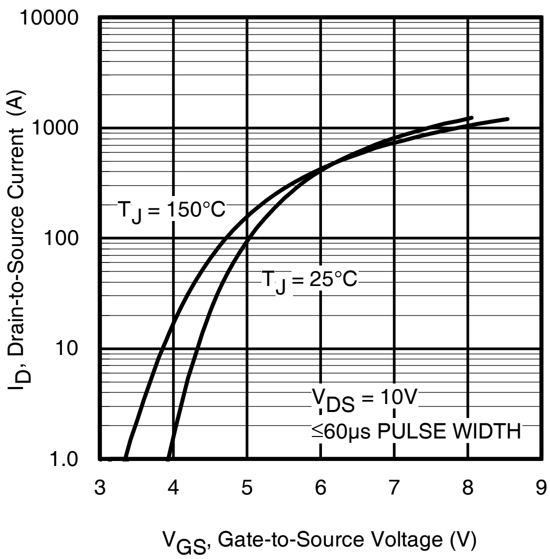


Fig 5. Typical Transfer Characteristics

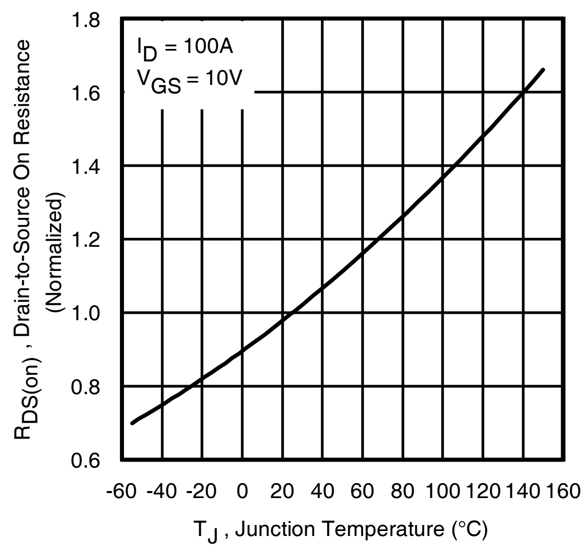


Fig 6. Normalized On-Resistance vs. Temperature

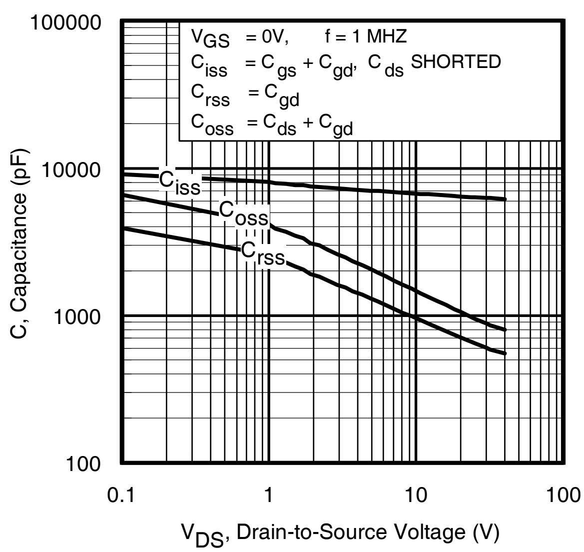


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

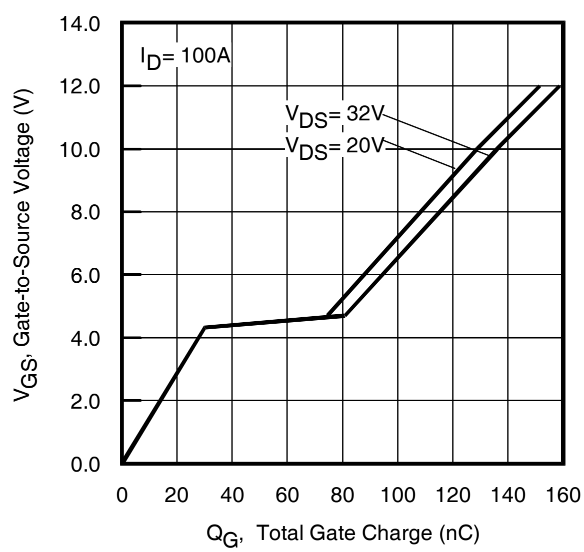


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

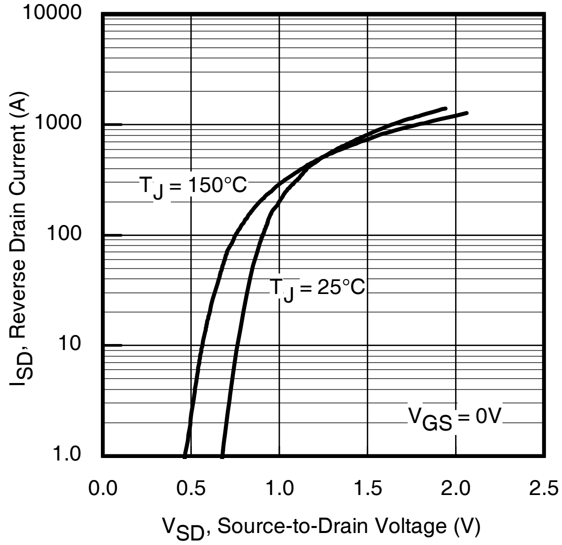


Fig 9. Typical Source-Drain Diode Forward Voltage

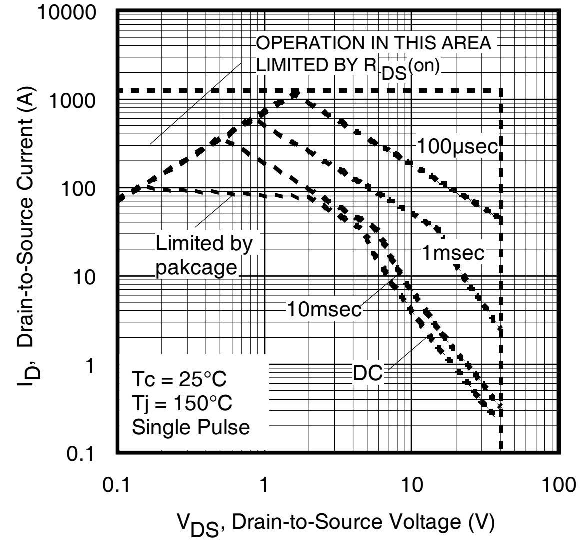


Fig 10. Maximum Safe Operating Area

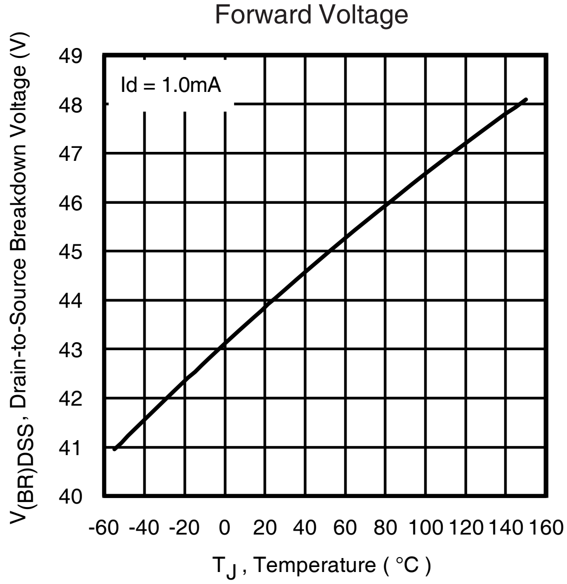


Fig 11. Drain-to-Source Breakdown Voltage

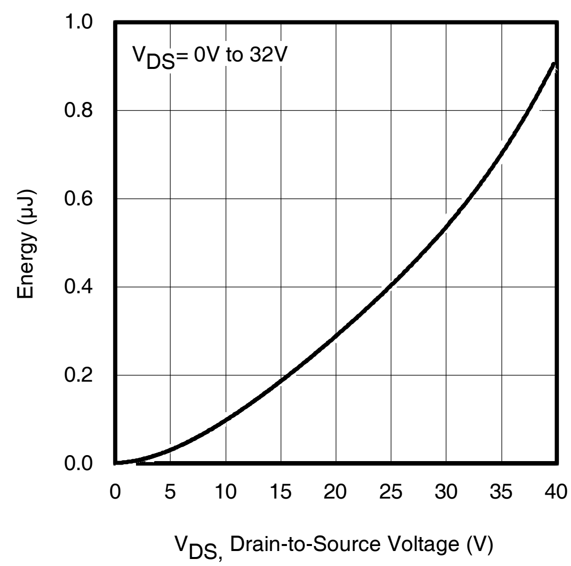


Fig 12. Typical C_{OSS} Stored Energy

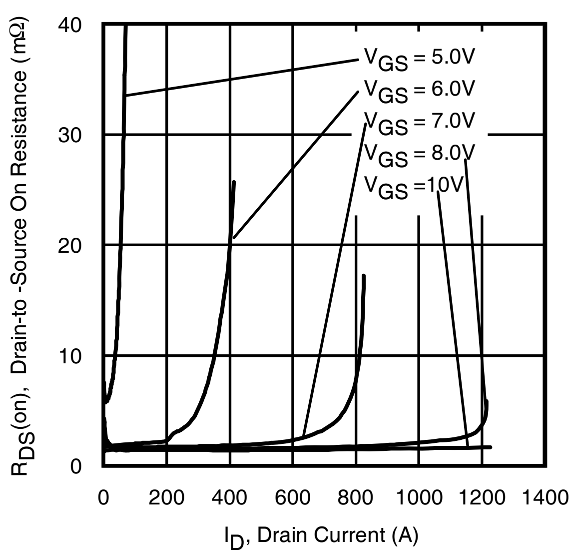


Fig 13. Typical On-Resistance vs. Drain Current

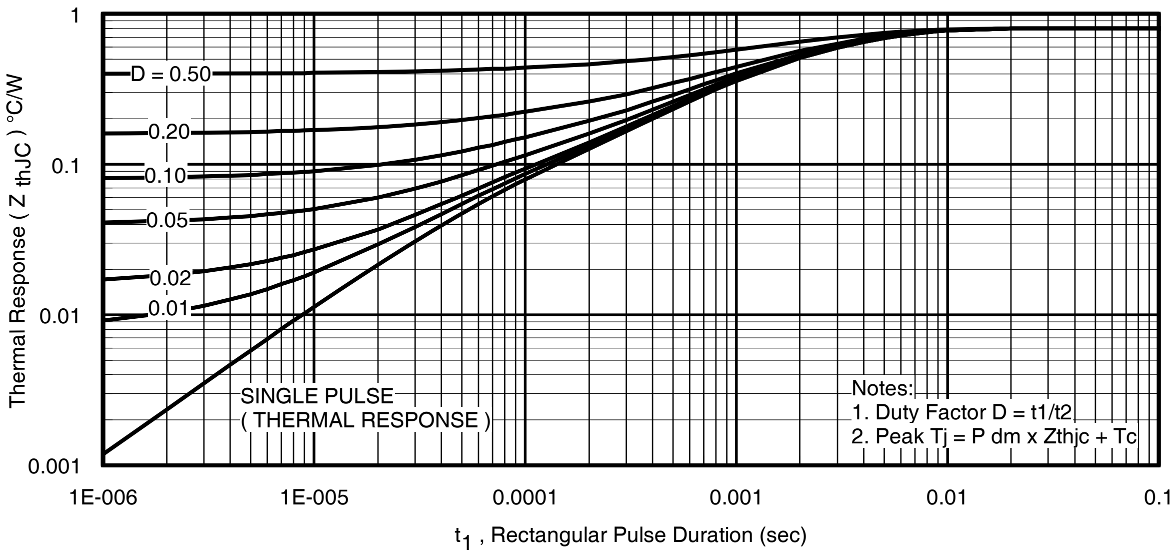


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

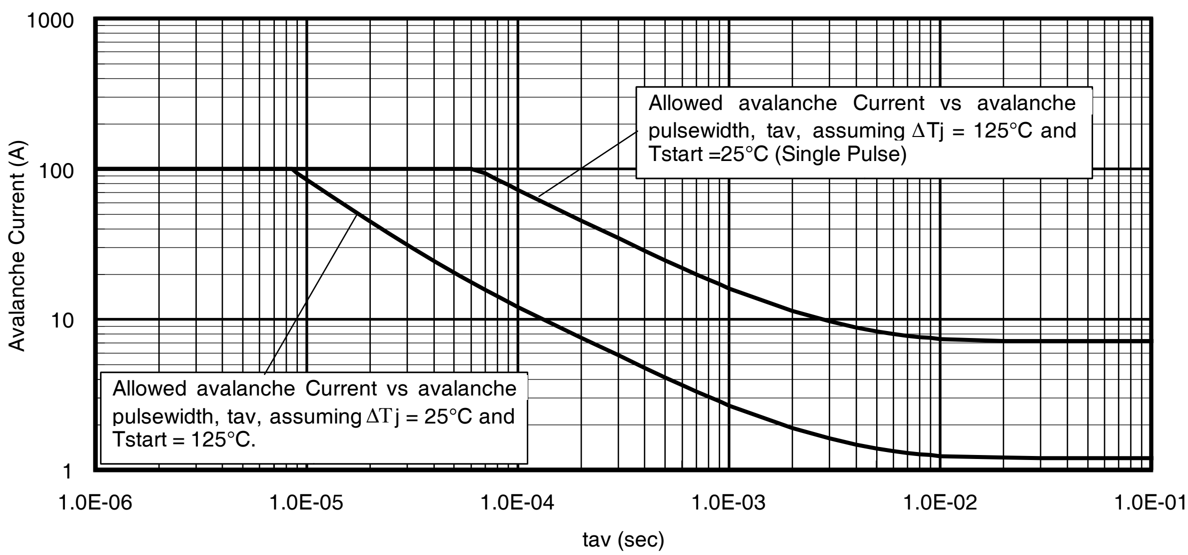


Fig 15. Typical Avalanche Current vs.Pulsewidth

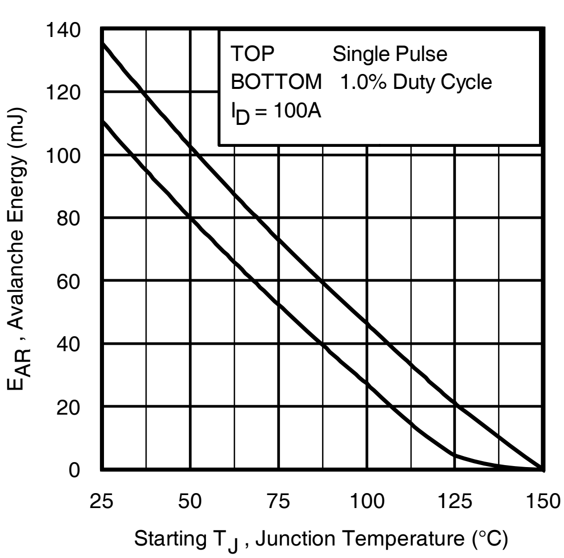


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

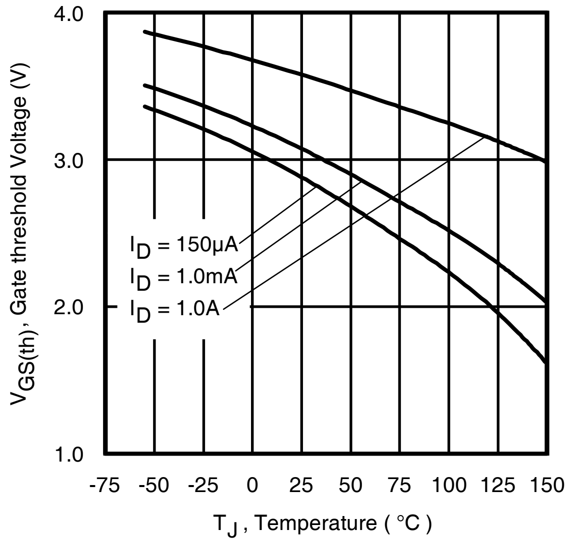


Fig 17. Threshold Voltage vs. Temperature

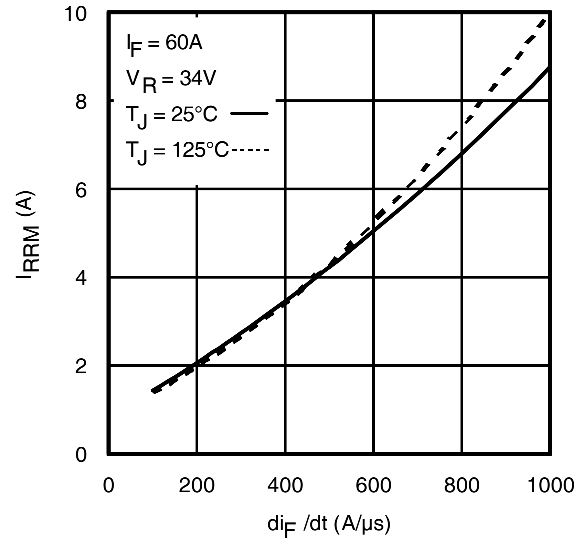


Fig. 18 - Typical Recovery Current vs. di_f/dt

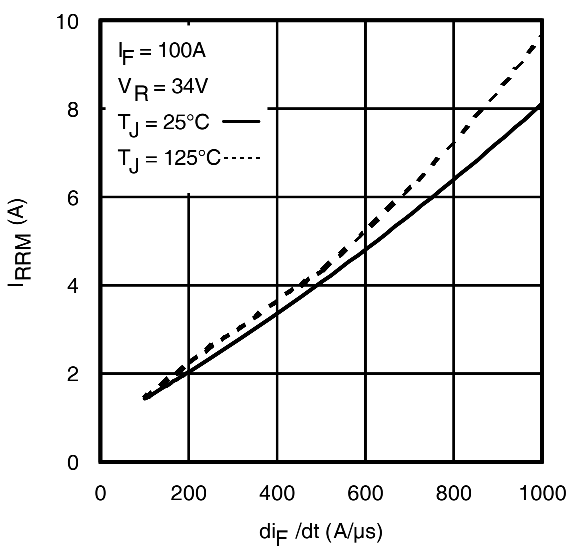


Fig. 19 - Typical Recovery Current vs. di_f/dt

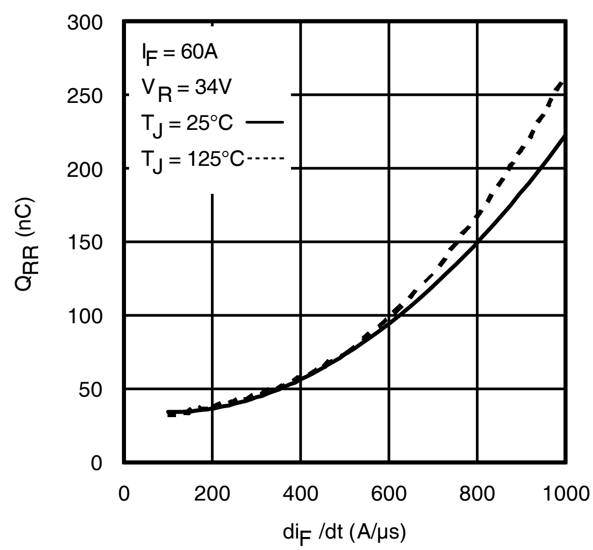


Fig. 20 - Typical Stored Charge vs. di_f/dt

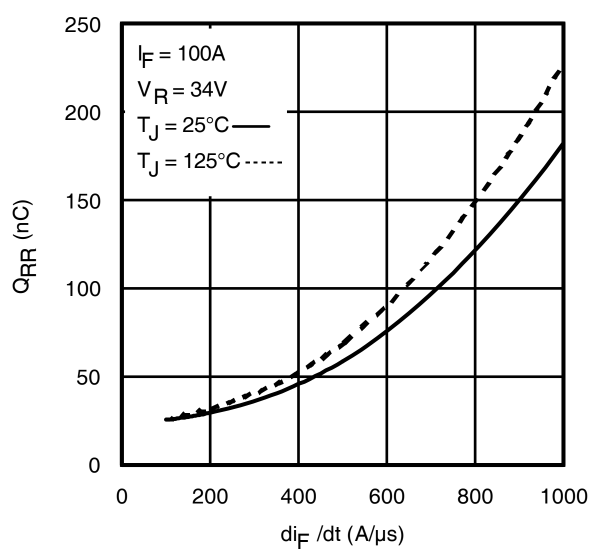
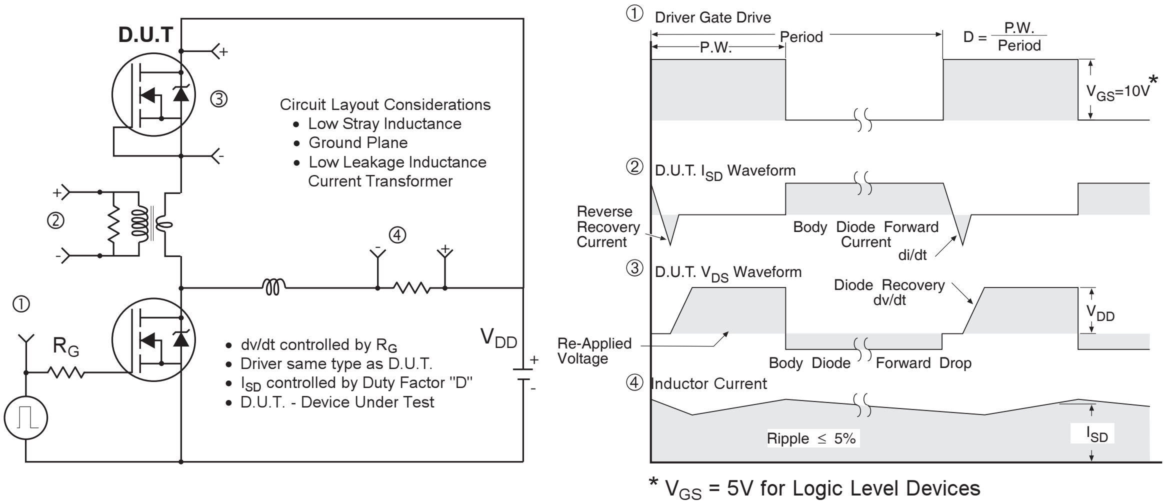


Fig. 21 - Typical Stored Charge vs. di_f/dt



* V_{GS} = 5V for Logic Level Devices

Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

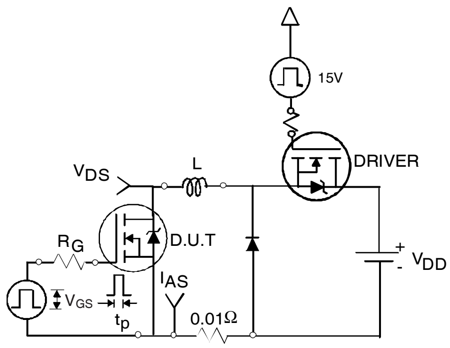


Fig 22a. Unclamped Inductive Test Circuit

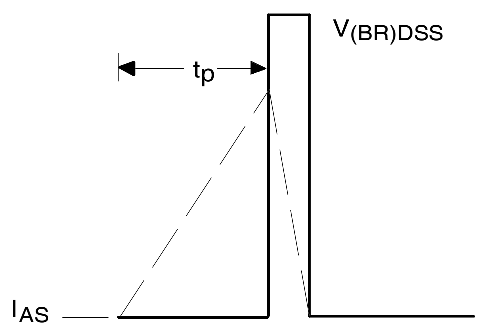


Fig 22b. Unclamped Inductive Waveforms

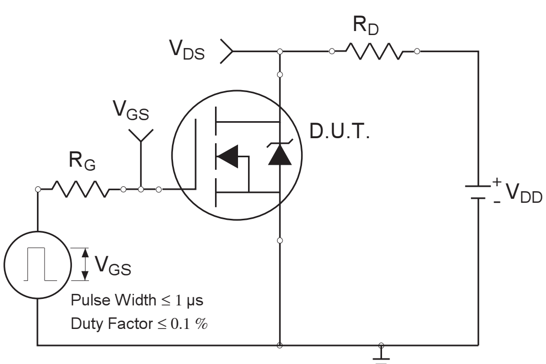


Fig 23a. Switching Time Test Circuit

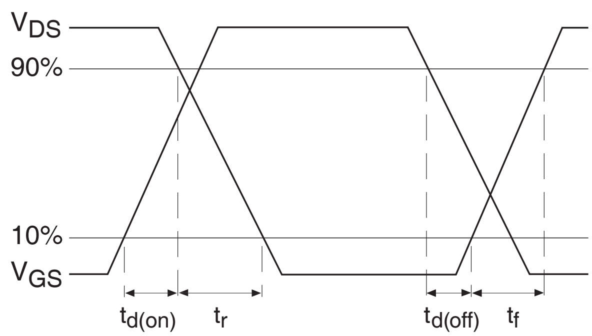


Fig 23b. Switching Time Waveforms

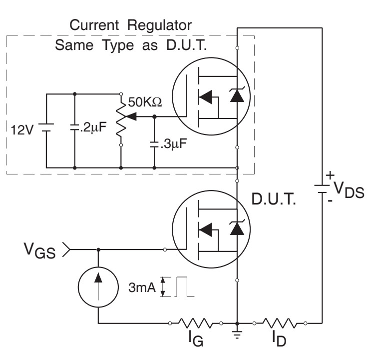


Fig 24a. Gate Charge Test Circuit

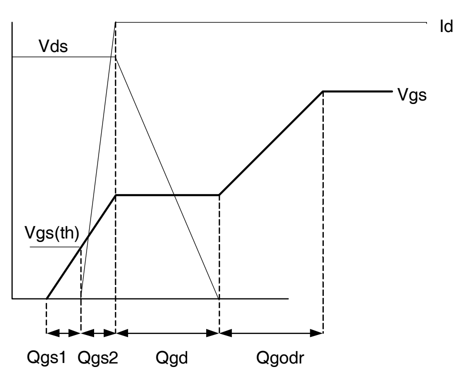
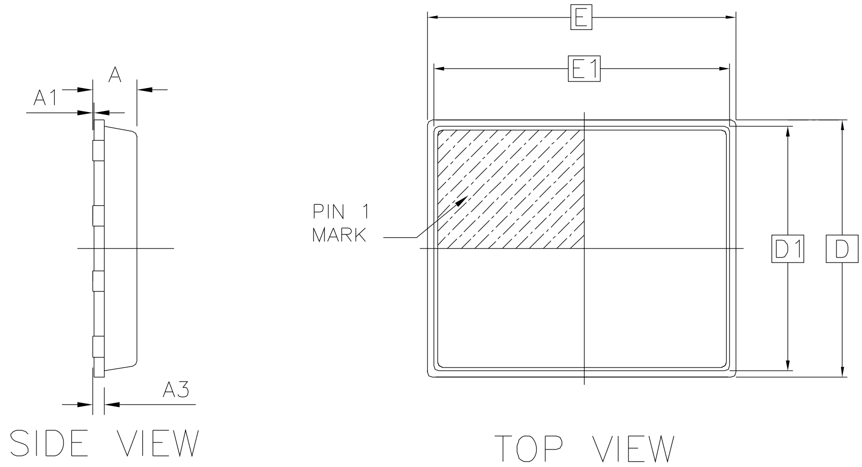
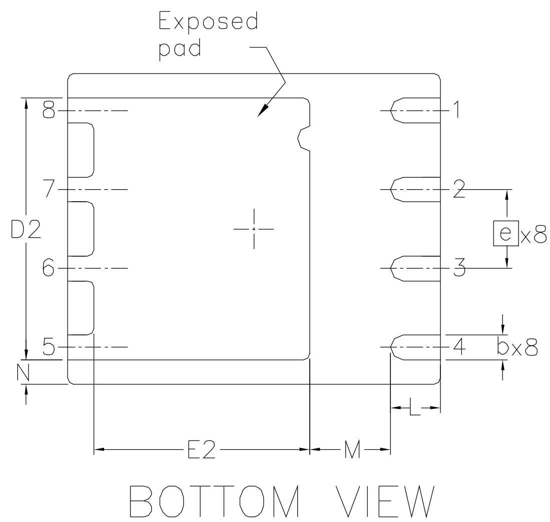


Fig 24b. Gate Charge Waveform

PQFN 5x6 Outline "B" Package Details

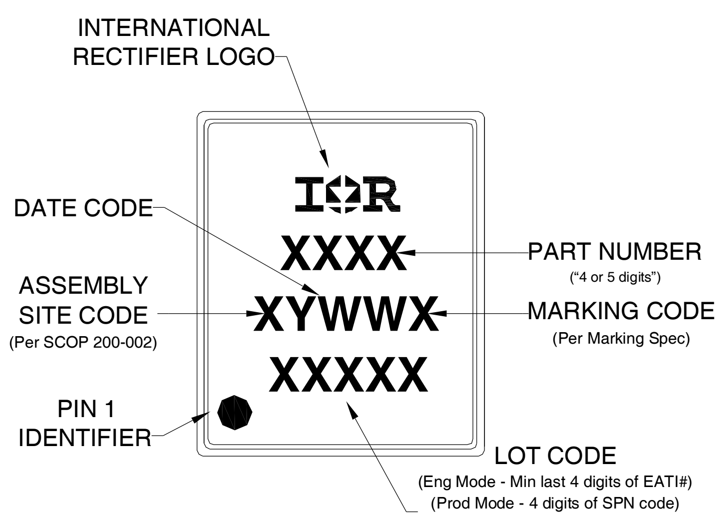


OUTLINE PQFN 5x6B			
SYMBOL \ DIM	MIN	NOM	MAX
A	0.80	0.83	0.90
A1	0	0.020	0.05
A3		0.20 REF	
b	0.35	0.40	0.47
D		5.00 BSC	
D1		4.75 BSC	
D2	4.10	4.21	4.30
e		1.27 BSC	
E		6.00 BSC	
E1		5.75 BSC	
E2	3.38	3.48	3.58
L	0.70	0.80	0.90
M		1.30 REF	
N		0.40 REF	



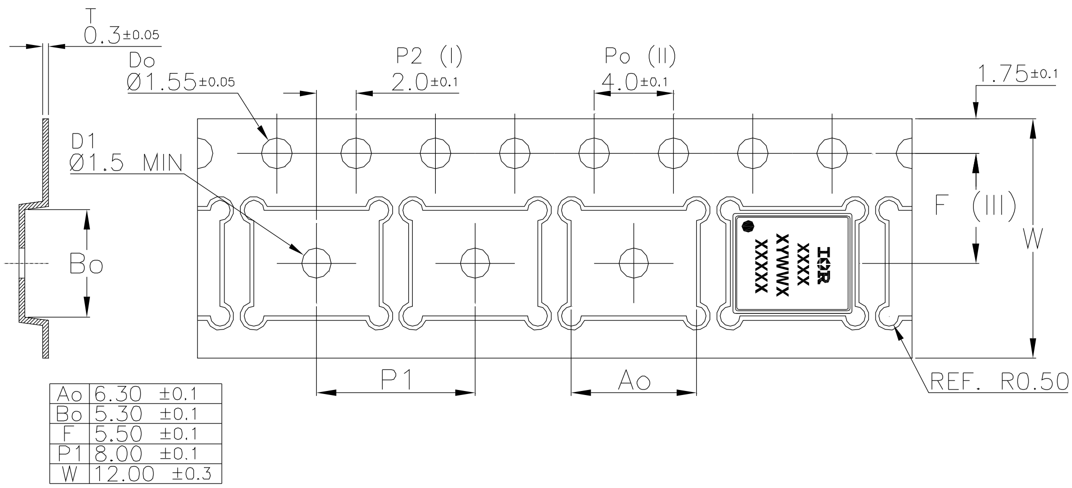
For footprint and stencil design recommendations, please refer to application note AN-1154 at
http://www.irf.com/technical-info/appnotes/an-1154.pdf

PQFN 5x6 Outline "B" Part Marking



Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

PQFN 5x6 Outline "B" Tape and Reel



Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Qualification information†

Qualification level	Industrial†† (per JEDEC JESD47F ††† guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D†††)
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http:www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

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