PD - 95289

International
IOR Rectifier

IRF7493PbF

HEXFET® Power MOSFET

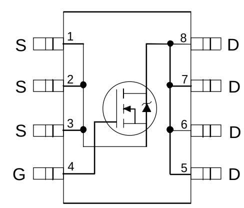
V_{DSS}	$R_{DS(on)}$ max	Qg (typ.)
80V	15mΩ@V_{GS}=10V	35nC

Applications

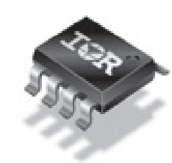
- High frequency DC-DC converters
- Lead-Free

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Top View


SO-8

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	9.3	A
I_D @ T_C = 70°C	Continuous Drain Current, V_{GS} @ 10V	7.4	
I_{DM}	Pulsed Drain Current ①	74	
P_D @T_C = 25°C	Maximum Power Dissipation ④	2.5	W
P_D @T_C = 70°C	Maximum Power Dissipation ④	1.6	
	Linear Derating Factor	0.02	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Lead	—	20	
$R_{\theta JA}$	Junction-to-Ambient ④	—	50	

Notes ① through ⑤ are on page 9

09/21/04

Static @ T_J = 25℃ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	80	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.074	——	mV/℃	Reference to 25℃, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	11.5	15	mΩ	V_{GS} = 10V, I_D = 5.6A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 80V, V_{GS} = 0V
		——	——	250		V_{DS} = 64V, V_{GS} = 0V, T_J = 125℃
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V

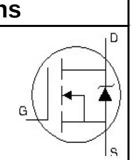
Dynamic @ T_J = 25℃ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	13	——	——	S	V_{DS} = 15V, I_D = 5.6A
Q_g	Total Gate Charge	——	35	53		I_D = 5.6A
Q_{gs}	Gate-to-Source Charge	——	5.7	——		V_{DS} = 40V
Q_{gd}	Gate-to-Drain Charge	——	12	——		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	——	8.3	——		V_{DD} = 40V, ③
t_r	Rise Time	——	7.5	——		I_D = 5.6A
$t_{d(off)}$	Turn-Off Delay Time	——	30	——	ns	R_G = 6.2Ω
t_f	Fall Time	——	12	——		V_{GS} = 10V
C_{iss}	Input Capacitance	——	1510	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	320	——	pF	V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	130	——		f = 1.0MHz
C_{oss}	Output Capacitance	——	1130	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	210	——		V_{GS} = 0V, V_{DS} = 64V, f = 1.0MHz
C_{rss} eff.	Effective Output Capacitance	——	320	——		V_{GS} = 0V, V_{DS} = 0V to 64V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	180	mJ
I_{AR}	Avalanche Current ①	——	5.6	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	9.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	74		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25℃, I_S = 5.6A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	37	56	ns	T_J = 25℃, I_F = 5.6A, V_{DD} = 15V
Q_{rr}	Reverse Recovery Charge	——	52	78	nC	di/dt = 100A/μs ③

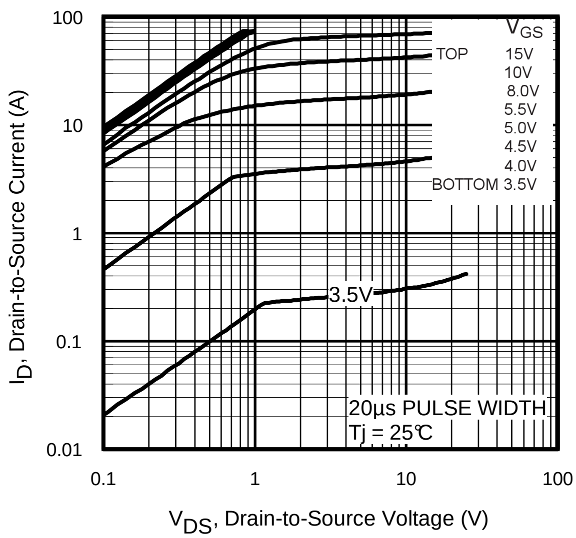


Fig 1. Typical Output Characteristics

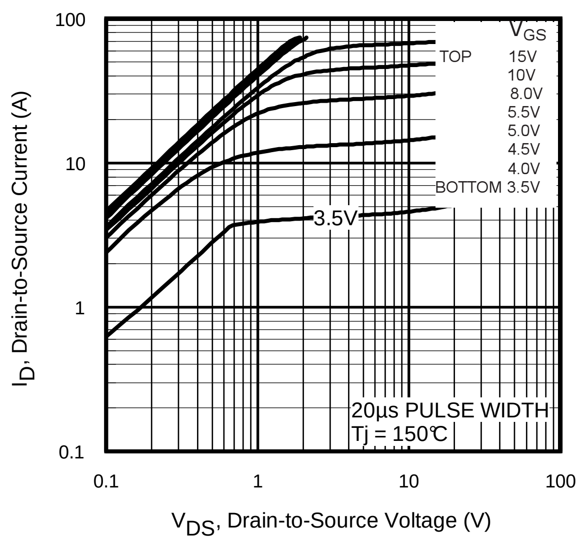


Fig 2. Typical Output Characteristics

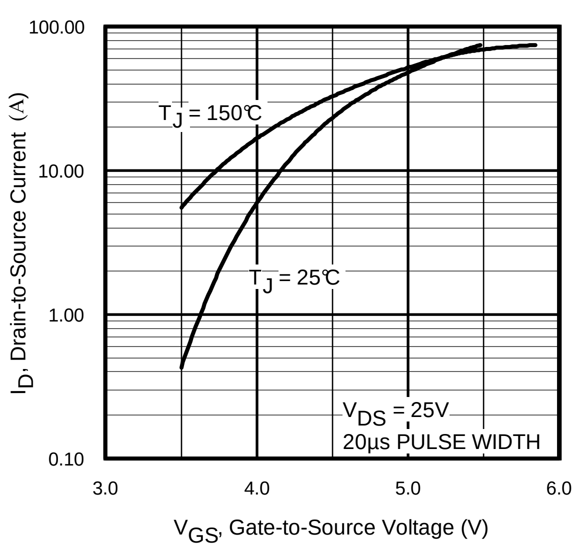


Fig 3. Typical Transfer Characteristics

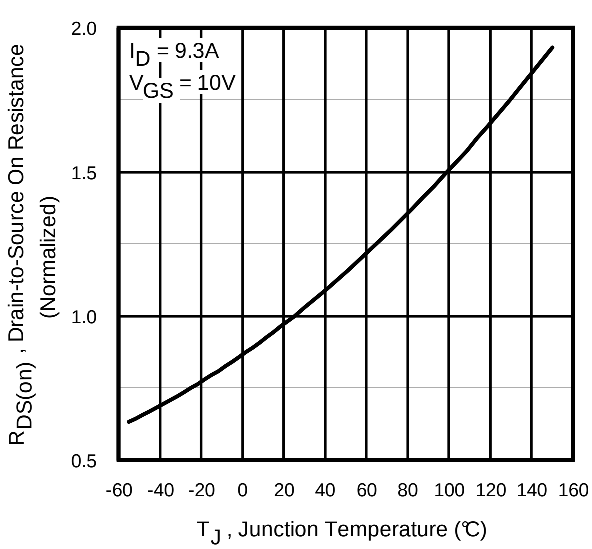


Fig 4. Normalized On-Resistance Vs. Temperature

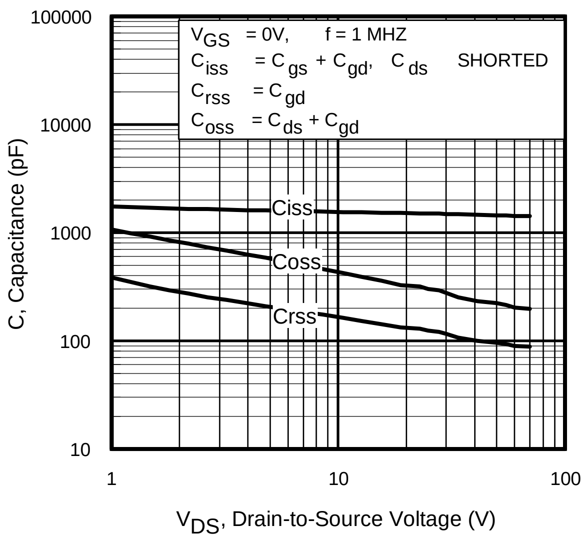


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

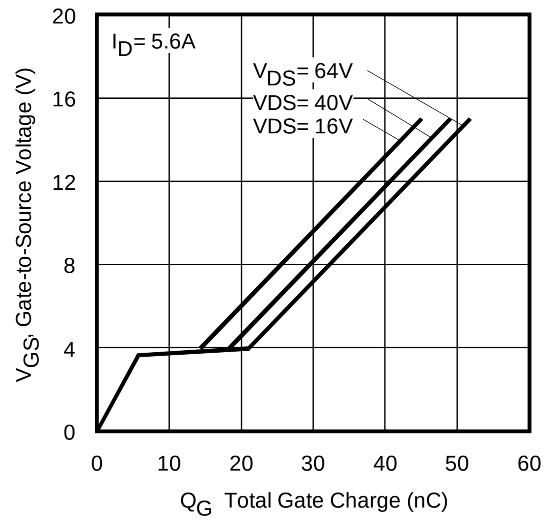


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

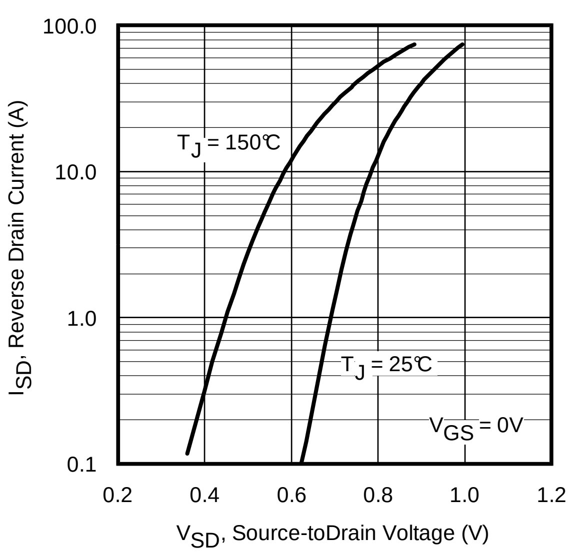


Fig 7. Typical Source-Drain Diode Forward Voltage

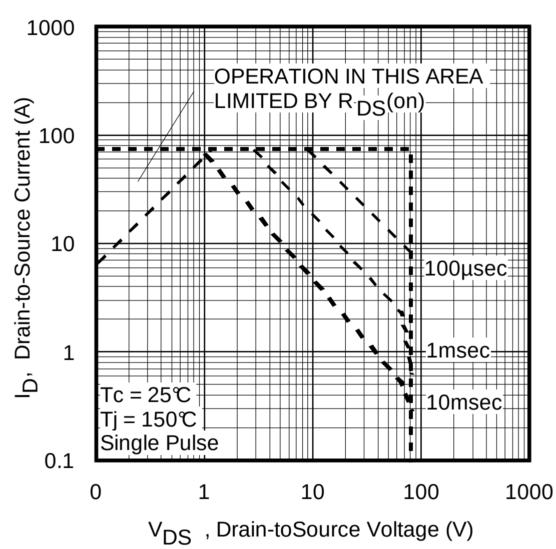


Fig 8. Maximum Safe Operating Area

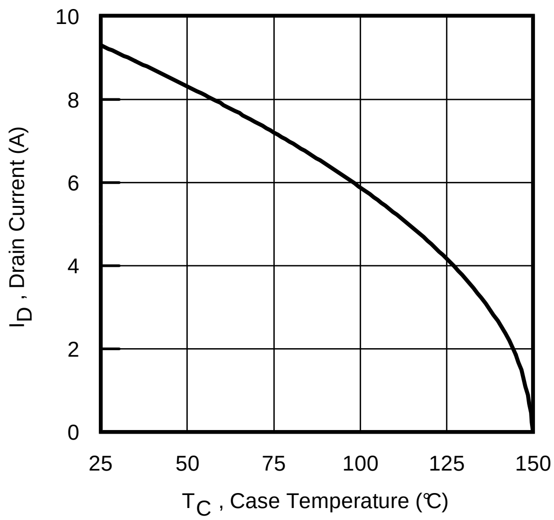


Fig 9. Maximum Drain Current Vs. Ambient Temperature

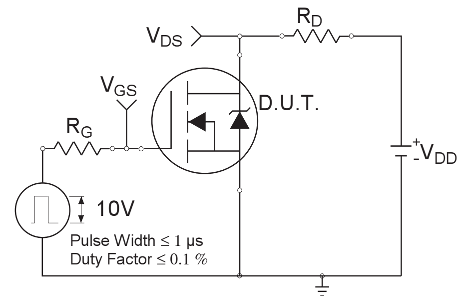


Fig 10a. Switching Time Test Circuit

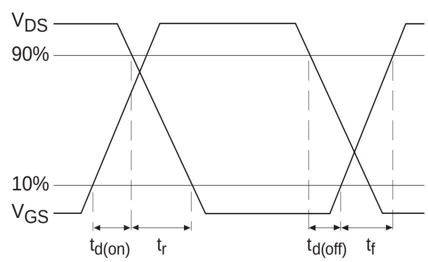


Fig 10b. Switching Time Waveforms

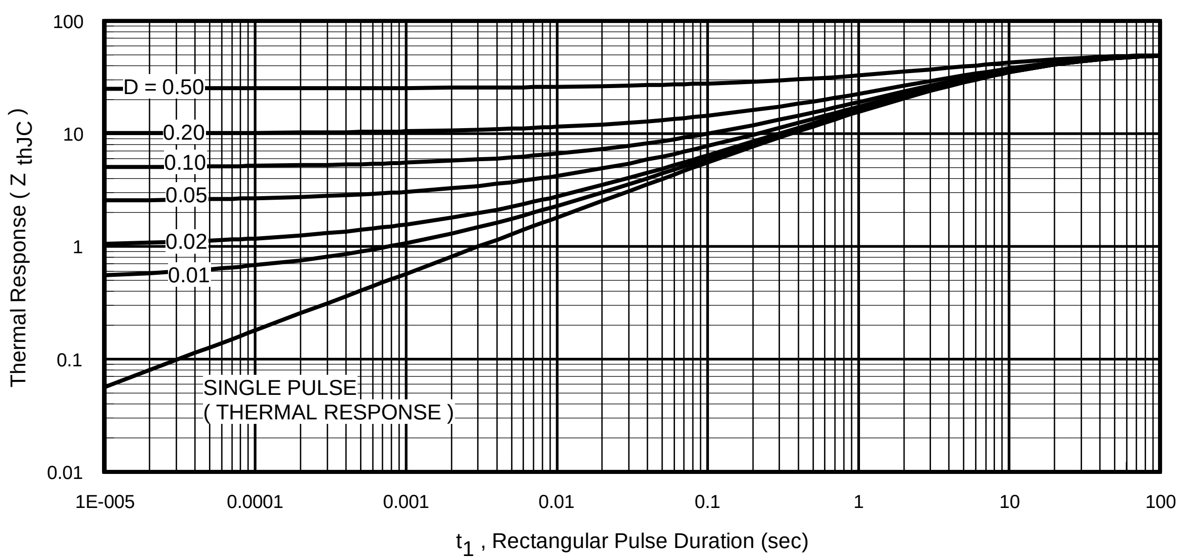


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

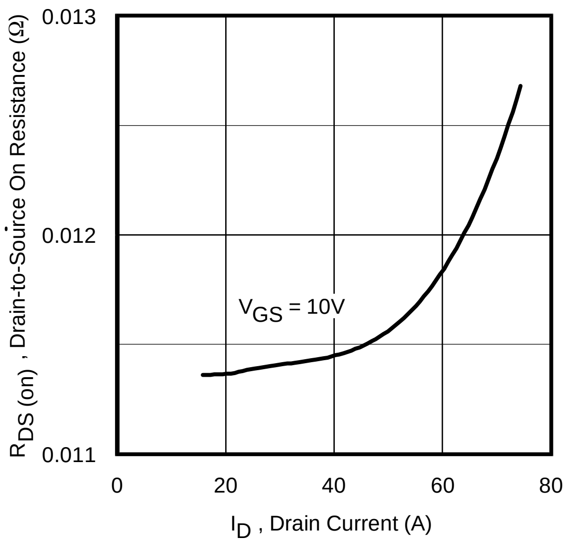


Fig 12. On-Resistance Vs. Drain Current

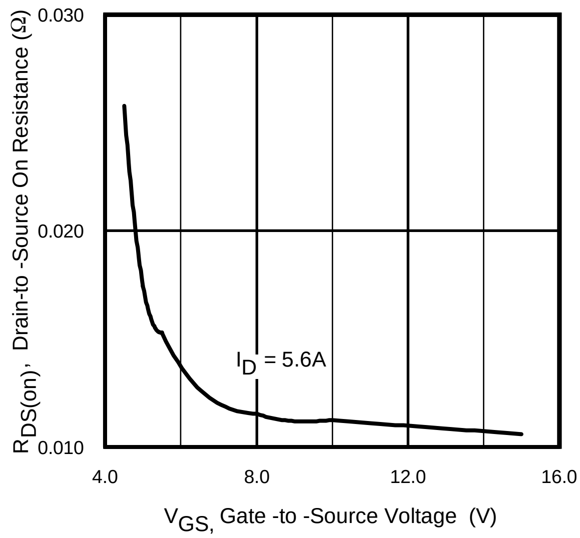


Fig 13. On-Resistance Vs. Gate Voltage

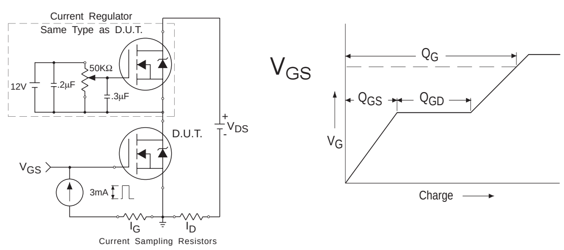


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

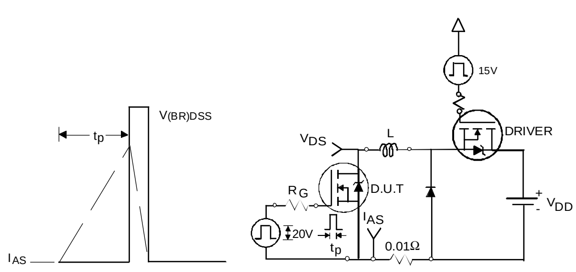


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

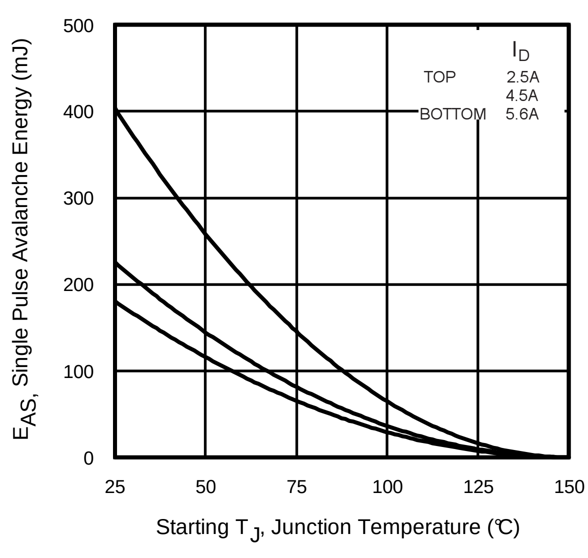


Fig 15c. Maximum Avalanche Energy Vs. Drain Current

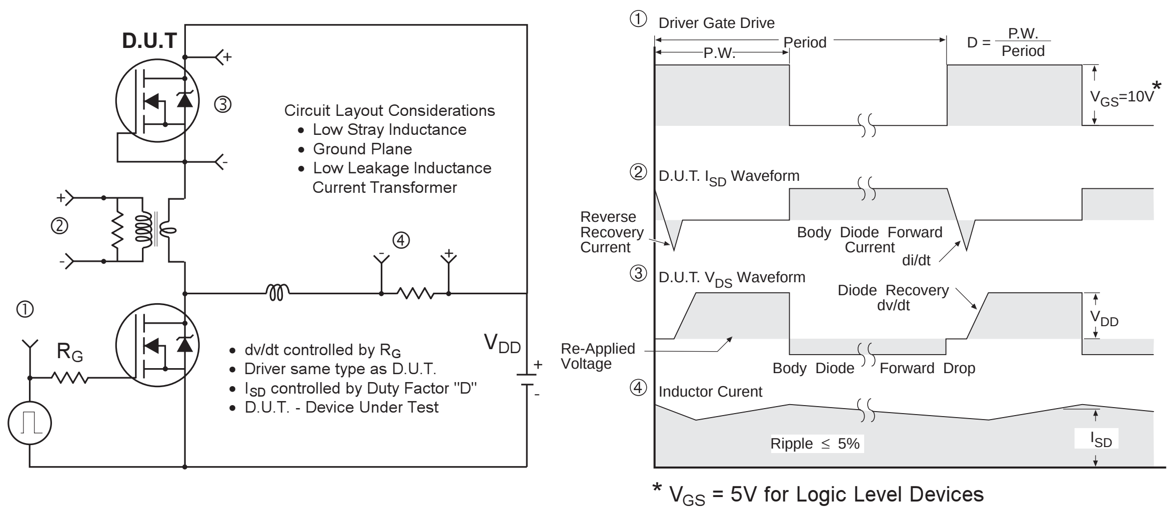


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

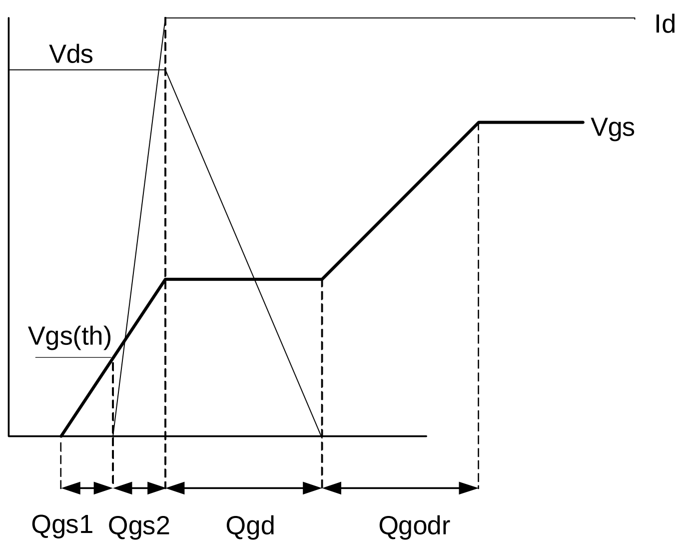
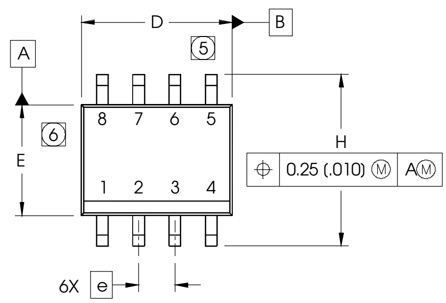


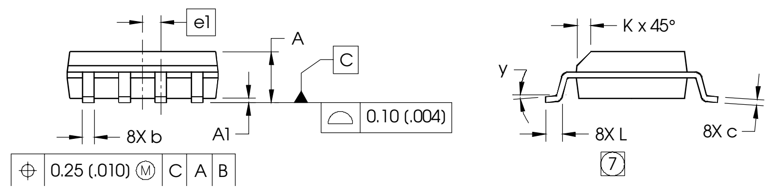
Fig 17. Gate Charge Waveform

SO-8 Package Outline

Dimensions are shown in millimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

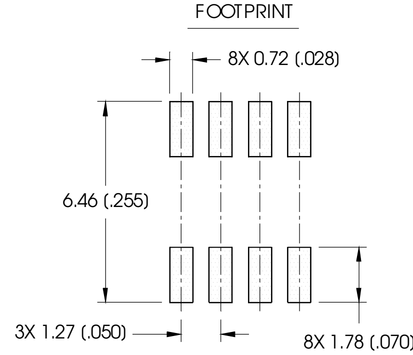


NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).

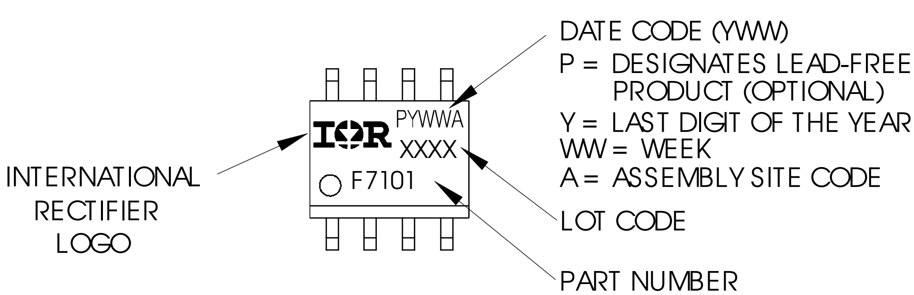
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



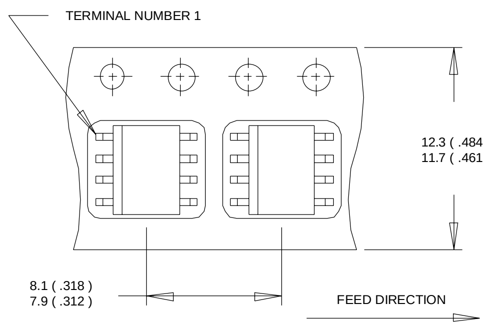
SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

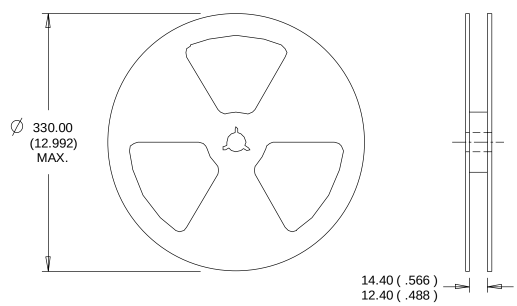


SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, L = 12mH $R_G = 25\Omega$, $I_{AS} = 5.6A$.

③ Pulse width ≤ 300µs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

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