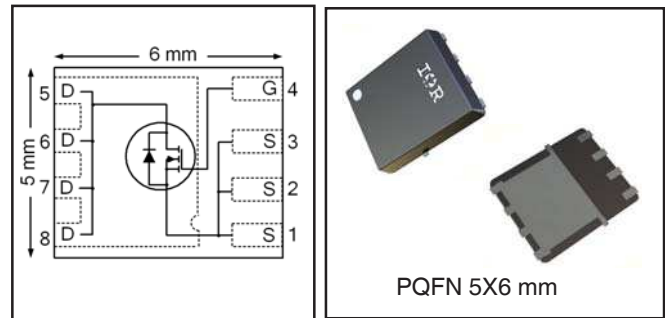


IRLH7134PbF

HEXFET® Power MOSFET

V_{DS}	40	V
$R_{DS(on) max}$ (@ $V_{GS} = 10V$)	3.3	mΩ
Q_g (typical)	39	nC
I_D (@ $T_{c(Bottom)} = 25^\circ C$)	50 ⑦	A



Applications

- Secondary Side Synchronous Rectification
- Inverters for DC Motors
- DC-DC Brick Applications
- Boost Converters

Features and Benefits

Features

Low $R_{DS(on)}$ ($\leq 4.7m\Omega$ @ $V_{GS} = 4.5V$)
Low Thermal Resistance to PCB ($< 1.2^\circ C/W$)
Low Profile (< 0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in

⇒

Benefits

Lower Conduction Losses
Enables better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLH7134TRPBF	PQFN 5mm x 6mm	Tape and Reel	4000	
IRLH7134TR2PBF	PQFN 5mm x 6mm	Tape and Reel	400	

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	± 16	
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	26	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V	21	
I_D @ $T_{c(Bottom)} = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	134⑥⑦	
I_D @ $T_{c(Bottom)} = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	85⑥⑦	
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	50⑦	
I_{DM}	Pulsed Drain Current ①	640	
P_D @ $T_A = 25^\circ C$	Power Dissipation ⑤	3.6	W
P_D @ $T_{c(Bottom)} = 25^\circ C$	Power Dissipation ⑤	104	
	Linear Derating Factor ⑤	0.029	W/°C
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Notes ① through ⑦ are on page 9

Static @ T_J = 25°C (unless otherwise specified)

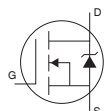
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	37	—	mV/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	2.8	3.3	mΩ	V _{GS} = 10V, I _D = 50A ③
			3.9	4.9		V _{GS} = 4.5V, I _D = 40A ③
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.5	V	V _{DS} = V _{GS} , I _D = 100μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-5.6	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 40V, V _{GS} = 0V
				250		V _{DS} = 40V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -16V
g _{fs}	Forward Transconductance	120	—	—	S	V _{DS} = 10V, I _D = 50A
Q _g	Total Gate Charge	—	39	58	nC	V _{DS} = 20V V _{GS} = 4.5V I _D = 50A
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	9.0	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	4.5	—		
Q _{gd}	Gate-to-Drain Charge	—	16	—		
Q _{godr}	Gate Charge Overdrive	—	9.5	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	20.5	—		
Q _{oss}	Output Charge	—	23	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	0.6	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	21	—	ns	V _{DD} = 20V, V _{GS} = 10V I _D = 50A R _G = 1.7Ω
t _r	Rise Time	—	75	—		
t _{d(off)}	Turn-Off Delay Time	—	18	—		
t _f	Fall Time	—	13	—		
C _{iss}	Input Capacitance	—	3720	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	610	—		
C _{rss}	Reverse Transfer Capacitance	—	350	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	125	mJ
I _{AR}	Avalanche Current ①	—	50	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	50 ⑦	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	640		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 50A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	25	38	ns	T _J = 25°C, I _F = 50A, V _{DD} = 20V
Q _{rr}	Reverse Recovery Charge	—	74	110	nC	di/dt = 400A/μs ③
t _{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				



Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC} (Bottom)	Junction-to-Case ④	—	1.2	°C/W
R _{θJC} (Top)	Junction-to-Case ④	—	30	
R _{θJA}	Junction-to-Ambient ⑤	—	35	
R _{θJA} (<10s)	Junction-to-Ambient ⑤	—	22	

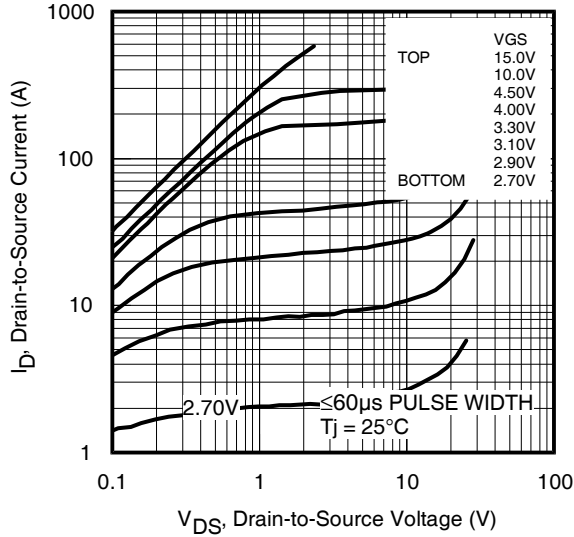


Fig 1. Typical Output Characteristics

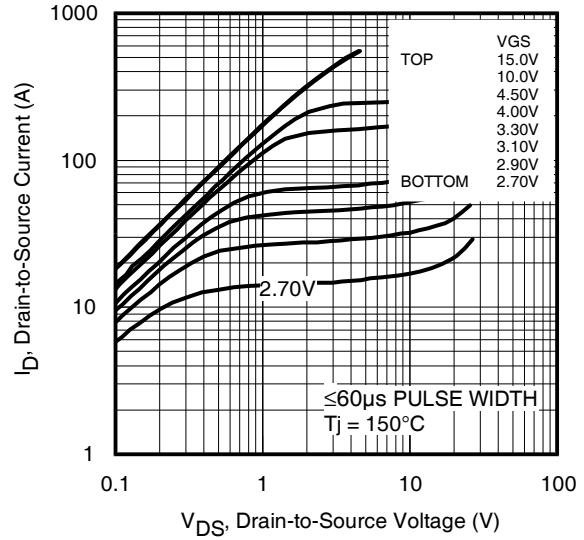


Fig 2. Typical Output Characteristics

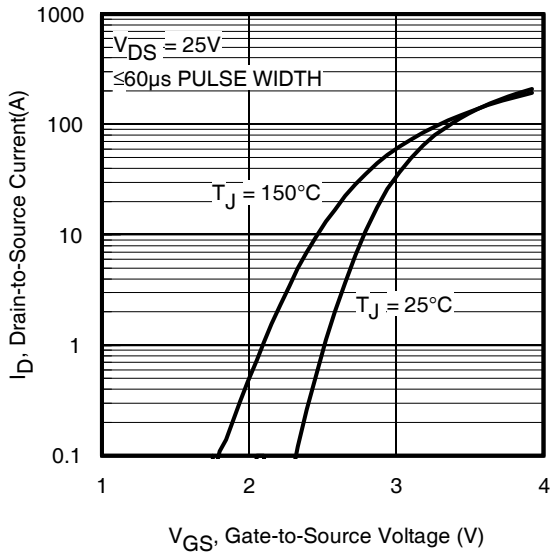


Fig 3. Typical Transfer Characteristics

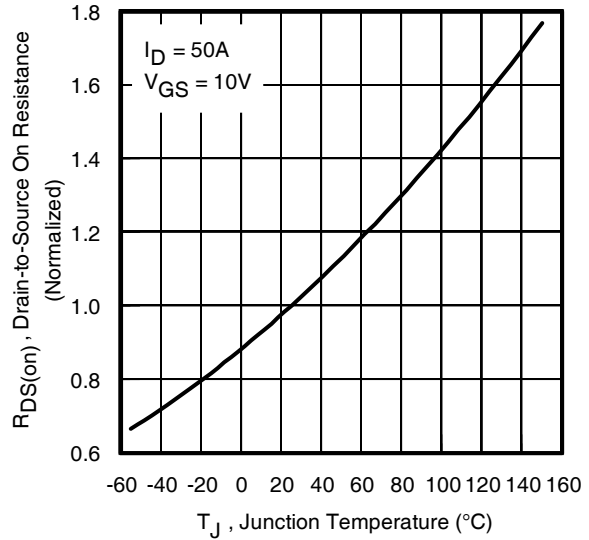


Fig 4. Normalized On-Resistance vs. Temperature

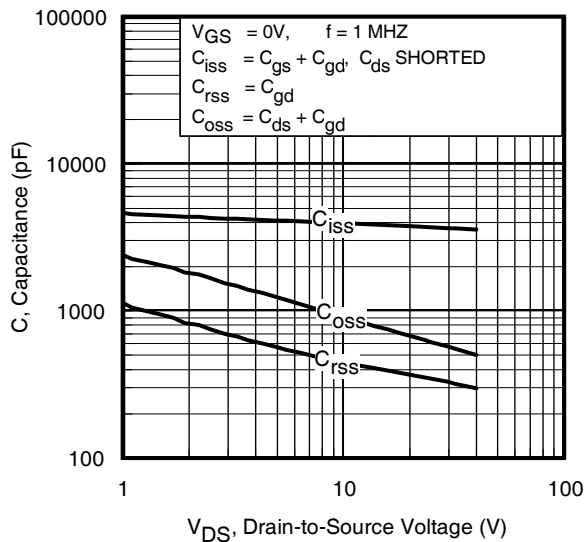


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage
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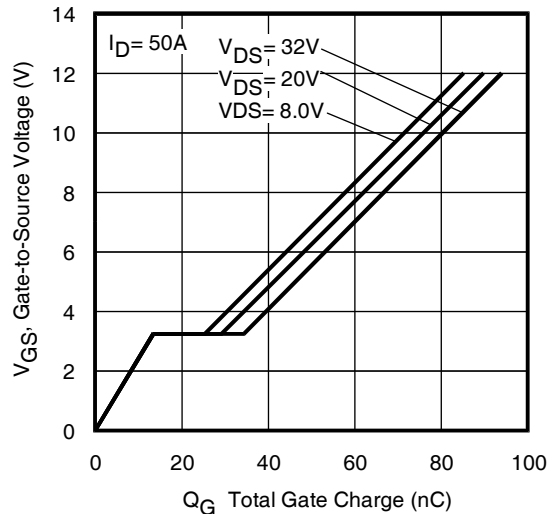


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

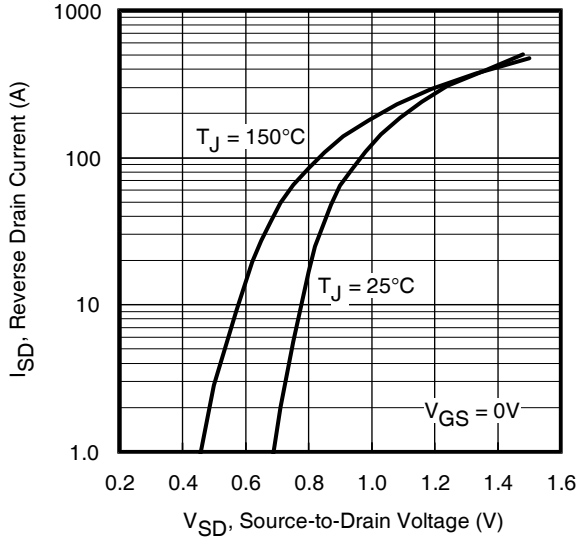


Fig 7. Typical Source-Drain Diode Forward Voltage

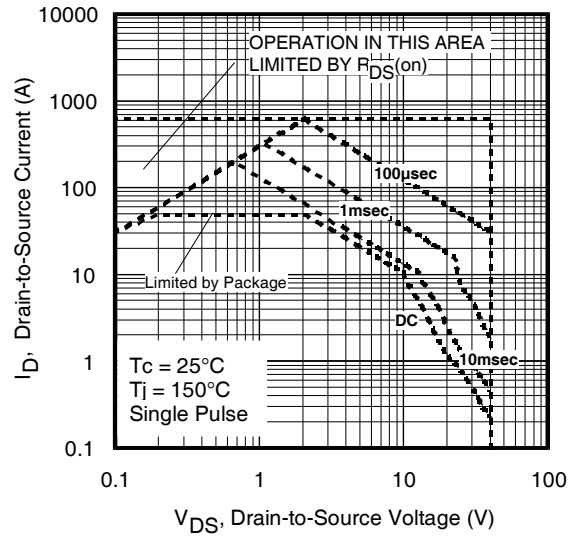


Fig 8. Maximum Safe Operating Area

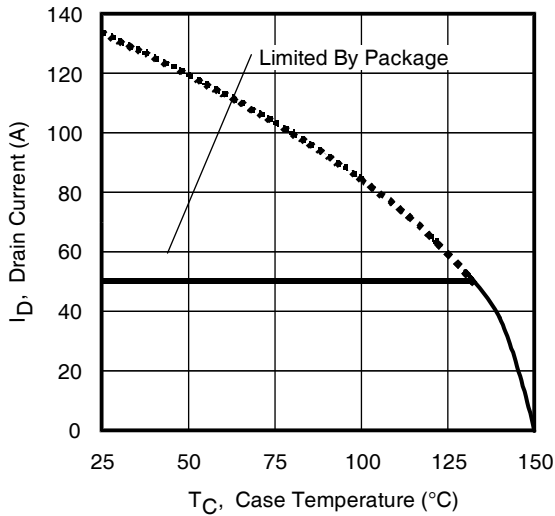


Fig 9. Maximum Drain Current vs. Case (Bottom) Temperature

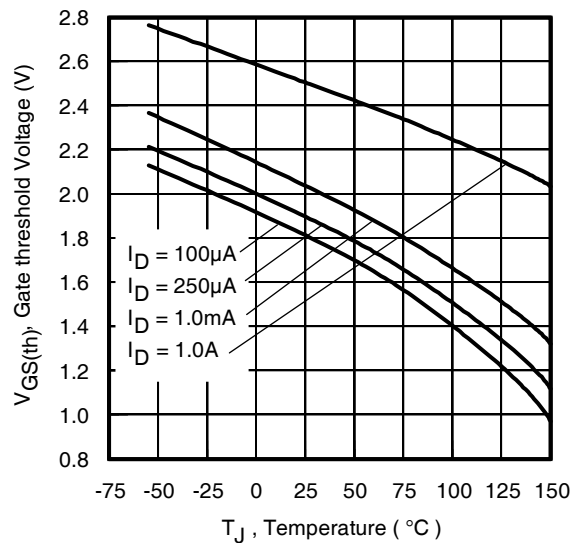


Fig 10. Threshold Voltage vs. Temperature

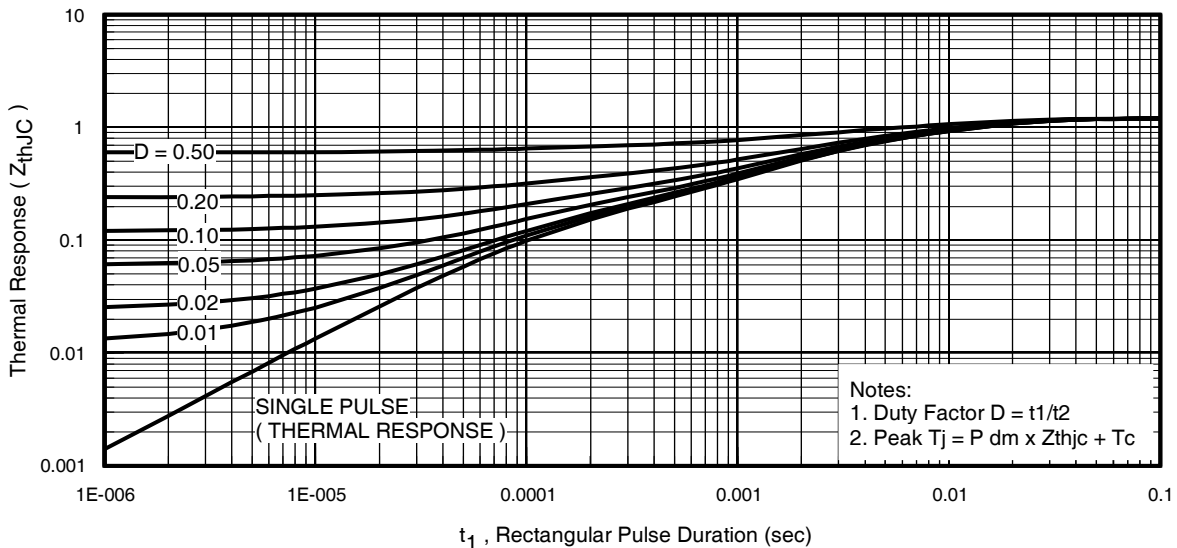


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)

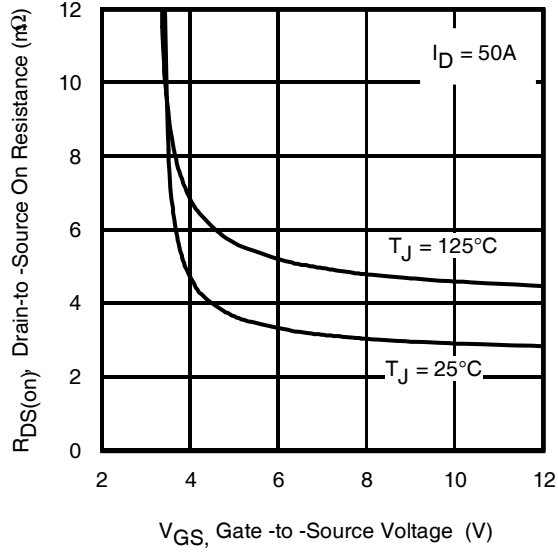


Fig 12. On-Resistance vs. Gate Voltage

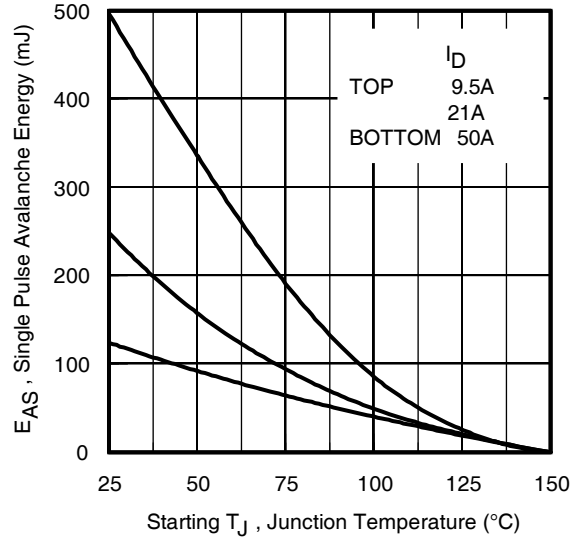


Fig 13. Maximum Avalanche Energy vs. Drain Current

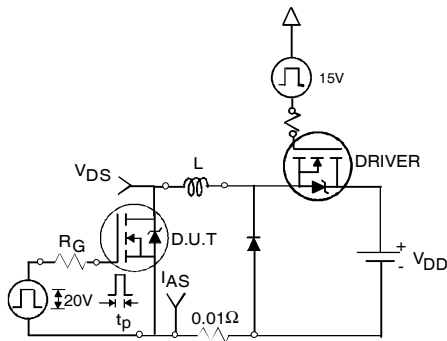


Fig 14a. Unclamped Inductive Test Circuit

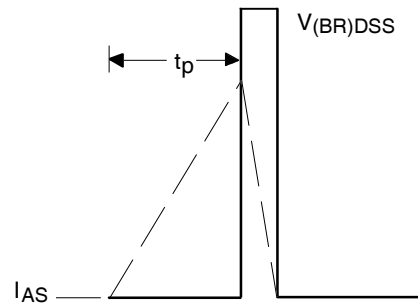


Fig 14b. Unclamped Inductive Waveforms

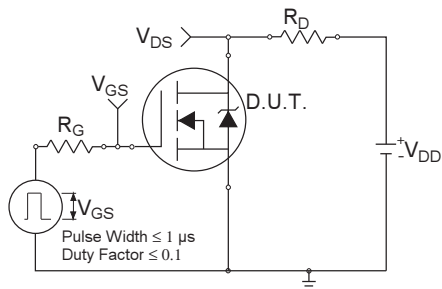


Fig 15a. Switching Time Test Circuit

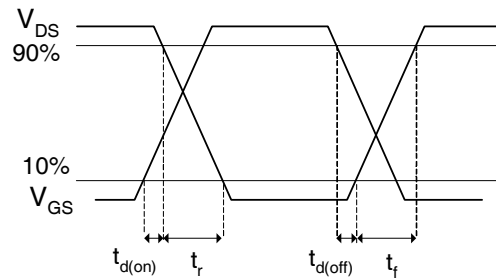


Fig 15b. Switching Time Waveforms

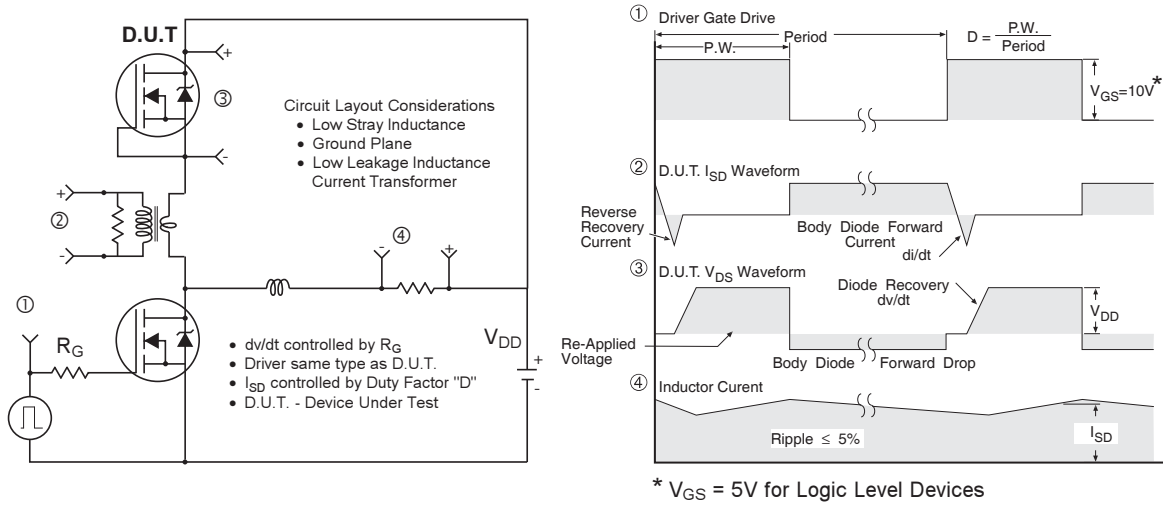


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

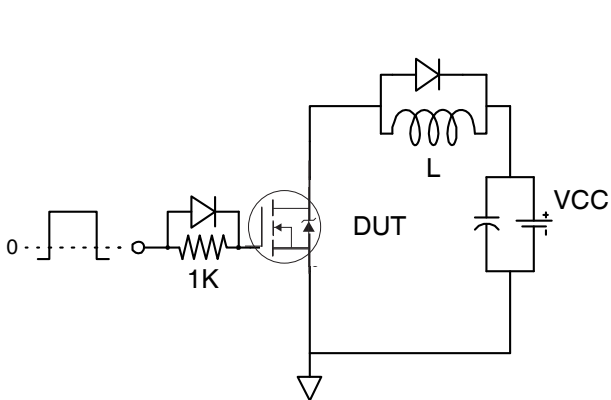


Fig 17. Gate Charge Test Circuit

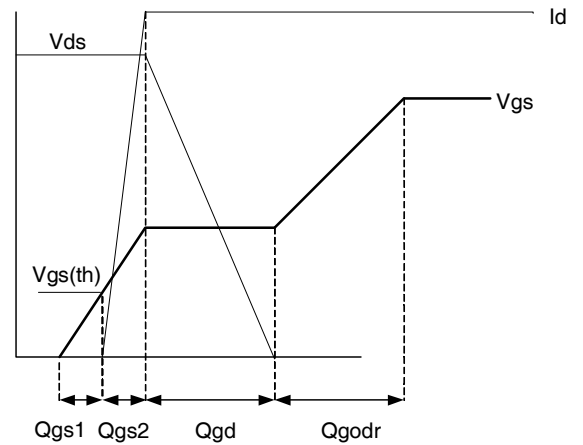
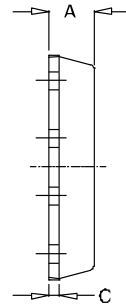
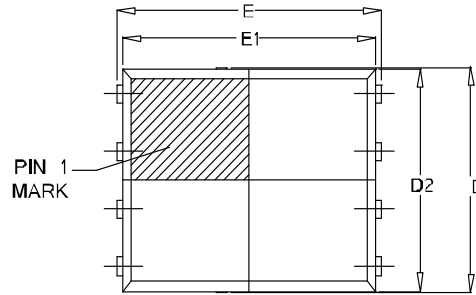


Fig 18. Gate Charge Waveform

PQFN 5x6 Outline "E" Package Details

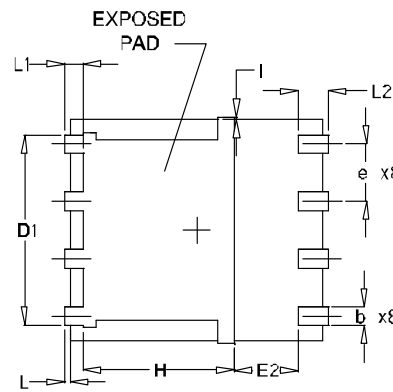


SIDEVIEW



TOP VIEW

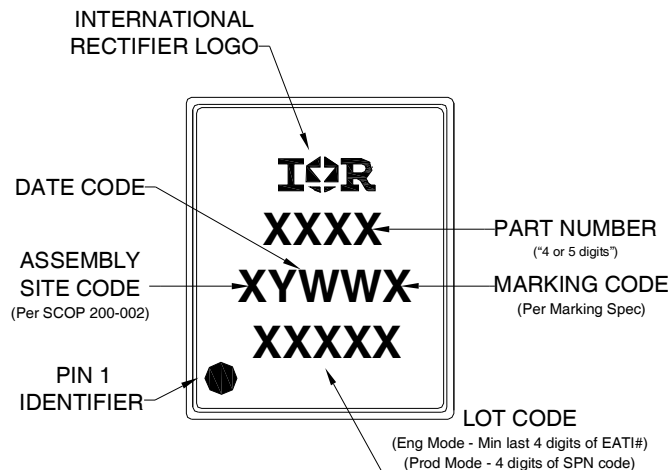
SYMBOL	OUTLINE PQFN 5X6E		
	MIN.	NOM.	MAX.
A	0.90	1.03	1.17
b	0.33	0.41	0.48
C	0.20	0.25	0.35
D	4.80	4.98	5.15
D1	3.91	4.11	4.31
D2	4.80	4.90	5.00
E	5.90	6.02	6.15
E1	5.65	5.75	5.85
E2	1.10	—	—
e	1.27 BSC		
L	0.05	0.15	0.25
L1	0.38	0.44	0.50
L2	0.51	0.68	0.86
H	3.32	3.45	3.58
I	—	—	0.18



BOTTOM VIEW

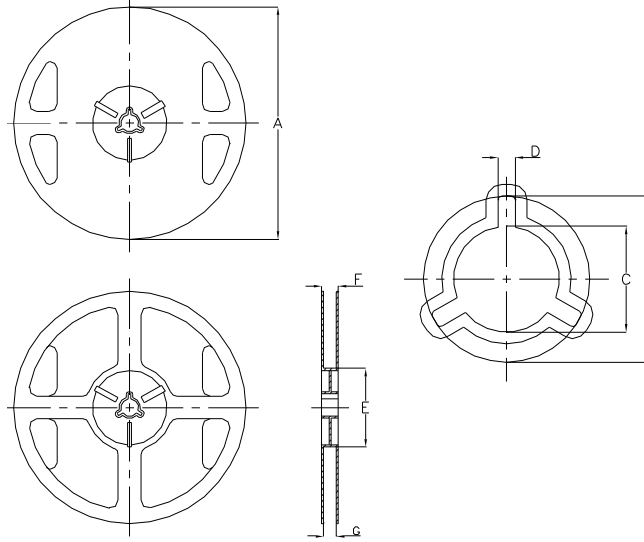
For footprint and stencil design recommendations, please refer to application note AN-1154 at <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "E" Part Marking



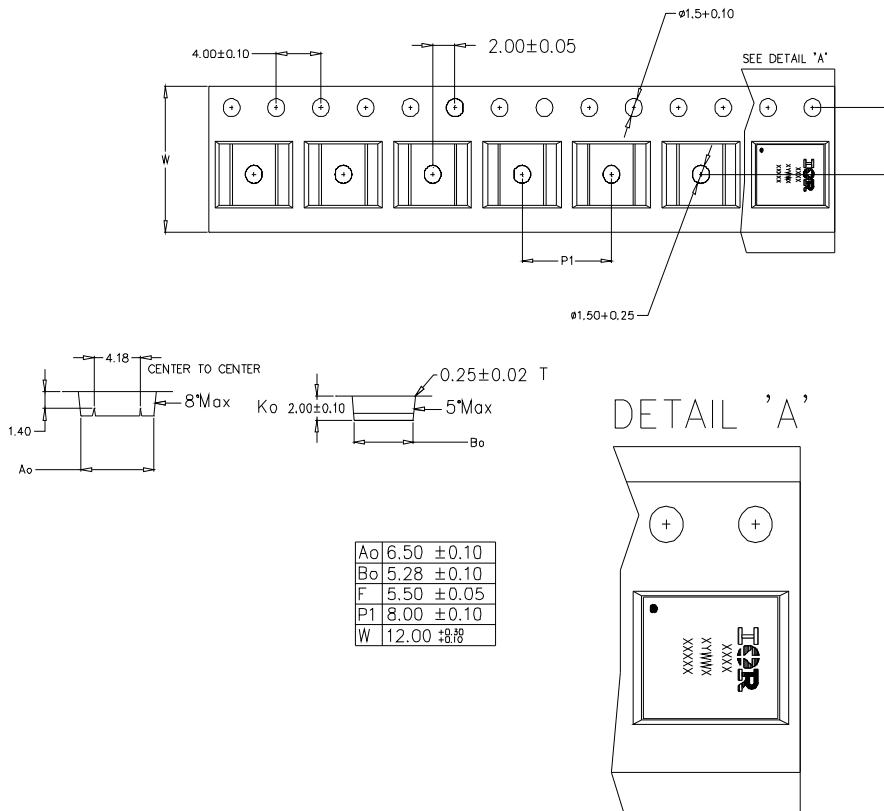
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>
www.irf.com

PQFN 5x6 Outline "E" Tape and Reel



NOTE: Controlling dimensions in mm Std reel quantity is 4000 parts.

REEL DIMENSIONS								
CODE	STANDARD OPTION (QTY 4000)				TR1 OPTION (QTY 400)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
A	329.5	330.5	12.972	13.011	177.5	178.5	6.988	7.028
B	20.9	21.5	0.823	0.846	20.9	21.5	0.823	0.846
C	12.8	13.5	0.504	0.532	13.2	13.8	0.520	0.543
D	1.7	2.3	0.067	0.091	1.9	2.3	0.075	0.091
E	97	99	3.819	3.898	65	66	2.350	2.598
F	Ref	17.4			Ref	12		
G	13	14.5	0.512	0.571	13	14.5	0.512	0.571



Qualification information[†]

Qualification level	Industrial ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.
 Please contact your International Rectifier sales representative for further information:
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.099\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 50\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Package is limited to 50A by die-source to lead-frame bonding technology

Data and specifications subject to change without notice.

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