# International **I⚙R** Rectifier

IRLS4030-7PPbF

HEXFET® Power MOSFET

Applications
- DC Motor Drive
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Optimized for Logic Level Drive
- Very Low $R_{DS(ON)}$ at 4.5V V_{GS}
- Superior R*Q at 4.5V V_{GS}
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
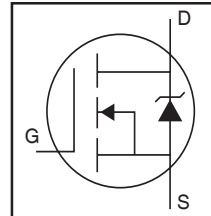
V_{DSS}		**100V**
$R_{DS(on)}$	**typ.**	**3.2mΩ**
	max.	**3.9mΩ**
I_D		**190A**

D²Pak 7 Pin
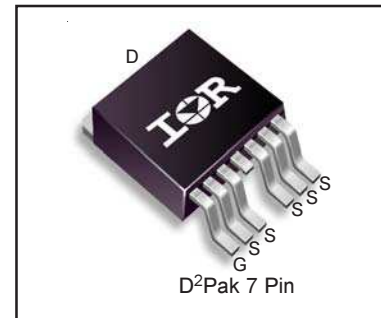
G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	190	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	130	A
I_{DM}	Pulsed Drain Current ①	750	
P_D @T_C = 25°C	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
dv/dt	Peak Diode Recovery ③	13	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

$E_{AS \text{ (Thermally limited)}}$	Single Pulse Avalanche Energy ②	320	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ④		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧⑨	——	0.40	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦⑧	——	40	
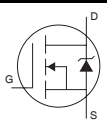
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.10	——	V/°C	Reference to 25°C, I_D = 5mA①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	3.2	3.9	mΩ	V_{GS} = 10V, I_D = 110A ④
		——	3.3	4.1		V_{GS} = 4.5V, I_D = 94A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	——	2.5	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 100V, V_{GS} = 0V
		——	——	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -16V
$R_{G(int)}$	Internal Gate Resistance	——	2.0	——	Ω	

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	250	——	——	S	V_{DS} = 25V, I_D = 110A
Q_g	Total Gate Charge	——	93	140	nC	I_D = 110A
Q_{gs}	Gate-to-Source Charge	——	27	——		V_{DS} = 50V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	43	——		V_{GS} = 4.5V ④
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	50	——		I_D = 110A, V_{DS} =0V, V_{GS} = 4.5V
$t_{d(on)}$	Turn-On Delay Time	——	53	——	ns	V_{DD} = 65V
t_r	Rise Time	——	160	——		I_D = 110A
$t_{d(off)}$	Turn-Off Delay Time	——	110	——		R_G = 2.7Ω
t_f	Fall Time	——	87	——		V_{GS} = 4.5V ④
C_{iss}	Input Capacitance	——	11490	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	680	——		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	——	300	——	pF	f = 1.0MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)⑥	——	760	——		V_{GS} = 0V, V_{DS} = 0V to 80V ⑥
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑤	——	1170	——		V_{GS} = 0V, V_{DS} = 0V to 80V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	190	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	750		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 110A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	53	——	ns	T_J = 25°C V_R = 85V,
		——	63	——		T_J = 125°C I_F = 110A
Q_{rr}	Reverse Recovery Charge	——	99	——	nC	T_J = 25°C di/dt = 100A/µs ④
		——	155	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	3.3	——	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.05mH
   R_G = 25Ω, I_{AS} = 110A, V_{GS} =10V. Part not recommended for use above this value .

③ I_{SD} ≤ 110A, di/dt ≤ 1520A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑧ R_θ is measured at T_J approximately 90°C.

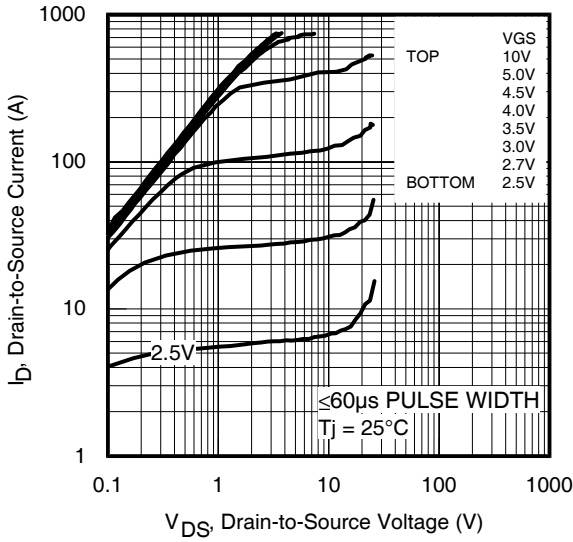⑨ $R_{\theta JC}$ value shown is at time zero.

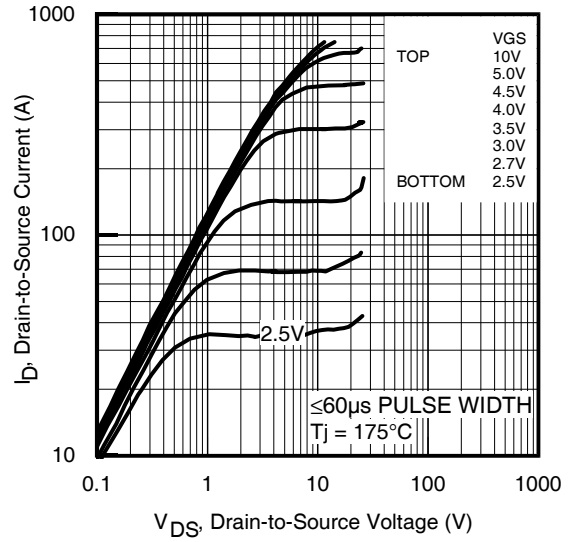**Fig 1.** Typical Output Characteristics

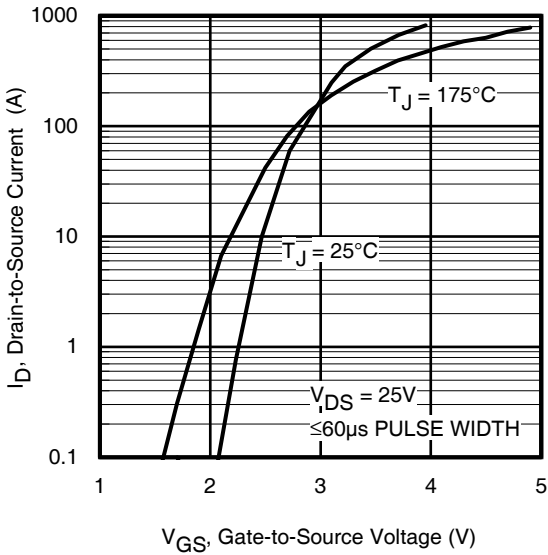**Fig 2.** Typical Output Characteristics

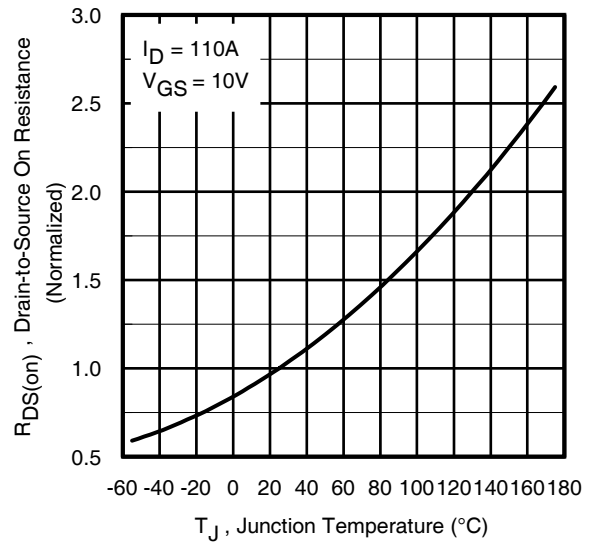**Fig 3.** Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature
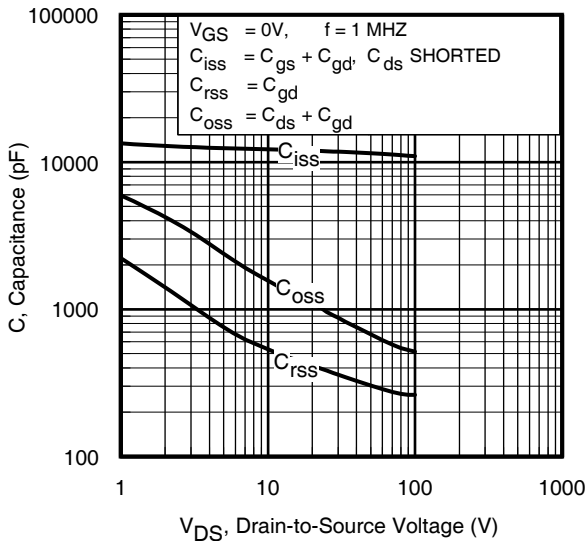

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage
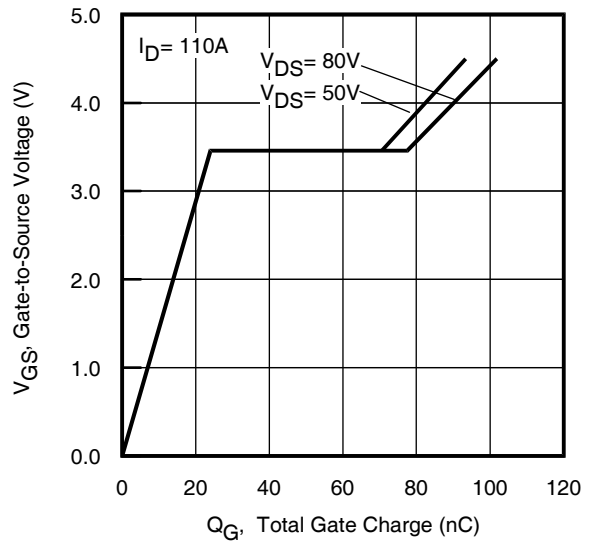

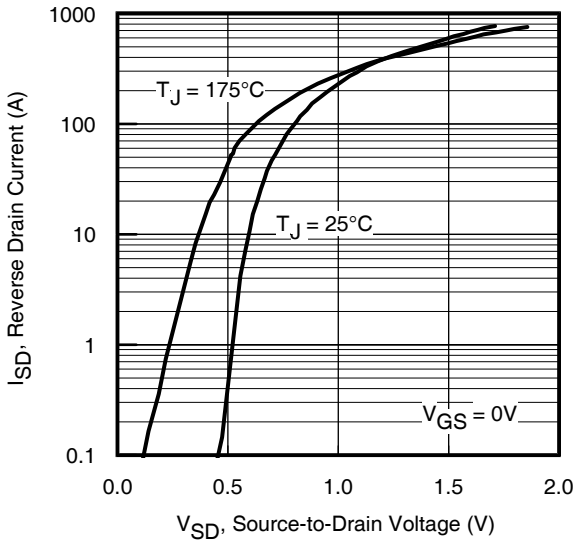**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

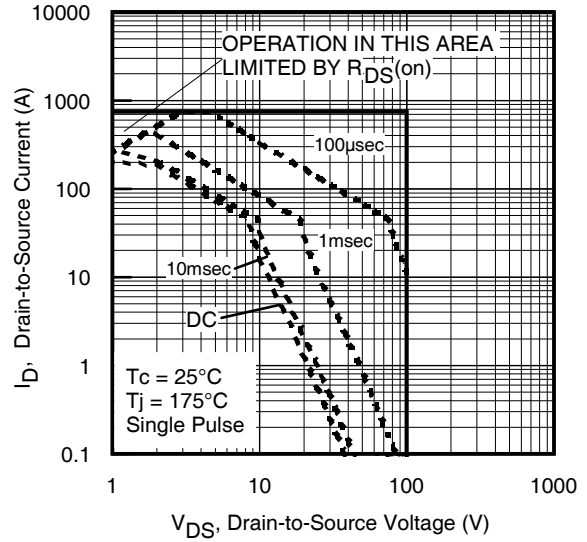**Fig 7.** Typical Source-Drain Diode
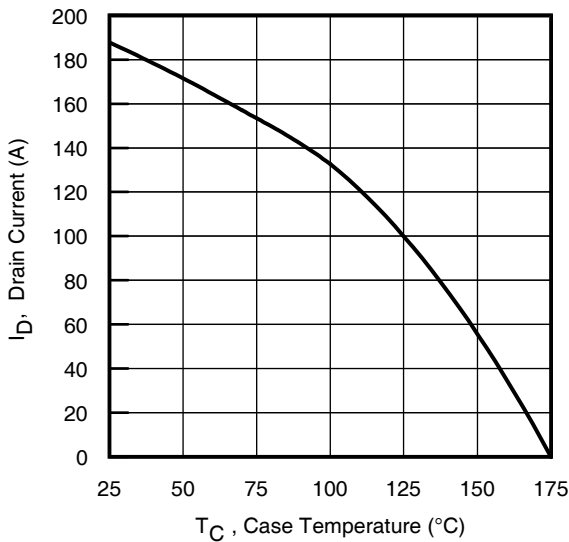Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs.
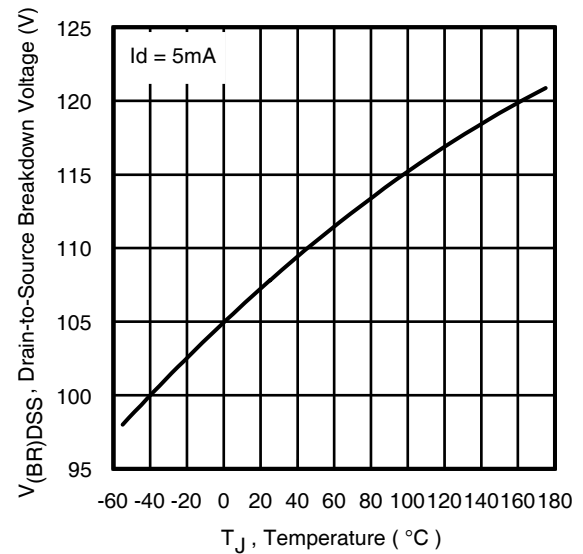Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage
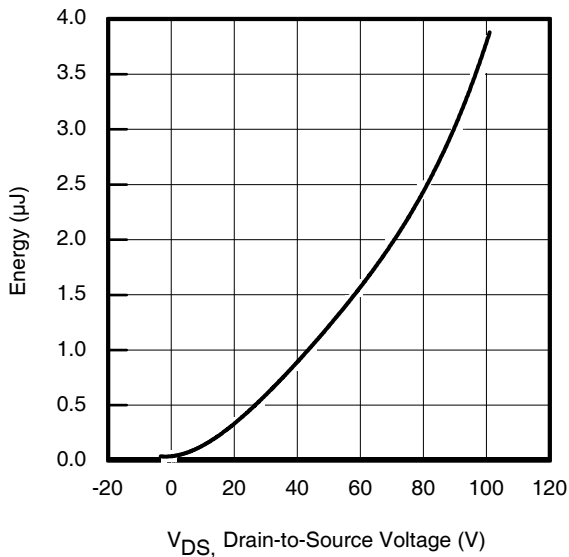

Fig 11. Typical C_{OSS} Stored Energy

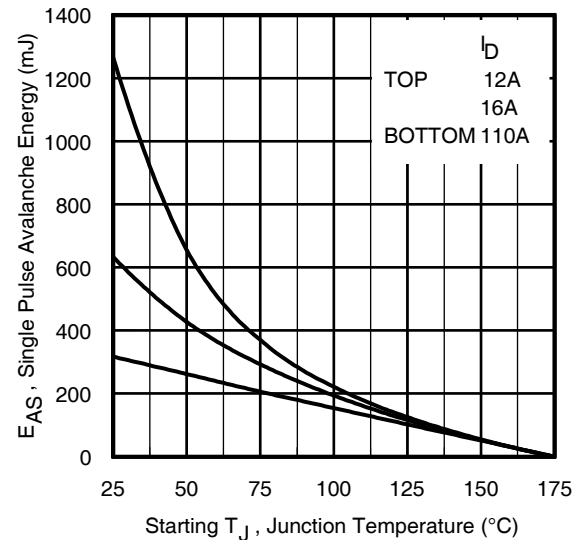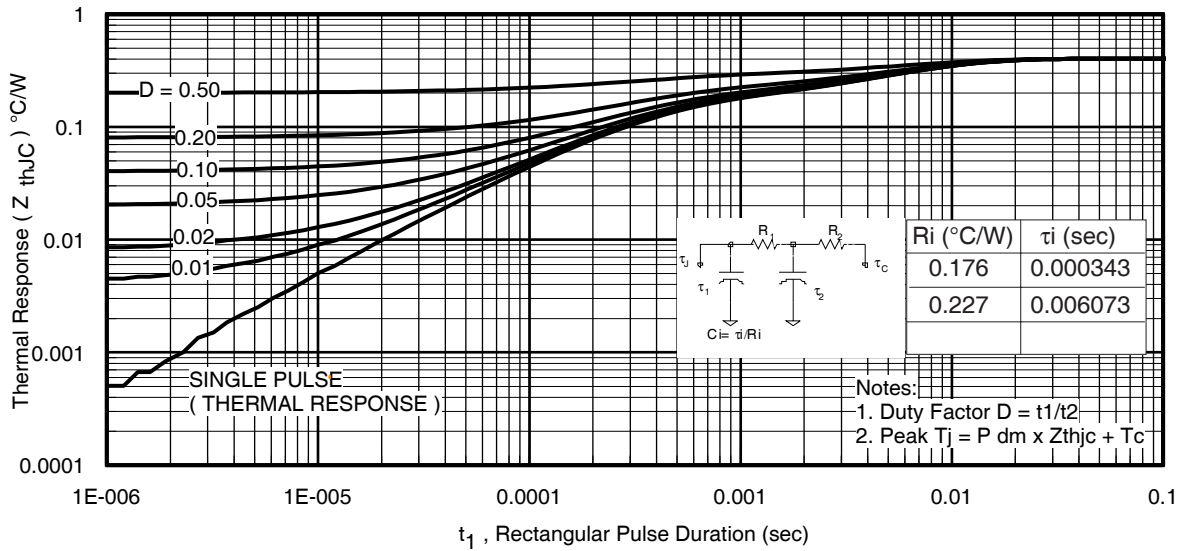**Fig 12.** Maximum Avalanche Energy vs. DrainCurrent

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

The table in Fig 13:

Ri (°C/W)	τi (sec)
0.176	0.000343
0.227	0.006073

Notes:
1. Duty Factor D = t1/t2
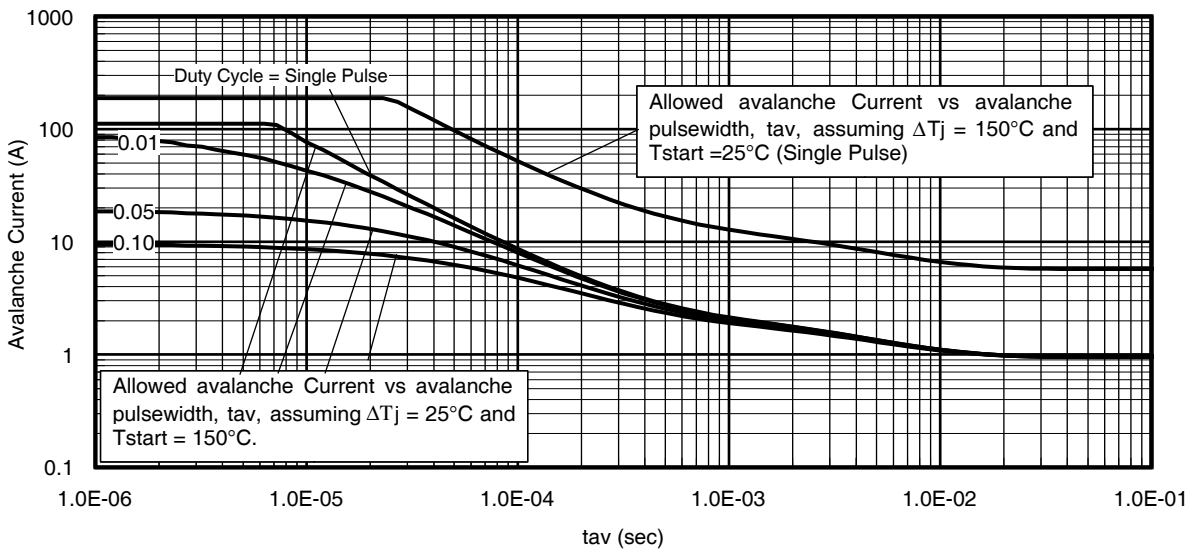2. Peak Tj = P dm x Zthjc + Tc

Fig 14. Typical Avalanche Current vs.Pulsewidth
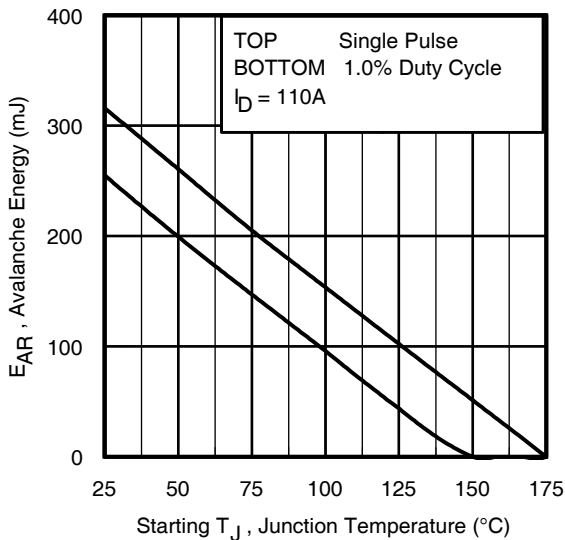

Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
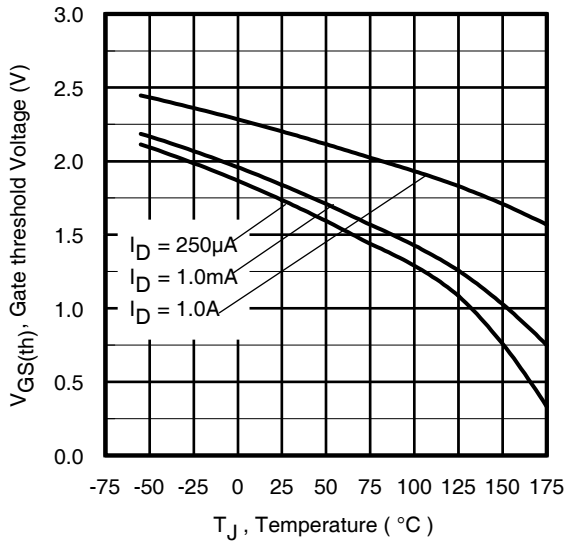$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$
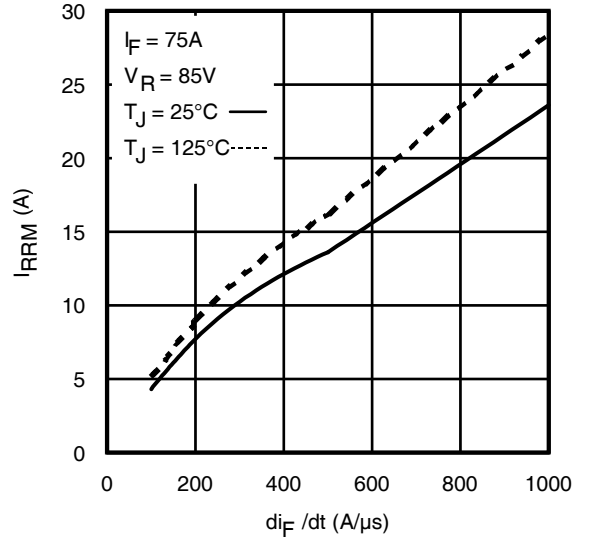
Fig 16. Threshold Voltage vs. Temperature

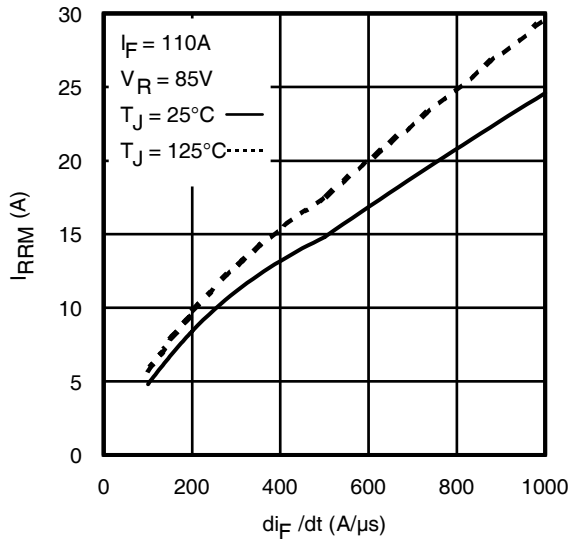**Fig. 17** - Typical Recovery Current vs. di$_f$/dt

Fig. 18 - Typical Recovery Current vs. di$_f$/dt
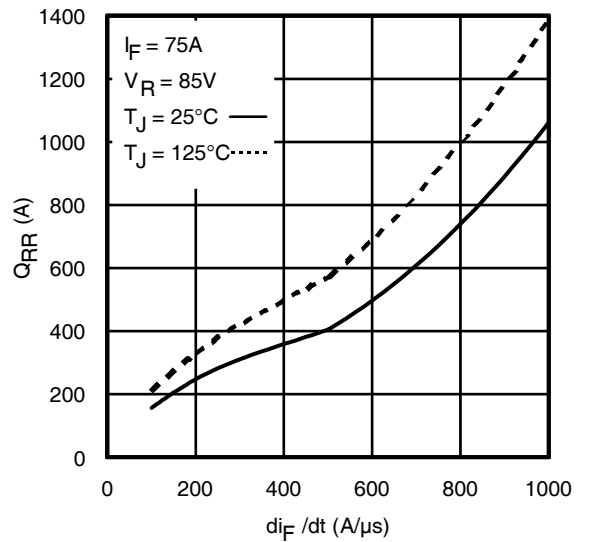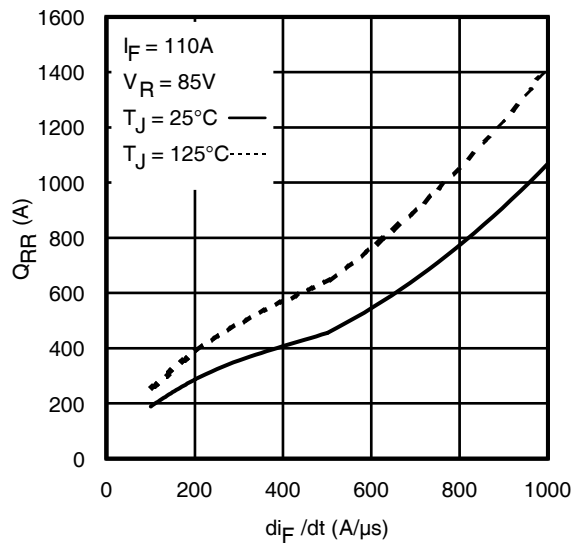

Fig. 19 - Typical Stored Charge vs. di$_f$/dt

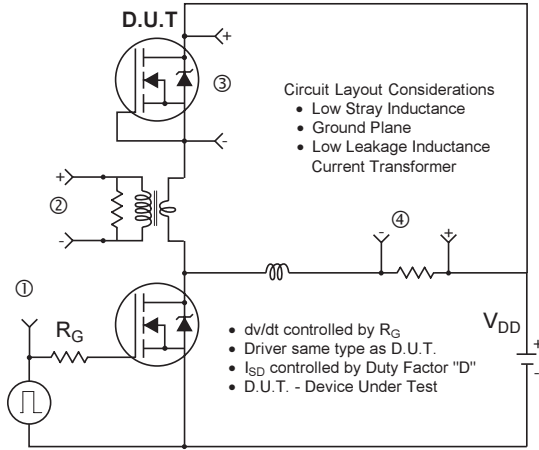**Fig. 20** - Typical Stored Charge vs. di$_f$/dt

D.U.T

Circuit Layout Considerations
• Low Stray Inductance
• Ground Plane
• Low Leakage Inductance
  Current Transformer

③

②

① R_G

• dv/dt controlled by R_G
• Driver same type as D.U.T.
• I_{SD} controlled by Duty Factor "D"
• D.U.T. - Device Under Test

V_{DD}

① Driver Gate Drive

P.W.   Period $D = \dfrac{P.W.}{Period}$

V_{GS}=10V *

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Current

Ripple ≤ 5% I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

15V

V_{DS} L DRIVER

R_G D.U.T.

V_{GS} I_{AS}

t_p 0.01Ω

V_{DD}
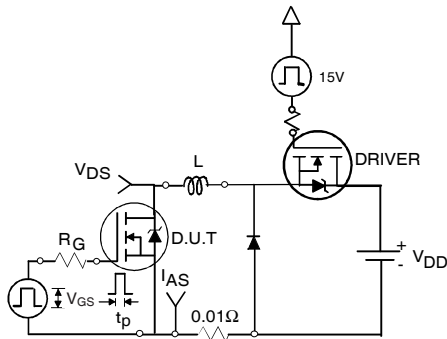
Fig 22a. Unclamped Inductive Test Circuit

$V_{(BR)DSS}$

t_p

I_{AS}
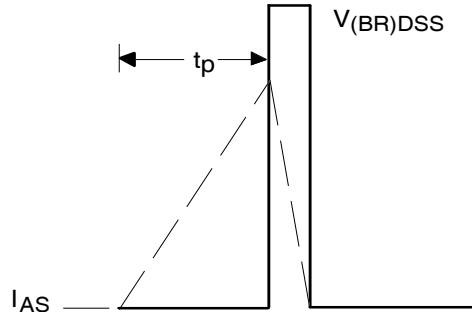
Fig 22b. Unclamped Inductive Waveforms

R_D

V_{DS}

V_{GS}

R_G D.U.T.

V_{GS}

Pulse Width ≤ 1 µs
Duty Factor ≤ 0.1 %

V_{DD}
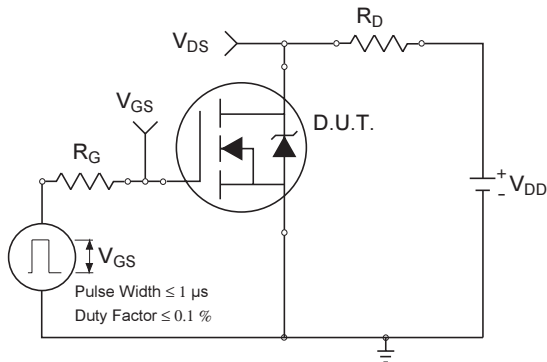
Fig 23a. Switching Time Test Circuit

V_{DS}

90%

10%

V_{GS}

$t_{d(on)}$ t_r $t_{d(off)}$ t_f
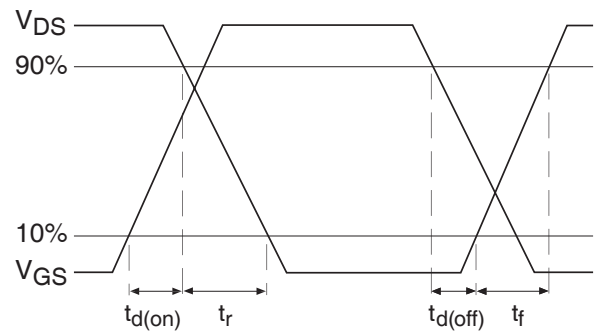
Fig 23b. Switching Time Waveforms

Current Regulator
Same Type as D.U.T.

12V .2µF 50KΩ .3µF

D.U.T.

V_{GS}

3mA

I_G I_D

Current Sampling Resistors

V_{DS}
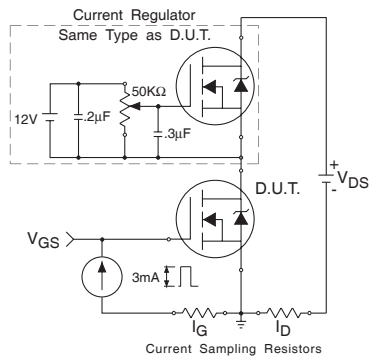
Fig 24a. Gate Charge Test Circuit

Id

Vds

Vgs

Vgs(th)

Qgs1 Qgs2 Qgd Qgodr

Fig 24b. Gate Charge Waveform
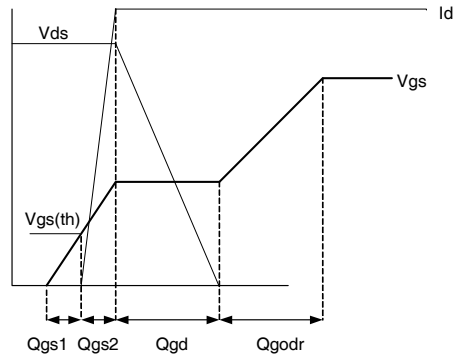
D^{2}Pak - 7 Pin Package Outline
Dimensions are shown in millimeters (inches)

THIRD ANGLE PROJECTION
IF IN DOUBT-ASK

10.35
10.15

A

8

15.3
14.5

1.8
1.25

1 2 3 4 5 6 7

SEE VIEW F

1.27 X4
TYP.

6X
0.75
0.65

⊕ 0.2|0.008|M|B|A|M

1.4
1.2

B

10°

2° TYP.

2° TYP.

0.55
0.35

1.4
1.15
2.75
2.25

VIEW F

7.15
6.85

5.25
4.75

8.9 REF

6°±0.5°
2 PLACES

R0.7
R0.5

4.55
4.35

10.5
10.3

0.25
0

0.25
0

3°MAX

8°MAX

Lead Assignment

1 - Gate
2 - Source
3 - Source
4 - Drain
5 - Source
6 - Source
7 - Source
8 - Drain

RECOMMENDED FOOTPRINT

10.8

8.15

16.3

2.54

3.2

0.9x4

1.27x2
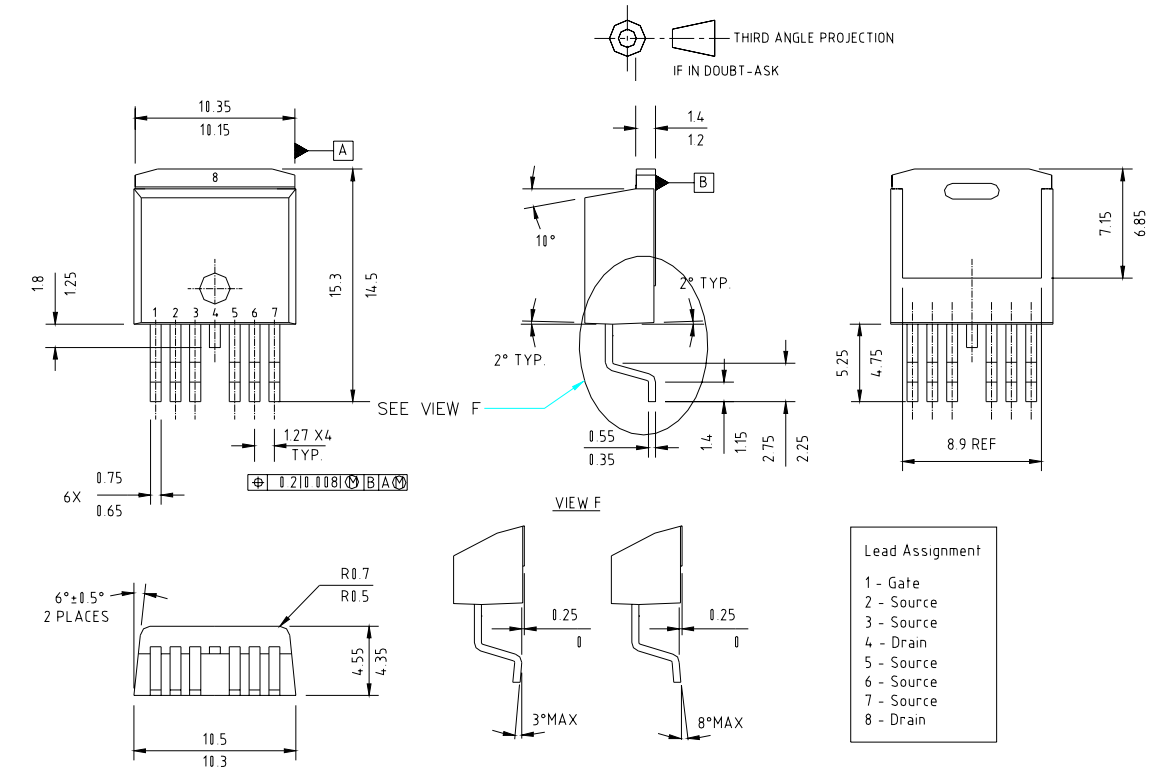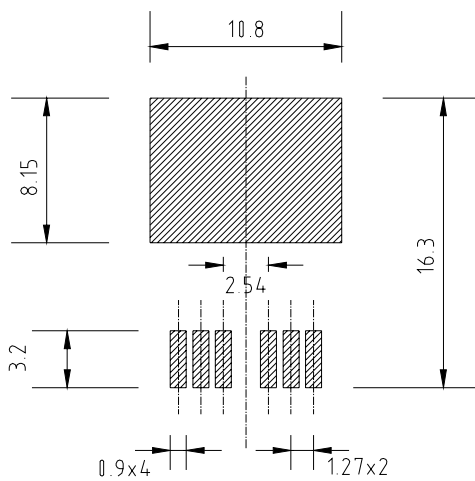
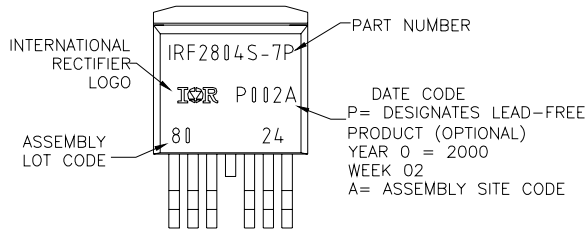| REV	DATE	MODIFICATION
-	18/03/03	RAISED IAW ECN 3426
Rev1	07/04/03	CHANGED IAW ECN 3438
A	23/04/04	ADD LEAD ASSIGNMENT

D²Pak - 7 Pin Part Marking Information

EXAMPLE: THIS IS AN IRF2804S-7P WITH
LOT CODE 8024
ASSEMBLED ON WW02,2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead Free"

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

IRF2804S-7P

I◯R 002L

ASSEMBLY
LOT CODE

80   24

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

OR

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

IRF2804S-7P

I◯R P002A

ASSEMBLY
LOT CODE

80   24

DATE CODE
P= DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 0 = 2000
WEEK 02
A= ASSEMBLY SITE CODE
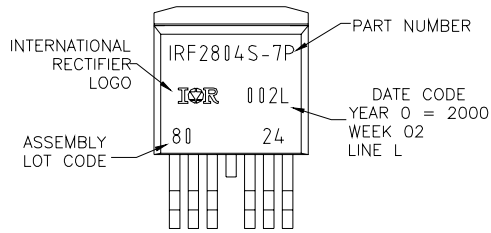
D²Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
   1.1 REEL SIZE 13 INCH DIAMETER.
   1.2 EACH REEL CONTAINING 800 DEVICES.
   1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS
       CONTAINED IN THE LEADER AND A MINIMUM OF 15
       SEALED POCKETS IN THE TRAILER.
   1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO.
       71-9667.
   1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
   1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE
       LOT CODE/DATE CODE COMBINATIONS.
       REWORKED REELS MAY CONTAIN A MAXIMUM OF
       THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS.
       HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR
       RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR
       CODE LABEL FOR THE AFFECTED REEL.
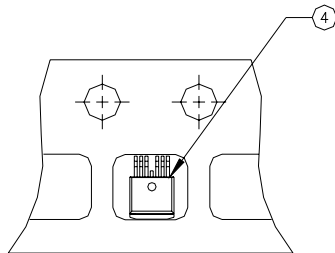
2. LABELLING (REEL AND SHIPPING BAG).
   2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
   2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
   2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
   2.4 QUANTITY:
   2.5 VENDOR CODE: IR
   2.6 LOT CODE:
   2.7 DATE CODE:

LABEL
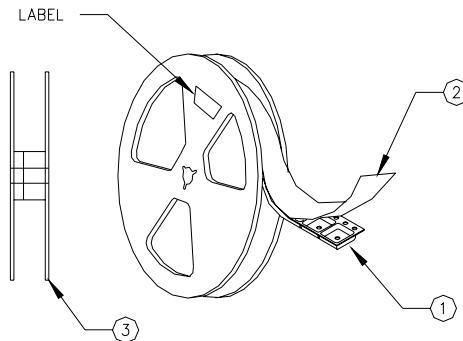
Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International I◯R Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 02/09