International
IOR Rectifier

IR3503

DATA SHEET

XPHASE3™ CONTROL IC

DESCRIPTION

The IR3503 control IC combined with an *XPHASE3*™ Phase IC provides a full featured and flexible way to implement a complete VR11.0 and VR11.1 power solution. The IR3503 provides overall system control and interfaces with any number of Phase ICs, each driving and monitoring a single phase. The X*Phase3*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

FEATURES

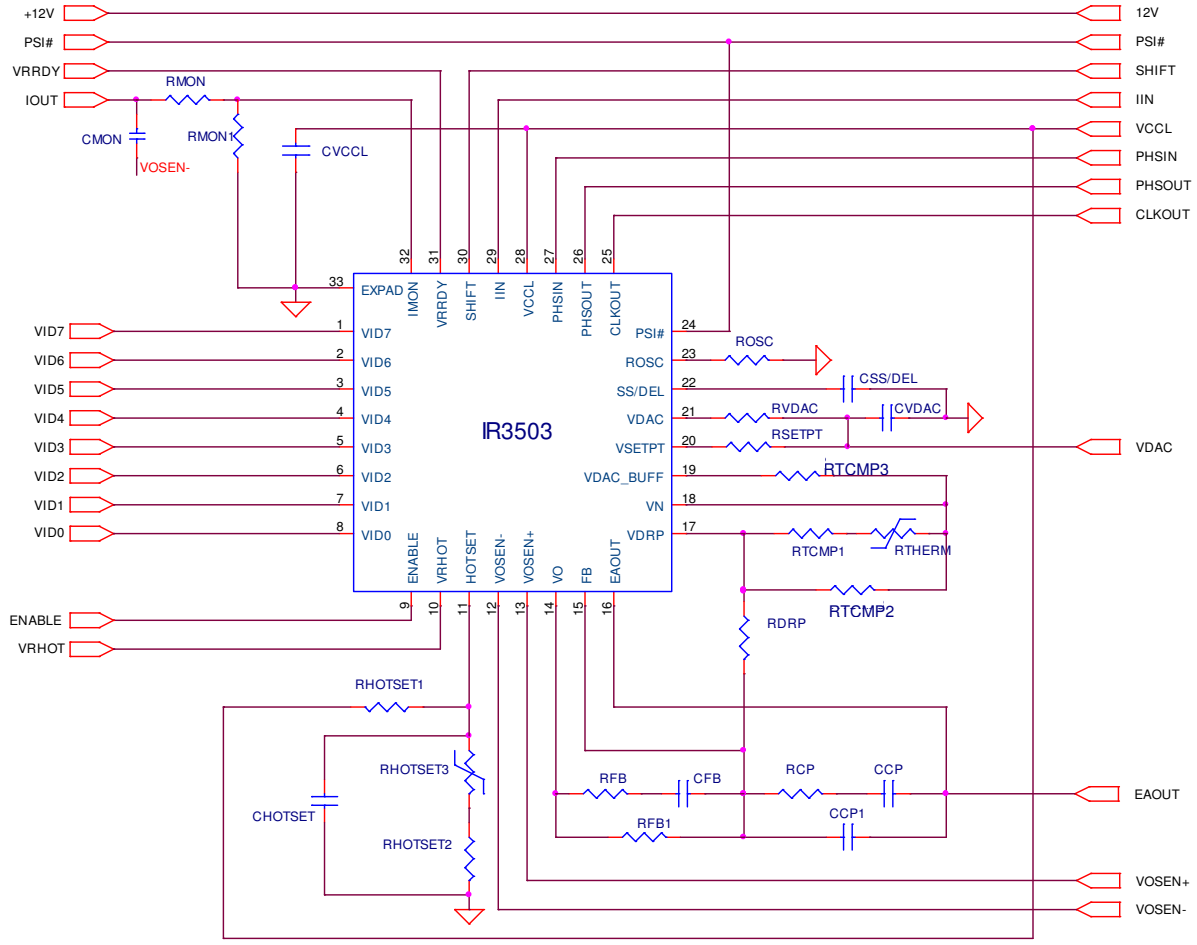
- 1 to X phase operation with matching Phase IC
- 0.5% overall system set point accuracy
- Daisy-chain digital phase timing provides accurate phase interleaving without external components
- Programmable 250kHz to 9MHz clock oscillator frequency provides per phase switching frequency of 250kHz to 1.5MHz
- Programmable Dynamic VID Slew Rate
- Programmable VID Offset or No Offset
- Programmable Load Line Output Impedance
- High speed error amplifier with wide bandwidth of 30MHz and fast slew rate of 10V/us
- Programmable constant converter output current limit during soft start
- Hiccup over current protection with delay during normal operation
- Central over voltage detection and latch with programmable threshold and communication to phase ICs
- Over voltage signal output to system with overvoltage detection during powerup and normal operation
- Load current reporting capable of interfacing directly to the CPU
- Single NTC thermistor compensation for correct current reporting, OC Threshold, and Droop
- Detection and protection of open remote sense line
- Open control loop protection
- Programmable VRHOT function monitors temperature of power stage through a NTC thermistor
- Remote sense amplifier with true converter voltage sensing
- Simplified VR Ready (VRRDY) output provides indication of proper operation
- Small thermally enhanced 32L 5mm x 5mm MLPQ package
- RoHS Compliant

ORDERING INFORMATION

Device	Package	Order Quantity
IR3503MTRPBF	32 Lead MLPQ (5 x 5 mm body)	3000 per reel
* IR3503MPBF	32 Lead MLPQ (5 x 5 mm body)	100 piece strips

- Samples only

APPLICATION CIRCUIT



Note: Pin 33 of IR3503 is the exposed pad located under the IC. It is connected to IC ground

Figure 1: IR3503 Application Circuit

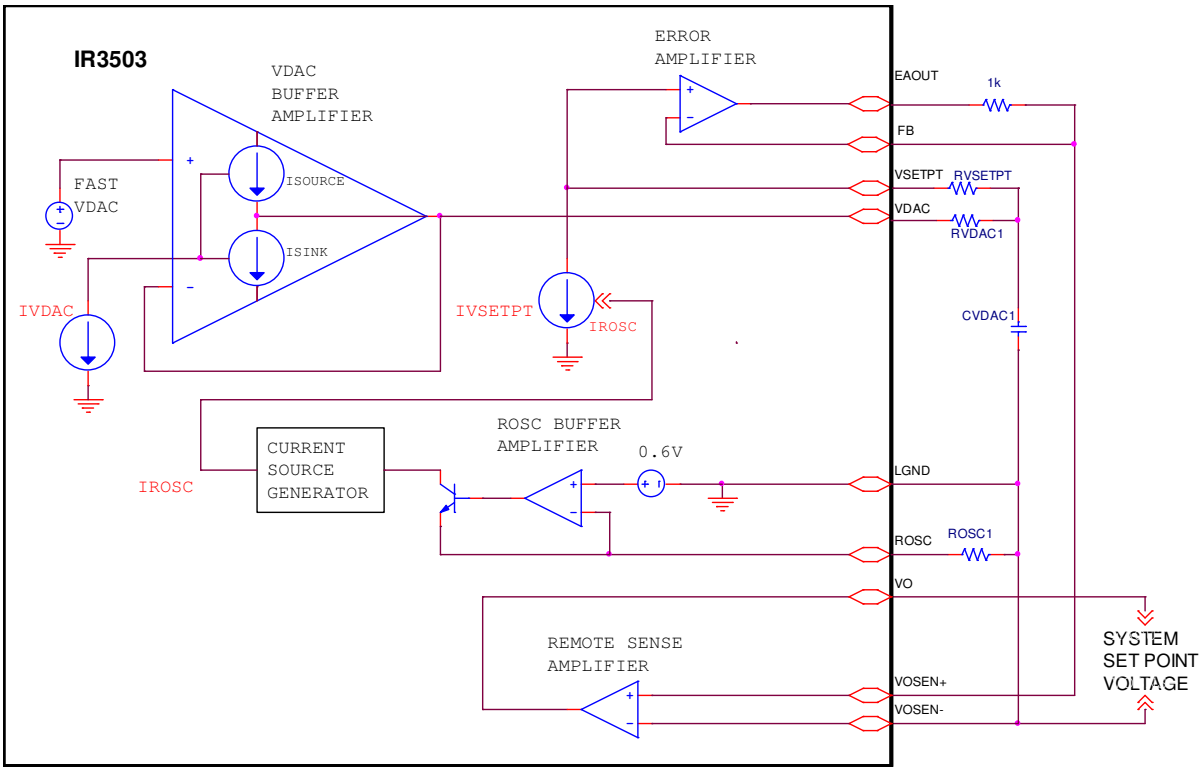


Figure 2: System set-point measurements

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Operating Junction Temperature……..0 to 150°C
Storage Temperature Range…….-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC Standard
MSL Rating……2
Reflow Temperature…….260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1-8	VID7-0	7.5V	-0.3V	1mA	1mA
9	ENABLE	3.5V	-0.3V	1mA	1mA
10	VRHOT	7.5V	-0.3V	1mA	50mA
11	HOTSET	7.5V	-0.3V	1mA	1mA
12	VOSEN-	1.0V	-0.5V	5mA	1mA
13	VOSEN+	7.5V	-0.5V	5mA	1mA
14	VO	7.5V	-0.5V	35mA	5mA
15	FB	7.5V	-0.3V	1mA	1mA
16	EAOUT	7.5V	-0.3V	35mA	5mA
17	VDRP	7.5V	-0.3V	35mA	1mA
18	VN	7.5V	-0.3V	1mA	1mA
19	VDAC_BUFF	3.5V	-0.3V	1mA	35mA
20	VSETPT	3.5V	-0.3V	1mA	1mA
21	VDAC	3.5V	-0.3V	1mA	1mA
22	SS/DEL	7.5V	-0.3V	1mA	1mA
23	ROSC	7.5V	-0.5V	1mA	1mA
24	PSI#	7.5V	-0.3V	1mA	1mA
25	CLKOUT	7.5V	-0.3V	100mA	100mA
26	PHSOUT	7.5V	-0.3V	10mA	10mA
27	PHSIN	7.5V	-0.3V	1mA	1mA
28	VCCL	7.5V	-0.3V	1mA	20mA
29	IIN	7.5V	-0.3V	1mA	1mA
30	SHIFT	7.5V	-0.3V	1mA	1mA
31	VRRDY	VCCL + 0.3V	-0.3V	1mA	20mA
32	IMON	3.5V	-0.3V	25mA	1mA
33	EXPAD	n/a	n/a	50mA	1mA

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 4.75 V<VCCL<7.5 V, -0.3 V ≤ VOSEN- ≤ 0.3 V, 0 °C ≤ T_J ≤ 100 °C, 7.75 kΩ ≤ R_{OSC} ≤ 50.0 kΩ, $C_{SS/DEL}$ = 0.1µF +/-10%.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDAC Reference					
System Set-Point Accuracy	VID ≥ 1V	-0.5		0.5	%
	0.8V ≤ VID < 1V	-5		+5	mV
	0.5V ≤ VID < 0.8V	-8		+8	mV
Source & Sink Currents	Include VSETPT current	30	44	58	µA
VIDx Operating Voltage		3	3.3	3.6	V
VIDx Input Threshold		500	600	700	mV
VIDx Input Bias Current	0V≤V(VIDx)≤2.5V.	-1	0	1	µA
VIDx OFF State Blanking Delay	Measure time till VRRDY drives low	0.5	1.3	2.1	µs
Oscillator					
ROSC Voltage		0.575	0.6	0.625	V
CLKOUT High Voltage	I(CLKOUT)= -10 mA, measure V(VCCL) – V(CLKOUT).			1	V
CLKOUT Low Voltage	I(CLKOUT)= 10 mA			1	V
PHSOUT Frequency	R_{OSC} = 50.0 KΩ	225	250	275	kHz
PHSOUT Frequency	R_{OSC} = 24.5 KΩ	450	500	550	kHz
PHSOUT Frequency	R_{OSC} = 7.75 KΩ	1.35	1.50	1.65	MHz
PHSOUT High Voltage	I(PHSOUT)= -1 mA, measure V(VCCL) – V(PHSOUT)			1	V
PHSOUT Low Voltage	I(PHSOUT)= 1 mA			1	V
SHIFT High Threshold	Percentage of VCCL	74	75	82	%
SHIFT Low Threshold	Percentage of VCCL	18	25	26	%
SHIFT Float Voltage	Percentage of (VCCL-LGND)/2	40	50	60	%
SHIFT Resistance to rails		10	30	50	kΩ
VDAC Buffer Amplifier					
Input Offset Voltage	V(VDAC_BUFF) – V(VDAC), 0.5V ≤ V(VDAC) ≤ 1.6V, < 1mA load	-5	0	9	mV
Source Current	0.5V ≤ V(VDAC) ≤ 1.6V	0.3	0.44	0.6	mA
Sink Current	0.5V ≤ V(VDAC) ≤ 1.6V	3.25	13	20	mA
Thermal Compensation Amplifier					
Output Offset Voltage	0V ≤ V(IIN) – V(VDAC) ≤ 1.6V, 0.5V ≤ V(VDAC) ≤ 1.6V, Req/R2 = 2	-10	0	10	mV
Source Current	0.5V ≤ V(VDAC) ≤ 1.6V	3	8	15	mA
Sink Current	0.5V ≤ V(VDAC) ≤ 1.6V	0.295	0.4	0.5	mA
Current Report Amplifier					
Output Offset Voltage	V(VDRP)–V(VDAC)=50,225,450,900mV	-15	0	15	mV
Source Current	0.5V ≤ V(IMON) ≤ 0.9V	5	9	15	mA
Sink Resistance	0.5V ≤ V(IMON) ≤ 0.9V	5	10	17	kΩ
Input Filter Time Constant			1		µs
Max Output Voltage		1.04	1.09	1.145	V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft Start and Delay					
Start Delay (TD1)		1.0	2.9	3.5	ms
Soft Start Time (TD2)		0.8	2.2	3.35	ms
VID Sample Delay (TD3)		0.3	1.2	3.0	ms
VRRDY Delay (TD4 + TD5)		0.5	1.2	2.3	ms
OC Delay Time	V(VDRP) – V(DACBUFF) = 1.67 mV (OC Delay post power-up)	75	125	300	us
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.7	1.4	1.9	V
Charge/Discharge Current Ratio		10	12	16	µA/µA
Charge Voltage		3.6	4.0	4.2	V
Remote Sense Differential Amplifier					
Input Offset Voltage	0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.6V	-3	0	3	mV
Sink Current	0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.6V	0.4	1	2	mA
Source Current	0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.6V	2.5	9	20	mA
VOSEN+ Bias Current	0.5 V < V(VOSEN+) < 1.6V			100	µA
VOSEN- Bias Current	-0.3V ≤ VOSEN- ≤ 0.3V, All VID Codes		160	285	µA
High Voltage	V(VCCL) – V(VO)	1.5	2	2.5	V
Low Voltage	V(VCCL)=7V			50	mV
Error Amplifier					
Input Offset Voltage	Measure V(FB) – V(VSETPT). Note 2		0		mV
FB Bias Current		-1	0	1	µA
VSETPT Bias Current	ROSC= 24.5 KΩ	23.00	24.25	25.50	µA
DC Gain	Note 1	100	110	120	dB
Bandwidth	Note 1	20	30	40	MHz
Sink Current		0.40	0.85	1.00	mA
Source Current		5	8	12	mA
Open Voltage Loop Detection Threshold	Measure V(VCCL) - V(EAOUT), Relative to Error Amplifier maximum voltage.	125	300	600	mV
Open Voltage Loop Detection Delay	Measure PHSOUT pulse numbers from V(EAOUT) = V(VCCL) to VRRDY = low.		8		Pulses
Enable Input					
VR 11 Threshold Voltage	ENABLE rising	825	850	875	mV
VR 11 Threshold Voltage	ENABLE falling	775	800	825	mV
VR 11 Hysteresis		25	50	75	mV
Bias Current	0V ≤ V(ENABLE) ≤ 3.3V	-5	0	5	µA
Blanking Time	Noise Pulse < 100ns will not register an ENABLE state change. Note 1	75	250	400	ns
PSI# Comparator					
Resistance		37	100	170	kΩ
Floating Voltage		800		1150	mV
Over-Current Comparator					
Over-Current Threshold	Maximum phases, VDRP-VDAC_BUFF	1.045	1.17	1.295	V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Reduced Phase OC Threshold: Total number of phases ≤ 15	$\left(1.17 * \frac{Actual\_number\_of\_phases}{Total\_number\_of\_phases}\right)$; 3 ≤ Actual number of phases ≤ 15	-8.5%		+8.5%	mV
	$\left(1.17 * \frac{Actual\_number\_of\_phases}{Total\_number\_of\_phases}\right)$; Actual number of phases ≤ 2	-20 %		+20%	mV
Over-Current Delay Counter	ROSC = 7.75 KΩ (PHSOUT=1.5MHz)		4096		Cycle
Over-Current Delay Counter	ROSC = 15.0 KΩ (PHSOUT=800kHz)		2048		Cycle
Over-Current Delay Counter	ROSC = 50.0 KΩ (PHSOUT=250kHz)		1024		Cycle
Over Voltage Protection (OVP) Comparators					
Rising Threshold	Compare to V(VDAC)	105	125	145	mV
OVP Release Voltage	Compare to V(VDAC)	-13	3	20	mV
Threshold during Dynamic VID down		1.70	1.73	1.75	V
Dynamic VID Detect Comparator Threshold		25	50	75	mV
VRRDY Output					
Output Voltage	I(VRRDY) = 4mA		150	300	mV
Leakage Current	V(VRRDY) = 5.5V		0	10	µA
Under Voltage Threshold-VO decreasing	Reference to VDAC	-360	-305	-250	mV
Under Voltage Threshold-VO increasing	Reference to VDAC	-290	-240	-190	mV
Under Voltage Threshold Hysteresis		25	60	95	mV
Open Sense Line Detection					
Sense Line Detection Source Currents	V(VO) = 100mV	200	500	700	µA
VRHOT Comparator					
Threshold Voltage		1.584	1.600	1.616	V
HOTSET Bias Current		-1	0	1	µA
Hysteresis		75	100	125	mV
Output Voltage	I(VRHOT) = 30mA		150	400	mV
VRHOT Leakage Current	V(VRHOT) = 5.5V		0	10	µA
VCCL Monitor					
UVLO Start Threshold		4.29	4.5	4.72	V
UVLO Stop Threshold		3.85	4	4.25	V
Hysteresis		0.41	0.455	0.5	V
General					
VCCL Supply Current		4	8	12	mA

Note 1: Guaranteed by design, but not tested in production
Note 2: VDAC Output is trimmed to compensate for Error Amplifier input offsets errors

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1-8	VID7-0	Inputs to VID D to A Converter.
9	ENABLE	Enable input. A logic low applied to this pin puts the IC into fault mode. Do not float this pin as the logic state will be undefined.
10	VRHOT	Open collector output of the VRHOT comparator which drives low if HOTSET pin voltage is lower than 1.6V. Connect external pull-up.
11	HOTSET	A resistor divider including thermistor senses the temperature, which is used for VRHOT comparator.
12	VOSEN-	Remote sense amplifier input. Connect to ground at the load.
13	VOSEN+	Remote sense amplifier input. Connect to output at the load.
14	VO	Remote sense amplifier output.
15	FB	Inverting input to the Error Amplifier.
16	EAOUT	Output of the error amplifier.
17	VDRP	Buffered, scaled and thermally compensated IIN signal. Connect an external RC network to FB to program converter output impedance.
18	VN	Node for DCR thermal compensation network.
19	VDAC_BUFF	Buffered VDAC.
20	VSETPT	Error amplifier non-inverting input. Converter output voltage can be decreased from the VDAC voltage with an external resistor connected between VDAC and this pin (there is an internal sink current at this pin).
21	VDAC	Regulated voltage programmed by the VID inputs. Connect an external RC network to LGND to program dynamic VID slew rate and provide compensation for the internal buffer amplifier.
22	SS/DEL	Programs converter startup and over current protection delay timing. It is also used to compensate the constant output current loop during soft start. Connect an external capacitor to LGND to program.
23	ROSC	Connect a resistor to LGND to program oscillator frequency and OCSET, VSETPT and VDAC bias currents. Oscillator frequency equals switching frequency per phase. The pin voltage is 0.6V during normal operation.
24	PSI#	Digital Power State Indicator input, active low.
25	CLKOUT	Clock output at switching frequency multiplied by phase number. Connect to CLKIN pins of phase ICs.
26	PHSOUT	Phase clock output at switching frequency. Connect to PHSIN pin of first phase IC.
27	PHSIN	Feedback input of phase clock. Connect to PHSOUT pin of the last phase IC.
28	VCCL	Voltage regulator and IC power input. Connect a decoupling capacitor to LGND.
29	IIN	Average current input from the phase IC(s). This pin is also used to communicate over voltage condition to phase ICs.
30	SHIFT	Communication input from phase IC(s) statically floats at VCCL/2. Momentarily pulling pin up to VCCL indicates a phase has entered the daisy chain loop resulting in an up-shift in the CLKOUT frequency. Momentarily pulling down to ground indicates a loss of a phase and down-shifts the CLKOUT frequency.
31	VRRDY	Open collector output that drives low during startup and under any external fault condition. Indicates converter within regulation. Connect external pull-up.
32	IMON	Voltage at IOUT pin will be proportional to load current.
33	EXPAD	Exposed pad located underneath the IC. Local Ground for internal circuitry and IC substrate connection.

SYSTEM THEORY OF OPERATION

Description:

The system consists of one control IC and scalable number of phase IC's depending upon the number of converter phases. The control IC communicates with the phase ICs using three digital buses, i.e., CLOCK, PHSIN, PHSOUT and three analog buses, i.e., VDAC, EA, IIN. The digital buses are responsible for switching frequency determination and accurate phase timing control without any external component. The analog buses are used for PWM control and current sharing among interleaved phases. The control IC incorporates all the system functions, i.e., VID, CLOCK signals, error amplifier, fault protections, current monitor, etc. The Phase IC implements the functions required by each phase of the converter, i.e., the gate drivers, PWM comparator and latch, over-voltage protection, Phase disable circuit, current sensing and sharing, etc. In addition to these functions, the control IC also implements PSI# (Power System Indicator) functionality to improve the efficiency of the voltage regulator at light loads.

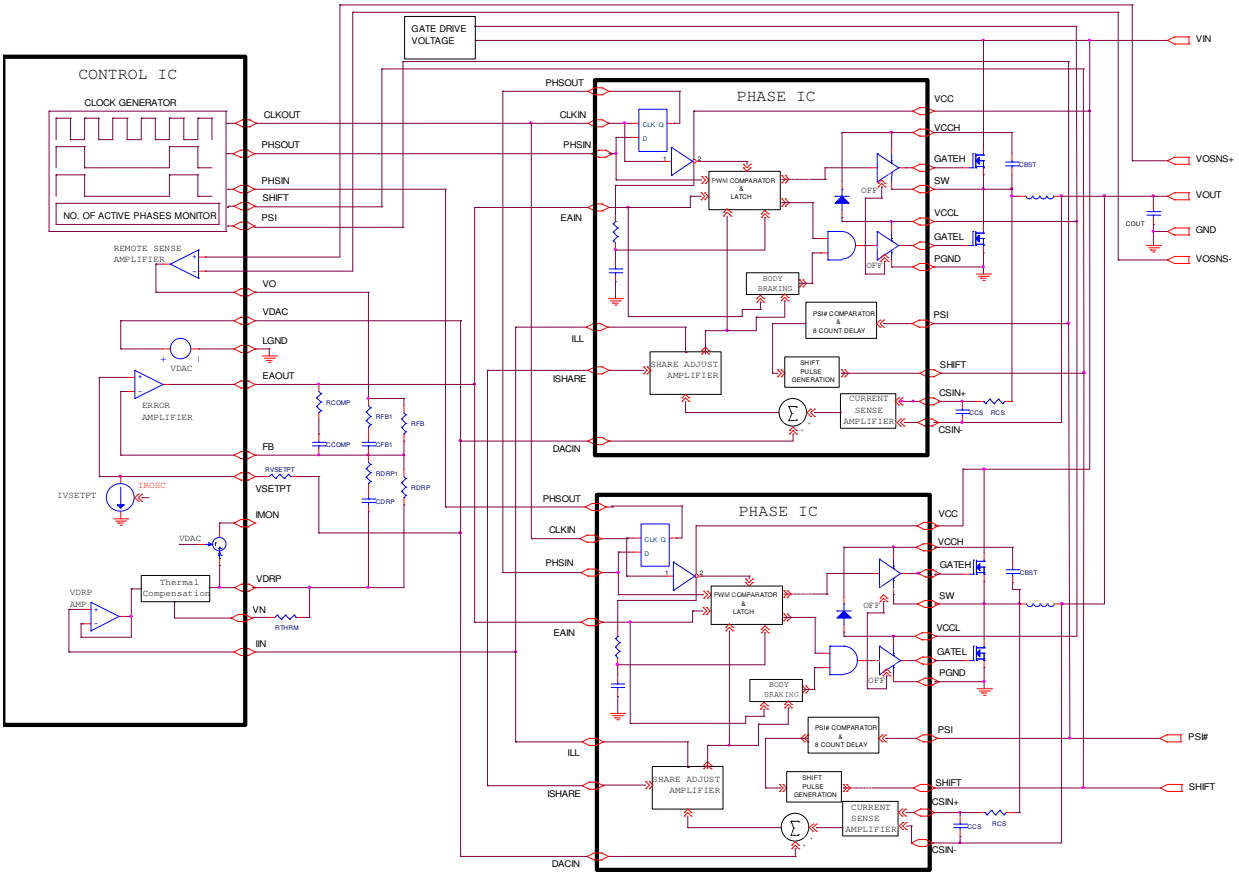
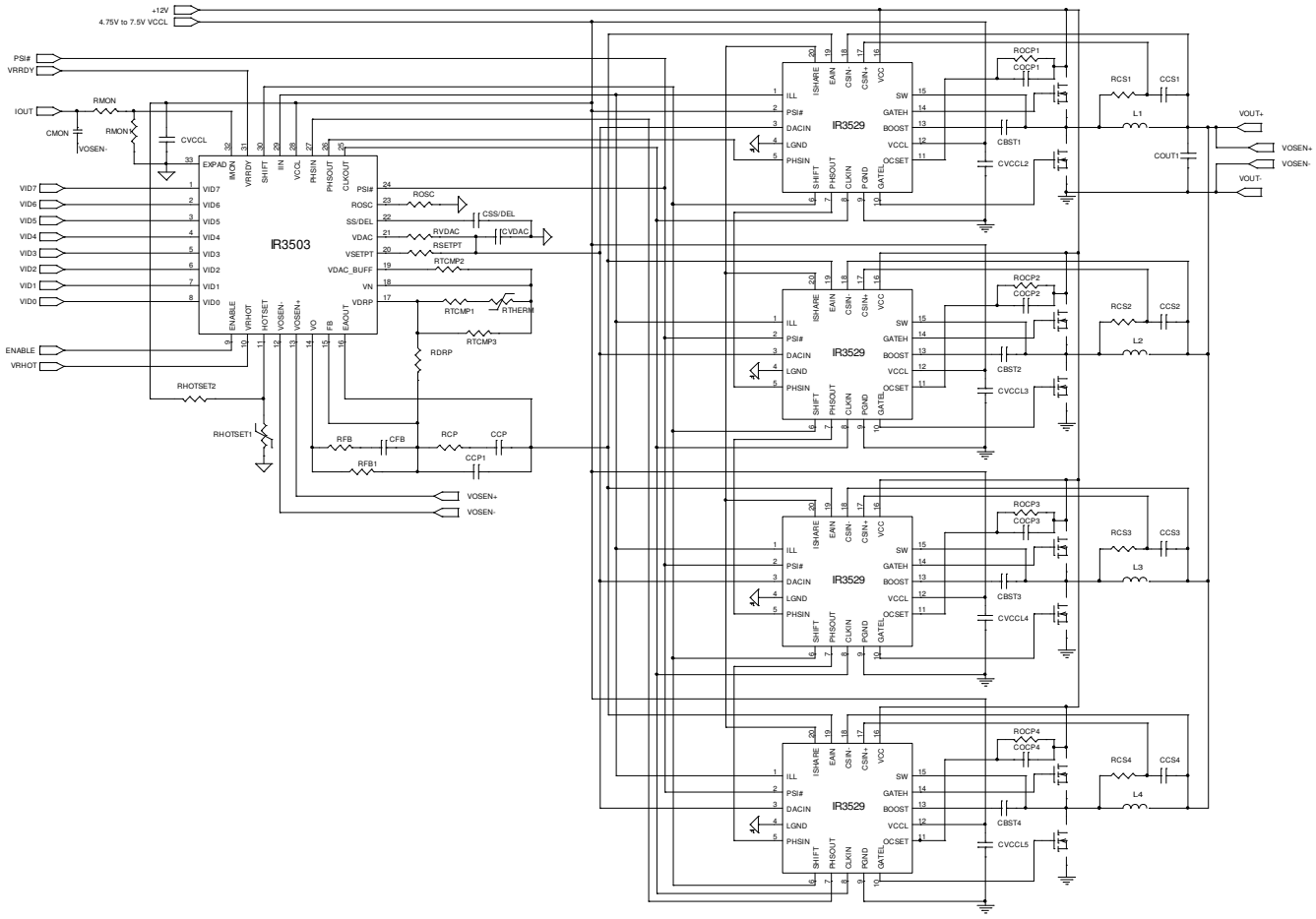


Figure 3: System Block Diagram

APPLICATION SYSTEM CIRCUIT



Note: Pin 33 of IR3503 is the exposed pad located under the IC. It is connected to IC ground

Figure 4: IR3503 Multiphase Application Circuit

PWM Control Method

The system block diagram of the *XPhase3*™ architecture is shown in Figure 3. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the control IC is used for the voltage control loop. Input voltage is sensed in phase ICs and feed-forward control is realized. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

Frequency and Phase Timing Control

The oscillator is located in the control IC and the system clock frequency is programmable from 250 kHz to 9 MHZ by an external resistor. The control IC system clock signal CLKOUT is connected to CLKIN of all the phase ICs. The phase timing of the phase ICs is controlled by the daisy chain loop, where control IC phase clock output PHSOUT is connected to the phase clock input PHSIN of the first phase IC, and PHSOUT of the first phase IC is connected to PHSIN of the second phase IC, etc. The PHSOUT of the last phase IC is connected back to PHSIN of the control IC.

During power up, the control IC sends out clock signals from both CLKOUT and PHSOUT pins and detects the feedback at PHSIN pin to determine the phase number and monitor any fault in the daisy chain loop. Figure 5 shows the phase timing for a four phase converter. The switching frequency is set by the resistor ROSC. The clock frequency equals the number of phase times the switching frequency.

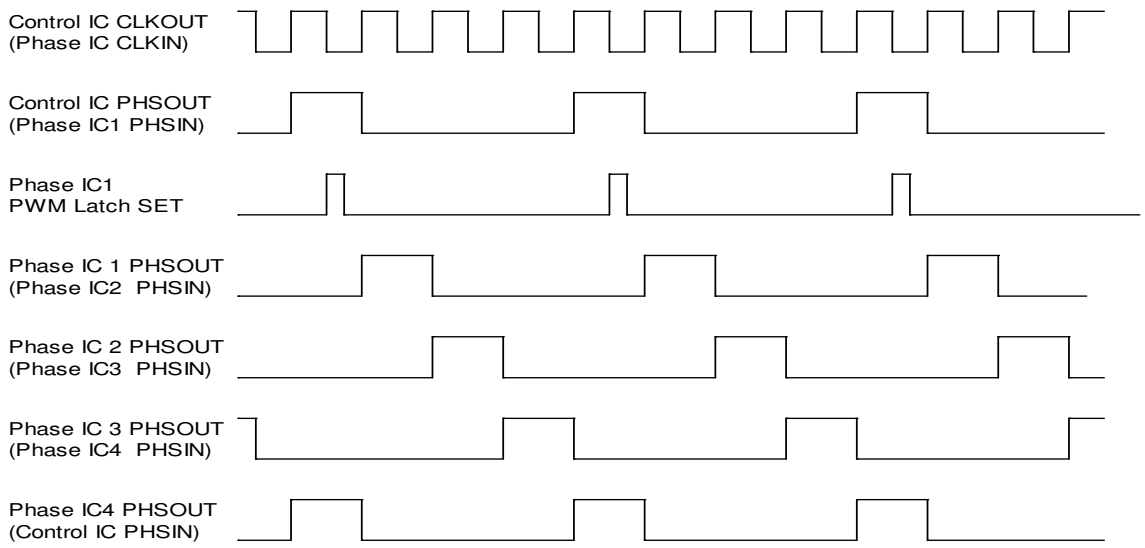


Figure 5: Four Phase Oscillator Waveforms

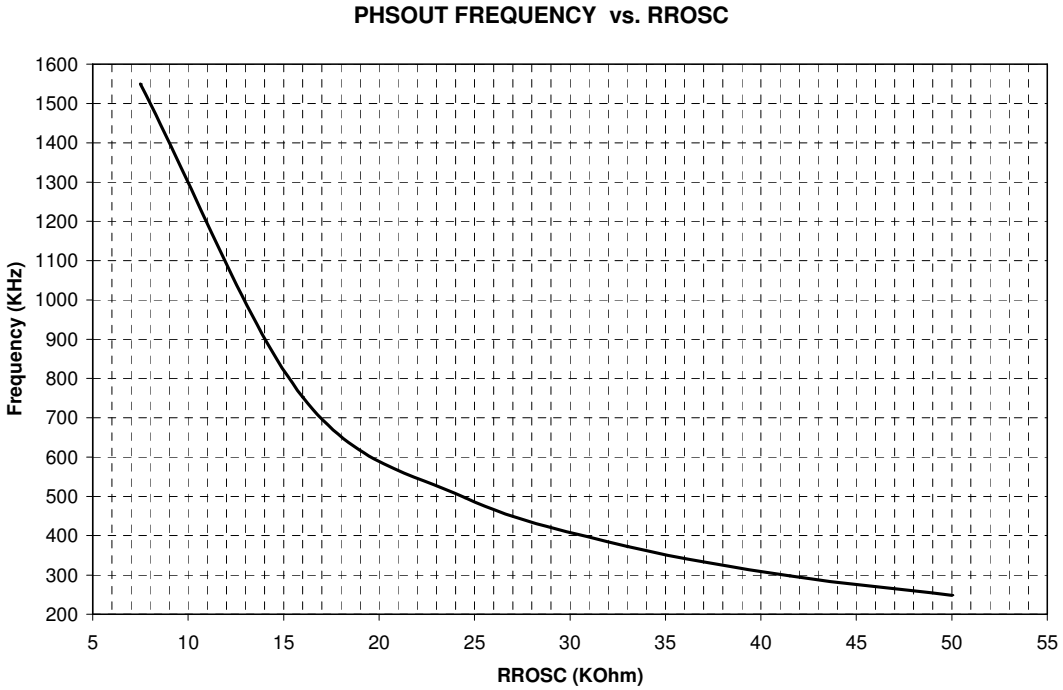


Figure 6: PHSOUT Frequency vs RROSC chart

PWM Operation

The PWM comparator is located in the phase IC. With the PHSIN voltage high, upon receiving the falling edge of a clock pulse, the PWM latch is set. The PWMRMP voltage begins to increase; the low side driver is turned off, and the high side driver is turned on after the non-overlap time. When the PWMRMP voltage exceeds the error amplifier's output voltage, the PWM latch is reset. This turns off the high side driver and then turns on the low side driver after the non-overlap time. Along with that, it activates the ramp discharge clamp, which quickly discharges the PWMRMP capacitor to the output voltage of share adjust amplifier in phase IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go up to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate, given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients. The error amplifier is a high speed amplifier with wide bandwidth and fast slew rate incorporated in the control IC. It is not unity gain stable.

This control method is designed to provide "single cycle transient response," where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage of the architecture is that differences in the ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC. Figure 6 depicts PWM operating waveforms under various conditions.

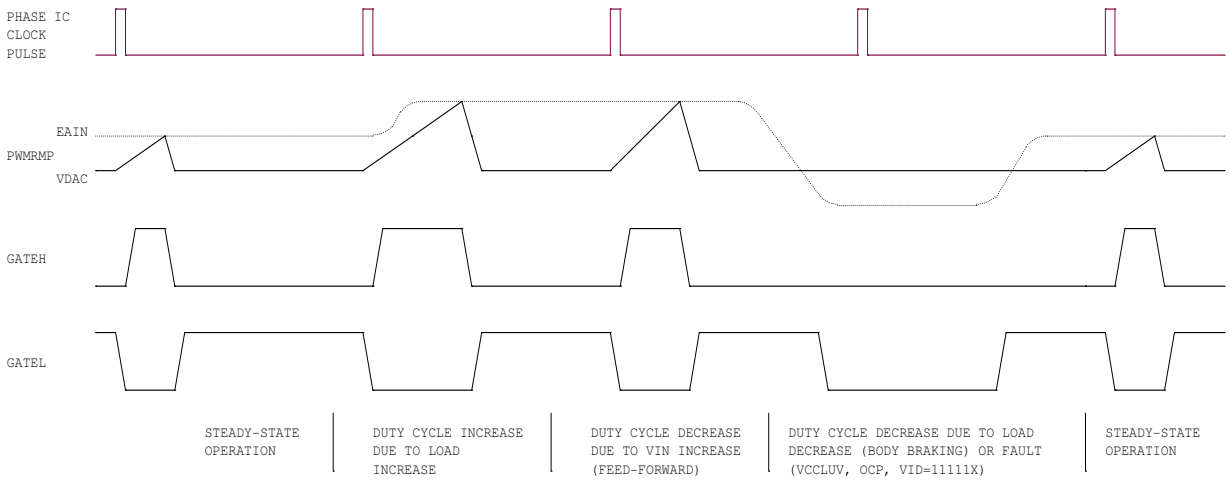


Figure 7: PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often comparable to the output voltage, the inductor current slew rate can be increased significantly. This patented technique is referred to as “body braking” and is accomplished through the “body braking comparator” located in the phase IC. If the error amplifier’s output voltage drops below the output voltage of the share adjust amplifier in the phase IC, this comparator turns off the low side gate driver, enabling the bottom FET body diode to take over. There is 100mV upslope and 200mV down slope hysteresis for the body braking comparator.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 7. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L + sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen, such that, the time constant of Rcs and Ccs equals the time constant of the inductor, which is the inductance L over the inductor DCR RL. If the two time constants match, the voltage across Ccs will be proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of RL was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

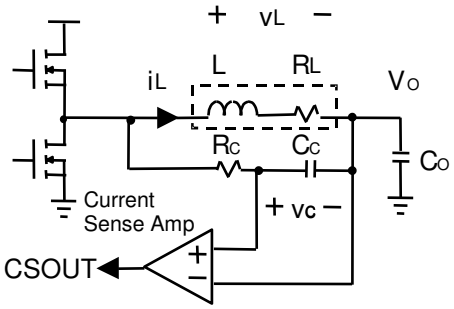


Figure 8: Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM propagation delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the phase IC, as shown in Figure 7. Its gain is nominally 33 at 25ºC, and the 3850 ppm/ºC increase in inductor DCR should be compensated in the voltage loop feedback path.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the VDAC voltage and sent to the control IC and other phases through an on-chip 3 kΩ resistor connected to the IIN pin. The IIN pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the control IC for voltage positioning and current limit protection. The input offset of this amplifier is calibrated to +/- 1mV in order to reduce the current sense error.

The input offset voltage is the primary source of error for the current share loop. In order to achieve very small input offset error and superior current sharing performance, the current sense amplifier continuously calibrates itself. This 21calibration algorithm creates ripple on IIN bus with a frequency of $\frac{f_{SW}}{32*28}$ in a multiphase architecture.

Average Current Share Loop

Current sharing between the phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated; such that, the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

IR3503 THEORY OF OPERATION

Block Diagram

The block diagram of the IR3503 is shown in figure 10.

VID Control

The control IC allows the processor voltage to be set by a parallel eight bit digital VID bus. The VID codes set the VDAC as shown in Table 1. The VID pins require an external bias voltage and should not be floated. The VID input comparators monitor the VID pins and control the Digital-to-Analog Converter (DAC), whose output is sent to the VDAC buffer amplifier. The output of the buffer amplifier is the VDAC pin. The VDAC voltage, input offsets of error amplifier and remote sense differential amplifier are post-package trimmed to achieve 0.5 % system set-point accuracy for VID range between 1 V to 1.6 V. A set-point accuracy of ± 5 mV and ± 8 mV is achieved for VID ranges of 0.8 V-1 V and 0.5 V-0.8 V respectively. The actual VDAC voltage does not determine the system accuracy, which has a wider tolerance.

The IR3503 can accept changes in the VID code while operating and vary the VDAC voltage accordingly. The slew rate of the voltage at the VDAC pin can be adjusted by an external capacitor between VDAC pin and LGND pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifier. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

Adaptive Voltage Positioning (AVP)

Adaptive voltage positioning is needed to optimize the output voltage excursions during dynamic load variations. The objective of AVP is to control the output voltage to a value that is slightly higher than the minimum value at full load and slightly lower than the maximum permissible limit at light load. Thus, AVP also helps to reduce the output power at full load and is essential to meet the load line specifications. The circuitry related to voltage positioning is shown in Figure 9. The output voltage is set by the reference voltage VSETPT at the positive input to the error amplifier. This reference voltage can be programmed to have a constant DC offset below the VDAC by connecting RSETPT between VDAC and VSETPT. The IVSETPT is controlled by the resistor, ROSC.

The average load current information for all the phases is fed back to the control IC through the IIN pin. As shown in Figure 9, this information is thermally compensated with some gain by a set of buffer and thermal compensation amplifiers to generate the voltage at the VDRP pin. The VDRP pin is connected to the FB pin through the resistor RDRP. Since the error amplifier will force the loop to maintain FB to be equal to the VDAC reference voltage, an additional current will flow into the FB pin equal to (VDRP-VDAC) / RDRP. When the load current increases, the VDRP voltage increases accordingly. More current flows through the feedback resistor RFB and causes the output to have more droop. The resistor R_{DRP} produces the required droop in output voltage proportional to the load current.

$$\Delta V_{DRP} = i * R_{FB} = I_{OUT} \times R_{loadline}$$

$$i = \frac{V_{DRP} - V_{DAC}}{R_{DRP}}$$

The positioning voltage can be programmed by the resistor RDRP so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to and therefore independent of the VDAC voltage.

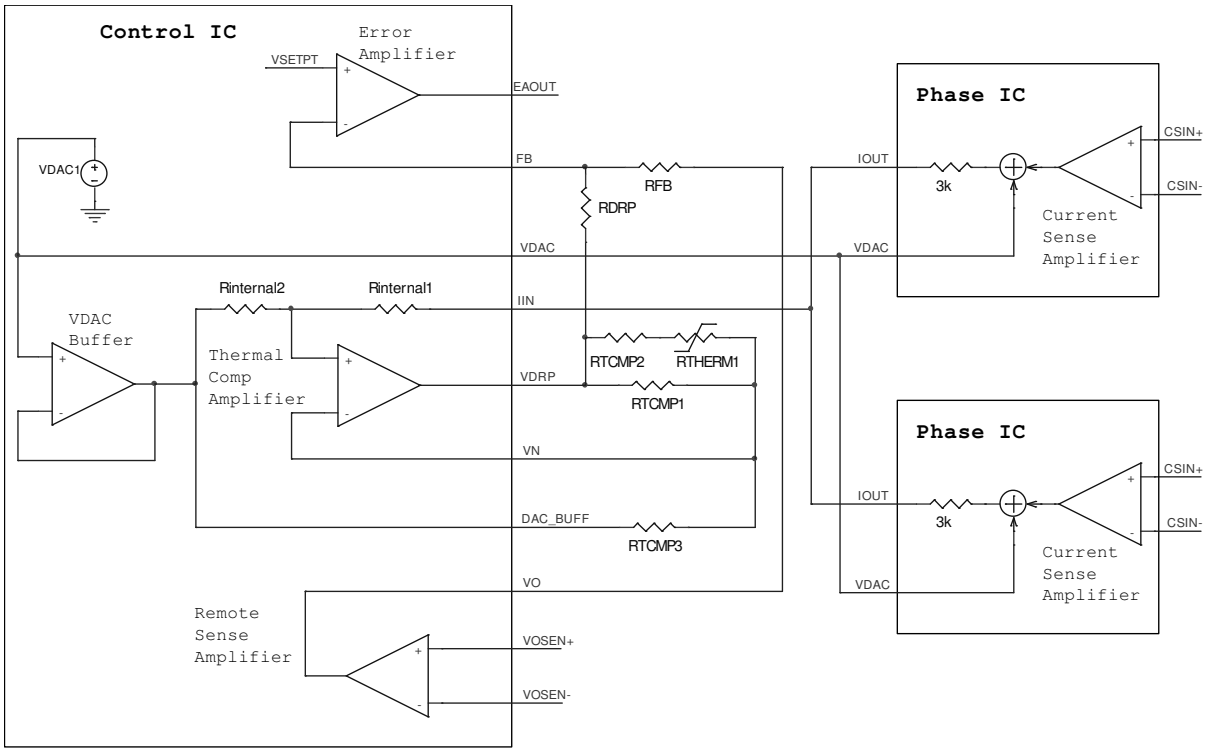


Figure 9: Adaptive Voltage Positioning (AVP) with Thermal Compensation

Inductor DCR Temperature Compensation

A negative temperature coefficient (NTC) thermistor should be used for inductor DCR temperature compensation. The thermistor and tuning resistor network connected between the VN and VDRP pins provides a single NTC thermal compensation. The thermistor should be placed close to the power stage to accurately reflect the thermal performance of the inductor DCR. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

Remote Voltage Sensing

VOSEN+ and VOSEN- are used for remote sensing and connected directly to the load. The remote sense differential amplifier with high speed, low input offset and low input bias current ensures accurate voltage sensing and fast transient response. There is finite input current at both pins VOSEN+ and VOSEN- due to the internal resistor of the differential amplifier. This limits the size of the resistors that can be used in series with these pins for acceptable regulation of the output voltage.

Block Diagram

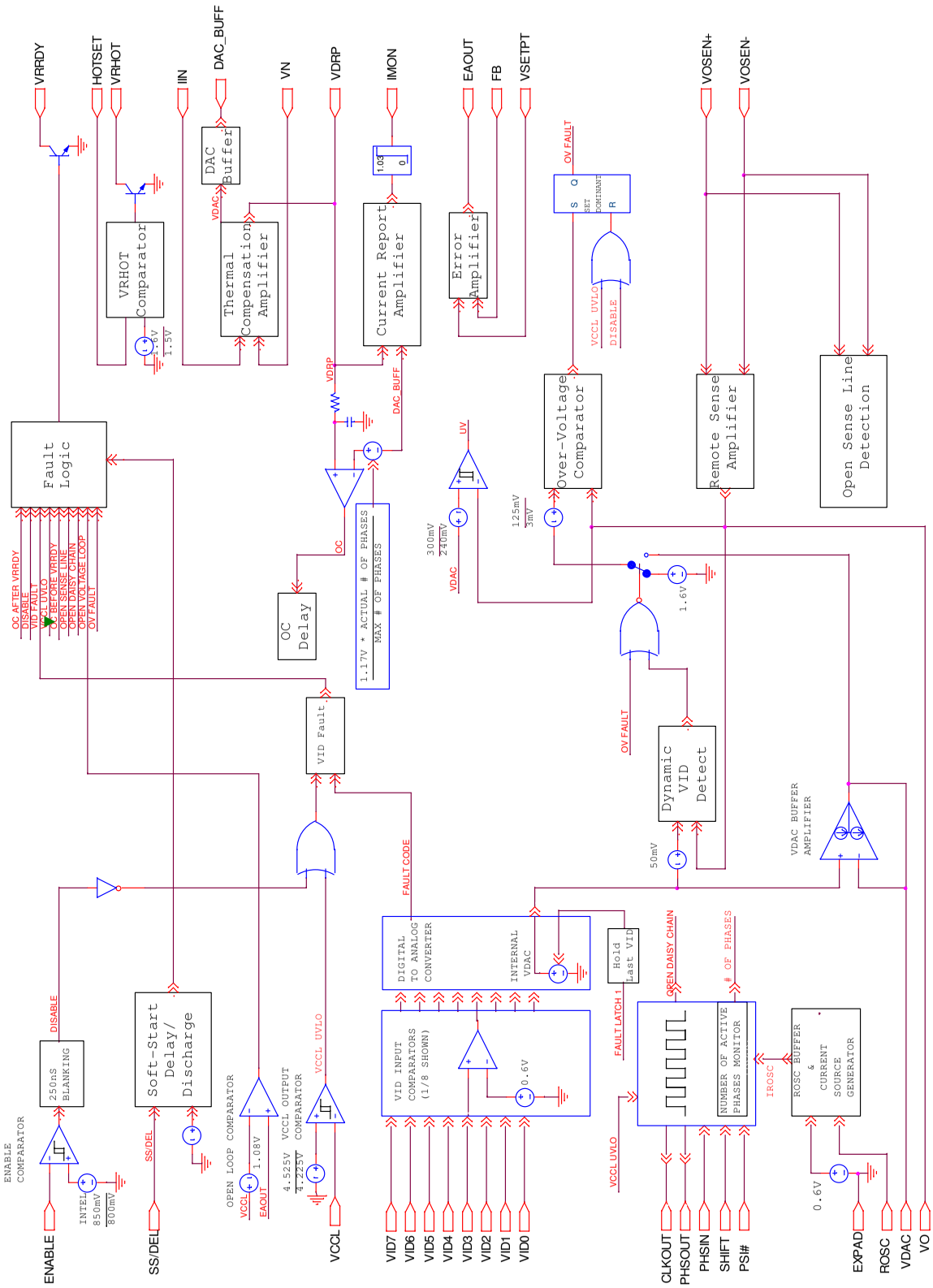


Figure 10: Block Diagram

TABLE 1: VR11 VID TABLE (PART1)

Hex (VID7:VID0)	Bin (VID7:VID0)	Voltage
00	00000000	Fault
01	00000001	Fault
02	00000010	1.60000
03	00000011	1.59375
04	00000100	1.58750
05	00000101	1.58125
06	00000110	1.57500
07	00000111	1.56875
08	00001000	1.56250
09	00001001	1.55625
0A	00001010	1.55000
0B	00001011	1.54375
0C	00001100	1.53750
0D	00001101	1.53125
0E	00001110	1.52500
0F	00001111	1.51875
10	00010000	1.51250
11	00010001	1.50625
12	00010010	1.50000
13	00010011	1.49375
14	00010100	1.48750
15	00010101	1.48125
16	00010110	1.47500
17	00010111	1.46875
18	00011000	1.46250
19	00011001	1.45625
1A	00011010	1.45000
1B	00011011	1.44375
1C	00011100	1.43750
1D	00011101	1.43125
1E	00011110	1.42500
1F	00011111	1.41875
20	00100000	1.41250
21	00100001	1.40625
22	00100010	1.40000
23	00100011	1.39375
24	00100100	1.38750
25	00100101	1.38125
26	00100110	1.37500
27	00100111	1.36875
28	00101000	1.36250
29	00101001	1.35625
2A	00101010	1.35000
3	00101011	1.34375
2C	00101100	1.33750
2D	00101101	1.33125
2E	00101110	1.32500
2F	00101111	1.31875
30	00110000	1.31250
31	00110001	1.30625
32	00110010	1.30000
33	00110011	1.29375
34	00110100	1.28750
35	00110101	1.28125
36	00110110	1.27500
37	00110111	1.26875
38	00111000	1.26250
39	00111001	1.25625
3A	00111010	1.25000
3B	00111011	1.24375
3C	00111100	1.23750
3D	00111101	1.23125
3E	00111110	1.22500
3F	00111111	1.21875

Hex (VID7:VID0)	Bin (VID7:VID0)	Voltage
40	01000000	1.21250
41	01000001	1.20625
42	01000010	1.20000
43	01000011	1.19375
44	01000100	1.18750
45	01000101	1.18125
46	01000110	1.17500
47	01000111	1.16875
48	01001000	1.16250
49	01001001	1.15625
4A	01001010	1.15000
4B	01001011	1.14375
4C	01001100	1.13750
4D	01001101	1.13125
4E	01001110	1.12500
4F	01001111	1.11875
50	01010000	1.11250
51	01010001	1.10625
52	01010010	1.10000
53	01010011	1.09375
54	01010100	1.08750
55	01010101	1.08125
56	01010110	1.07500
57	01010111	1.06875
58	01011000	1.06250
59	01011001	1.05625
5A	01011010	1.05000
5B	01011011	1.04375
5C	01011100	1.03750
5D	01011101	1.03125
5E	01011110	1.02500
5F	01011111	1.01875
60	01100000	1.01250
61	01100001	1.00625
62	01100010	1.00000
63	01100011	0.99375
64	01100100	0.98750
65	01100101	0.98125
66	01100110	0.97500
67	01100111	0.96875
68	01101000	0.96250
69	01101001	0.95625
6A	01101010	0.95000
6B	01101011	0.94375
6C	01101100	0.93750
6D	01101101	0.93125
6E	01101110	0.92500
6F	01101111	0.91875
70	01110000	0.91250
71	01110001	0.90625
72	01110010	0.90000
73	01110011	0.89375
74	01110100	0.88750
75	01110101	0.88125
76	01110110	0.87500
77	01110111	0.86875
78	01111000	0.86250
79	01111001	0.85625
7A	01111010	0.85000
7B	01111011	0.84375
7C	01111100	0.83750
7D	01111101	0.83125
7E	01111110	0.82500
7F	01111111	0.81875

TABLE 1: VR11 VID TABLE (PART 2)

Hex (VID7:VID0)	Bin (VID7:VID0)	Voltage
80	10000000	0.81250
81	10000001	0.80625
82	10000010	0.80000
83	10000011	0.79375
84	10000100	0.78750
85	10000101	0.78125
86	10000110	0.77500
87	10000111	0.76875
88	10001000	0.76250
89	10001001	0.75625
8A	10001010	0.75000
8B	10001011	0.74375
8C	10001100	0.73750
8D	10001101	0.73125
8E	10001110	0.72500
8F	10001111	0.71875
90	10010000	0.71250
91	10010001	0.70625
92	10010010	0.70000
93	10010011	0.69375
94	10010100	0.68750
95	10010101	0.68125
96	10010110	0.67500
97	10010111	0.66875
98	10011000	0.66250
99	10011001	0.65625
9A	10011010	0.65000
9B	10011011	0.64375
9C	10011100	0.63750
9D	10011101	0.63125
9E	10011110	0.62500
9F	10011111	0.61875
A0	10100000	0.61250
A1	10100001	0.60625
A2	10100010	0.60000
A3	10100011	0.59375
A4	10100100	0.58750
A5	10100101	0.58125
A6	10100110	0.57500
A7	10100111	0.56875
A8	10101000	0.56250
A9	10101001	0.55625
AA	10101010	0.55000
AB	10101011	0.54375
AC	10101100	0.53750
AD	10101101	0.53125
AE	10101110	0.52500
AF	10101111	0.51875
B0	10110000	0.51250
B1	10110001	0.50625
B2	10110010	0.50000
B3	10110011	n/a
B4	10110100	n/a
B5	10110101	n/a
B6	10110110	n/a
B7	10110111	n/a
B8	10111000	n/a
B9	10111001	n/a
BA	10111010	n/a
BB	10111011	n/a
BC	10111100	n/a
BD	10111101	n/a
BE	10111110	n/a
BF	10111111	n/a

Hex (VID7:VID0)	Bin (VID7:VID0)	Voltage
C0	11000000	n/a
C1	11000001	n/a
C2	11000010	n/a
C3	11000011	n/a
C4	11000100	n/a
C5	11000101	n/a
C6	11000110	n/a
C7	11000111	n/a
C8	11001000	n/a
C9	11001001	n/a
CA	11001010	n/a
CB	11001011	n/a
CC	11001100	n/a
CD	11001101	n/a
CE	11001110	n/a
CF	11001111	n/a
D0	11010000	n/a
D1	11010001	n/a
D2	11010010	n/a
D3	11010011	n/a
D4	11010100	n/a
D5	11010101	n/a
D6	11010110	n/a
D7	11010111	n/a
D8	11011000	n/a
D9	11011001	n/a
DA	11011010	n/a
DB	11011011	n/a
DC	11011100	n/a
DD	11011101	n/a
DE	11011110	n/a
DF	11011111	n/a
E0	11100000	n/a
E1	11100001	n/a
E2	11100010	n/a
E3	11100011	n/a
E4	11100100	n/a
E5	11100101	n/a
E6	11100110	n/a
E7	11100111	n/a
E8	11101000	n/a
E9	11101001	n/a
EA	11101010	n/a
EB	11101011	n/a
EC	11101100	n/a
ED	11101101	n/a
EE	11101110	n/a
EF	11101111	n/a
F0	11110000	n/a
F1	11110001	n/a
F2	11110010	n/a
F3	11110011	n/a
F4	11110100	n/a
F5	11110101	n/a
F6	11110110	n/a
F7	11110111	n/a
F8	11111000	n/a
F9	11111001	n/a
FA	11111010	n/a
FB	11111011	n/a
FC	11111100	n/a
FD	11111101	n/a
FE	11111110	FAULT
FF	11111111	FAULT

Start-up Sequence

The IR3503 has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL and LGND pins controls soft start timing, over-current protection delay and hiccup mode timing. A charge current of 52.5 µA and discharge current of 4 µA control the up slope and down slope of the voltage at the SS/DEL pin respectively. Figure 11 depicts start-up sequence of converter with VR 11.1 VID. If there is no fault, as the ENABLE is asserted, the SS/DEL pin will start charging. The error amplifier output EAOUT is clamped low until SS/DEL reaches 1.4 V. The error amplifier will then regulate the converter's output voltage to match the SS/DEL voltage less the 1.4 V offset until the converter output reaches the 1.1 V boot voltage. The SS/DEL voltage continues to increase until it rises above the 3.0 V threshold of VID delay comparator. The VID set inputs are then activated and VDAC pin transitions to the level determined by the VID inputs. The SS/DEL voltage continues to increase until it rises above 3.92 V and allows the VRRDY signal to be asserted. SS/DEL finally settles at 4.0 V, indicating the end of the soft start. The remote sense amplifier has a very low operating range of 50 mV in order to achieve a smooth soft start of output voltage without bump. *The rise time of the VCCL applied to the system should be at least greater than 25 µs.*

The VCCL under voltage lock-out, VID fault modes, over current, as well as a low signal on the ENABLE input immediately sets the fault latch, which causes the EAOUT pin to drive low turning off the phase IC drivers. The VRRDY pin also drives low and SS/DEL begin to discharge until the voltage reaches 0.2 V. If the fault has cleared the fault latch will be reset by the discharge comparator allowing a normal soft start to occur.

Other fault conditions, such as over voltage, open sense lines, open loop monitor, and open daisy chain, set different fault latches, which start discharging SS/DEL, pull down EAOUT voltage and drive VRRDY low. However, the latches can only be reset by cycling VCCL power.

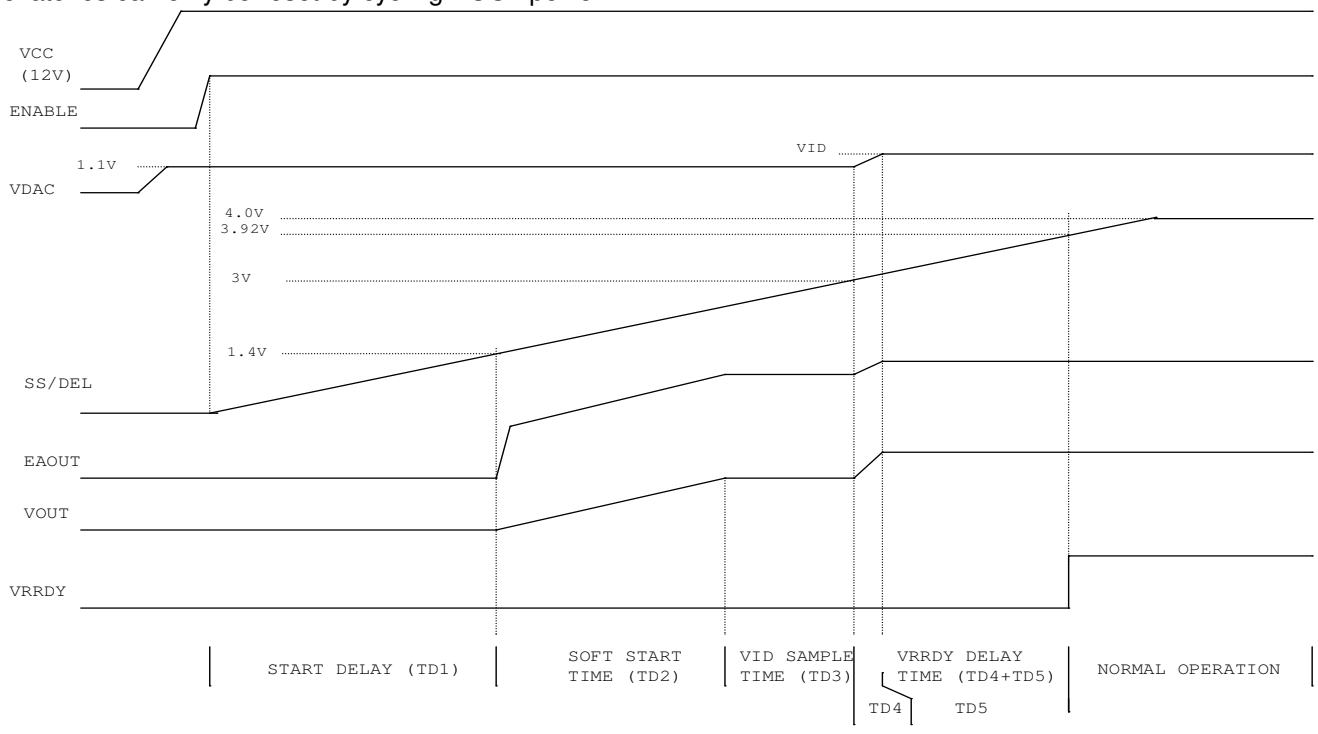


Figure 11: Start-up Sequence of the Converter with Boot Voltage

Current Monitor (IMON)

The control IC generates a current monitor signal IMON using the VDRP voltage and the VDAC reference, as shown in Figure 12. This voltage is thermally compensated for the inductor DCR variation. The voltage at this pin reports the average load current information without being referenced to VDAC. The slope of the IMON signal with

respect to the load current can be adjusted with the resistors RTCMP2 and RTCMP3. The IMON signal is clamped at 1.03V in order to facilitate direct interfacing with the CPU.

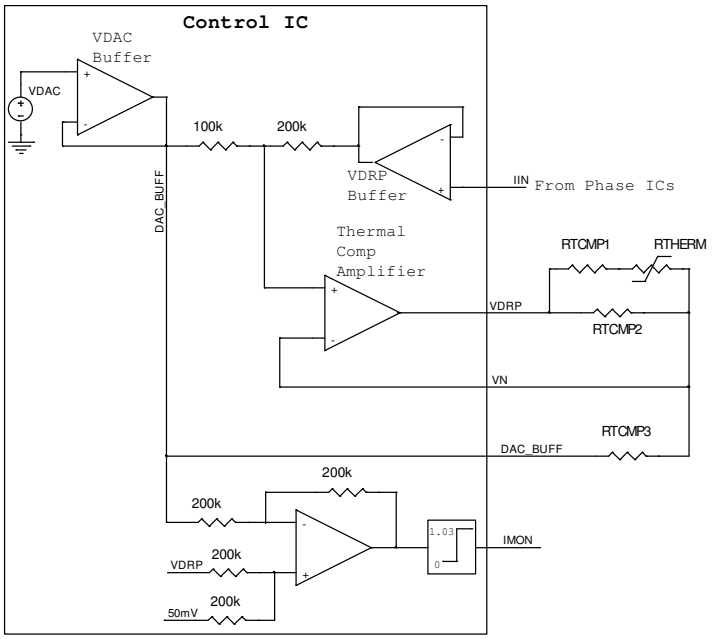


Figure 12: Current Report Signal (IMON) implementation

Power State Indicator (PSI#)

PSI# is an active low input logic signal to IR3503 sent by the CPU. The PSI# signal will be asserted (low) whenever the CPU enters low power state. IR3503 uses this signal to improve the efficiency of the voltage regulator (VR) by turning off a few phases under light load conditions. A single PSI# bus is hard wired to all the phase ICs. Once, PSI# is asserted (low), IR3503 waits for 7 CLKOUT cycles and then registers the active number of phases at that instant. The phase IC (IR3529) waits for 8 PHSIN cycles after PSI# assertion to shut the phase off and then issues a down SHIFT signal. On PSI# de-assertion, IR3503 cranks the CLKOUT frequency (corresponding to the number of phases active before PSI# assertion) once it receives an up SHIFT signal from the phase ICs. *The first phase in the daisy chain should be always on during PSI mode of operation. The system design should also ensure that the VR is not forced into PSI mode of operation within 8 switching cycles after a phase shed event.*

SHIFT Signal Implementation:

The SHIFT function is used to communicate the status change of the phase ICs in order to improve the daisy chain timing. The main objective is to minimize the output voltage deviation when phases are taken into or out of the daisy chain loop. The SHIFT signal rides on $\frac{V_{CCL}}{2}$ and is pulled up to VCCL to indicate an up shift in CLK frequency (insertion of phases) and is pulled down to LGND to indicate a down shift in CLK frequency (phase shedding operation). Changes in the number of phases in the system may occur due to the following operations:

- *Active or Dynamic Shedding:* This is a post-power up event when phases are shut down based on the load requirements. Such an operation will lead to perturbations in the output voltage.
- *Static Shedding:* This may occur prior to power supply turn-on as long as phases are not de-shed post-power up. Since, this occurs when the power supply is turned off and hence does not affect the output voltage.
- *PSI# assertion or de-assertion:* This is mostly a dynamic event and it will affect the output voltage. The maximum permissible deviation in output voltage is slightly higher during such events.

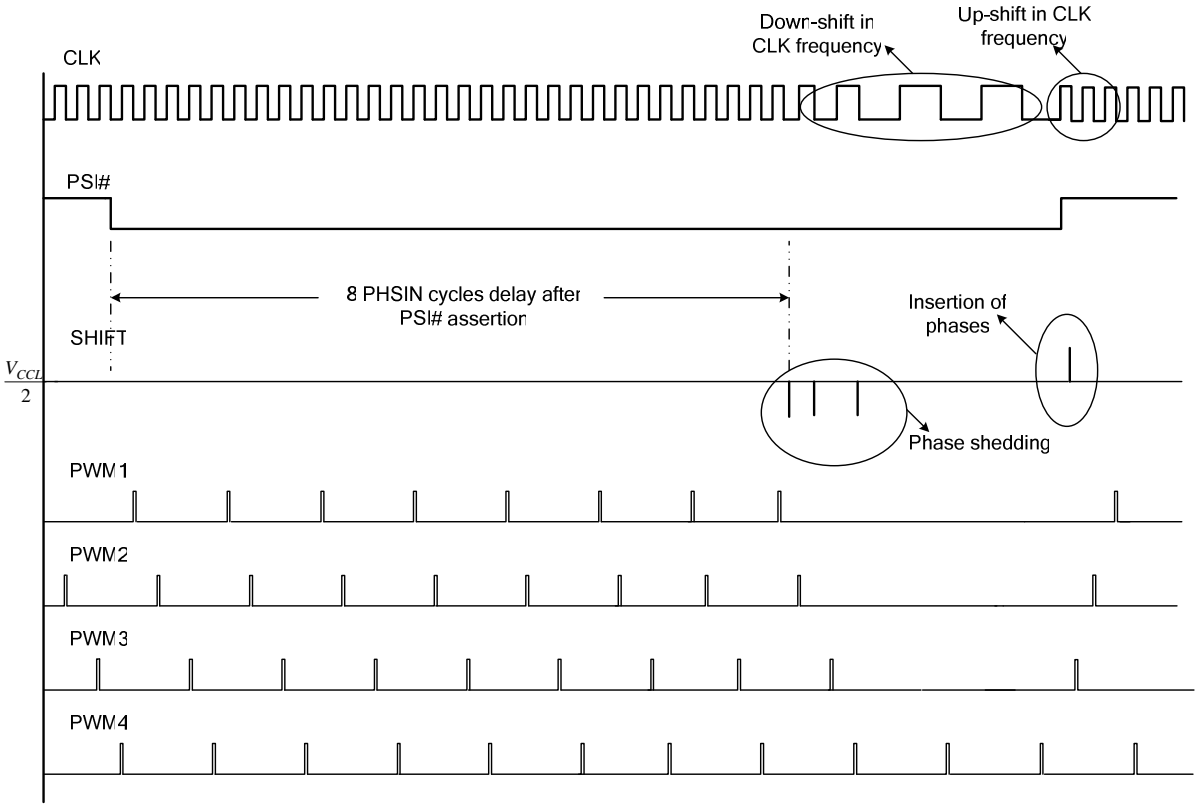


Figure 13: SHIFT functionality

Figure 13 clearly explains the SHIFT functionality. The phase ICs wait for 8 PHSIN cycles after the assertion of PSI# to start shedding the phases (and issue a down SHIFT signal). When the phases are shed, the CLK frequency is also reduced simultaneously. The SHIFT signal is synchronized with the CLKOUT falling edge. However, on de-assertion of PSI#, all the phases that were active before PSI# assertion will be restored immediately without any delay. Another key feature in IR3503 is the internal programming of over-current protection (OCP). The OCP threshold is calculated based on the number of phases in the system as given by the equation below:

$$\text{OCP threshold} = \frac{1.17 * \text{Number of active phases}}{\text{Maximum number of phases}}$$

Hence, the OCP threshold will be automatically adjusted based on the number of active phases in the system. When PSI# de-assertion occurs, all the phases in the system are restored immediately without any delay which can also be clearly observed in figure 13.

Over-Current Hiccup Protection after Soft Start

The over current limit is fixed at $\boxed{\frac{1.17 * \text{Number of active phases}}{\text{Maximum number of phases}}}$ above the VDAC. Figure 14 shows the constant over-current control with delay after VRRDY is asserted. The delay is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions.

If the VDRP pin voltage, which is proportional to the average current plus VDAC voltage, exceeds the over current protection (OCP) limit after VRRDY is asserted, it will initiate the discharge of the capacitor at SS/DEL. The magnitude of the discharge current is proportional to the voltage difference between VDRP and OCP limit and has a maximum nominal value of 55uA. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 120 mV offset of the delay comparator, the fault latch will be set pulling the error amplifier's

output low and inhibiting switching in the phase ICs and de-asserting the VRRDY signal. The output current is not controlled during the delay time. The SS/DEL capacitor will discharge until it reaches 200 mV and the fault latch is reset allowing a normal soft**.**

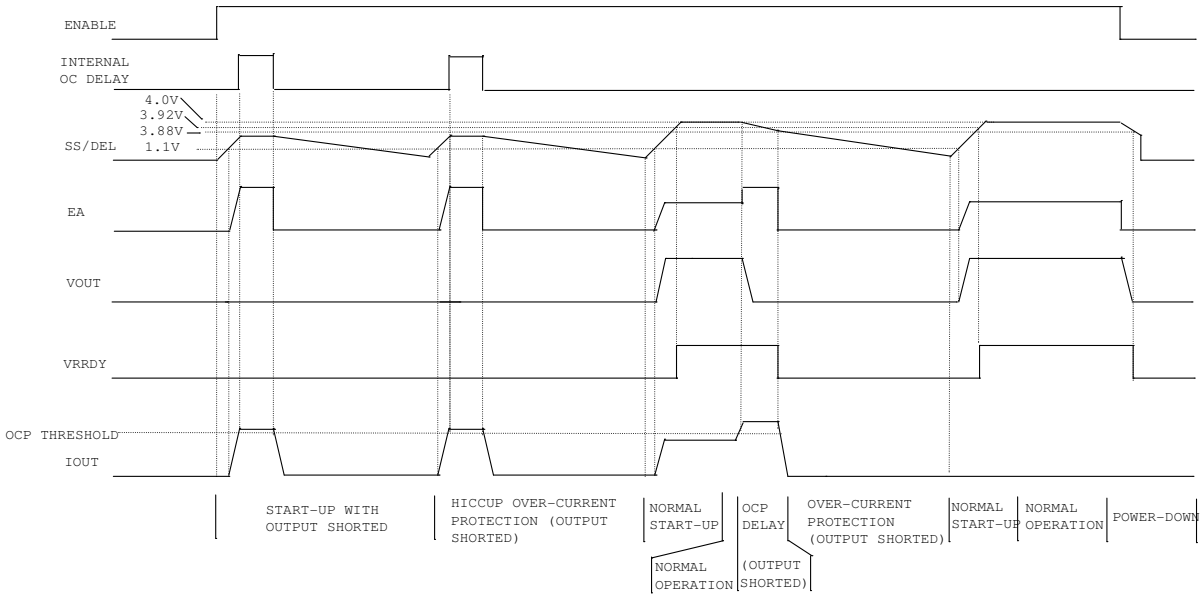


Figure 14: Constant over-current protection during and after soft-start

VCCL Under Voltage Lockout (UVLO)

The IR3503 has no under voltage lockout for converter input voltage (VCC), but monitors the VCCL voltage instead, which is used for the gate drivers of phase ICs and circuits in control IC and phase ICs. During power up, the fault latch will be reset if VCCL is above 4.2 V. If VCCL voltage drops below 3.8 V, the fault latch will be set.

Over Voltage Protection (OVP)

Output over-voltage happens during normal operation if a high side MOSFET short occurs or if output voltage is out of regulation. The over-voltage protection comparator monitors VO pin voltage. If VO pin voltage exceeds VDAC by 130mV after SS, as shown in Figure 15, IR3503 raises ROSC/OVP pin voltage above to V (VCCL) - 1V, which sends over voltage signal to system. The ROSC/OVP pin can also be connected to a thyristor in a crowbar circuit, which pulls the converter input low in over voltage conditions. The over voltage condition also sets the over voltage fault latch, which pulls error amplifier output low to turn off the converter output. At the same time IIN pin (IIN of phase ICs) is pulled up to VCCL to communicate the over voltage condition to phase ICs, as shown in Figure 15. In each phase IC, the OVP circuit overrides the normal PWM operation and will fully turn-on the low side MOSFET within approximately 150ns. The low side MOSFET will remain on until IIN pin voltage drops below V(VCCL) - 800mV, which signals the end of over voltage condition. An over voltage fault condition is latched in the IR3503 and can only be cleared by recycling VCCL or ENABLE.

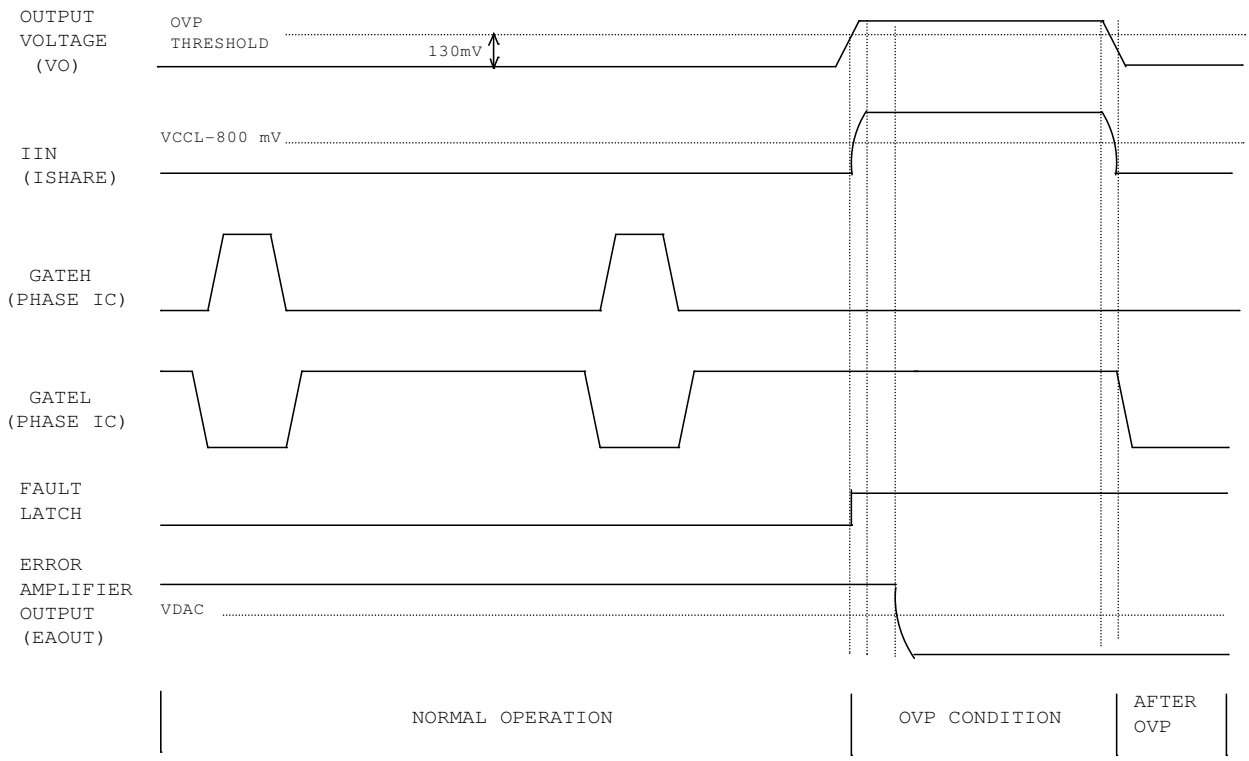


Figure 15: Over voltage protection during normal operation

During dynamic VID down, OVP may be triggered when output voltage can not follow VDAC voltage change at light load with large output capacitance. Therefore, over-voltage threshold is raised to 1.73V from VDAC+130mV whenever dynamic VID is detected and the difference between output voltage and VDAC is more than 50mV, as shown in Figure 16. The over-voltage threshold is changed back to VDAC+130mV if the difference is smaller than 50mV.

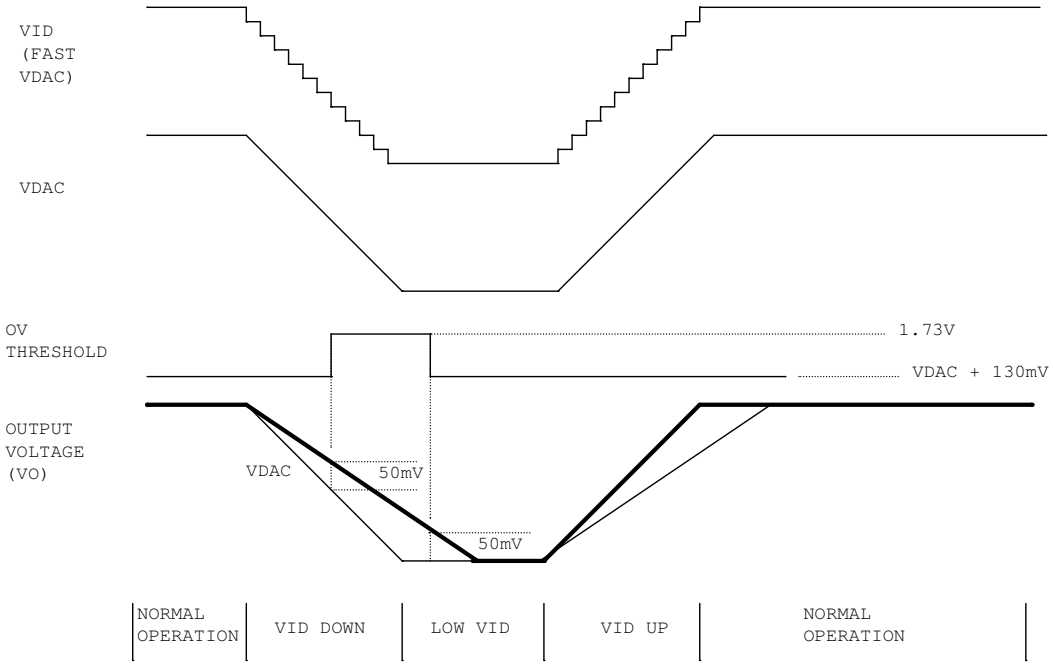


Figure 16: Over voltage protection during dynamic VID transition

VID Fault Codes

VID codes of 0000000X and 1111111X for VR11 will set the fault latch and disable the error amplifier. A 1.3 µs delay is provided to prevent a fault condition from occurring during Dynamic VID changes. A VID FAULT condition is latched with boot voltage and can only be cleared by cycling power to VCCL or re-issuing ENABLE.

Voltage Regulator Ready (VRRDY)

The VRRDY pin is an open-collector output and should be pulled up to a voltage source through a resistor. After the soft start completion cycle, the VRRDY remains high until the output voltage is in regulation and SS/DEL is above 3.92 V. The VRRDY pin becomes low if the fault latch, over voltage latch, open sense line latch, or open daisy chain is set. A high level at the VRRDY pin indicates that the converter is in operation and has no fault. The VRRDY stays high as long as the output voltage is within 300 mV of the programmed VID. During start-up, it is pulled low with an input voltage as low as 2 V. It stays low until the startup sequence has completed, and the output voltage has moved to the programmed VID.

Open Voltage Loop Detection

The output voltage range of error amplifier is detected all the time to ensure the voltage loop is in regulation. If any fault condition forces the error amplifier output above VCCL-1.08 V for 8 switching cycles, the fault latch is set. The fault latch can only be cleared by cycling power to VCCL.

Open Remote Sense Line Protection

If either remote sense line VOSEN+ or VOSEN- or both are open, the output of remote sense amplifier (VO) drops. The IR3503 monitors VO pin voltage continuously. If VO voltage is lower than 200 mV, two separate pulse currents are applied to VOSEN+ and VOSEN- pins respectively to check if the sense lines are open. If VOSEN+ is open, a voltage higher than 90 % of V(VCCL) will be present at VOSEN+ pin and the output of open line detect comparator will be high. If VOSEN- is open, a voltage higher than 700 mV will be present at VOSEN- pin and the output of open-line-detect comparator will be high. The open sense line fault latch is set, which pulls error amplifier output low immediately and shut down the converter. The SS/DEL voltage is discharged and the fault latch can only be reset by cycling VCCL power. During dynamic VID down, OVP may be triggered when output voltage can not follow

VDAC voltage change at light load with large output capacitance. Therefore, over-voltage threshold is raised to 1.73 V from VDAC+130 mV whenever dynamic VID is detected and the difference between output voltage and VDAC is more than 50mV, as shown in Figure 17. The over-voltage threshold is changed back to VDAC+130 mV if the difference is smaller than 50 mV.

Open Daisy Chain Protection

IR3503 checks the daisy chain every time it powers up. It starts a daisy chain pulse on the PHSOUT pin and detects the feedback at PHSIN pin. If no pulse comes back after 32 CLKOUT pulses, the pulse is restarted again. If the pulse fails to come back the second time, the open daisy chain fault is registered, and SS/DEL is not allowed to charge. The fault latch can only be reset by cycling the power to VCCL.

After powering up, the IR3503 monitors PHSIN pin for a phase input pulse equal or less than the number of phases detected. If PHSIN pulse does not return within the number of phases in the converter, another pulse is started on PHSOUT pin. If the second started PHSOUT pulse does not return on PHSIN, an open daisy chain fault is registered.

Enable Input

The ENABLE pin below 0.8 V sets the Fault Latch and a voltage above 0.85 V enables the soft start of the converter.

Thermal Monitoring (VRHOT)

A resistor divider including a thermistor at HOTSET pin sets the VRHOT threshold. The thermistor is usually placed at the temperature sensitive region of the converter, and is linearized by a series resistor. The IR3503 compare HOTSET pin voltage with a reference voltage of 1.6 V. The VRHOT pin is an open-collector output and should be pulled up to a voltage source through a resistor. If the thermal trip point is reached the VRHOT output drives low. The hysteresis of the VRHOT comparator helps eliminate toggling of VRHOT output.

The overall system must be considered when designing for OVP. In many cases the over-current protection of the AC-DC or DC-DC converter supplying the multiphase converter will be triggered and provide effective protection without damage as long as all PCB traces and components are sized to handle the worst-case maximum current. If this is not possible, a fuse can be added in the input supply to the multiphase converter.

Phase Number Determination

After a daisy chain pulse is started, the IR3503 checks the timing of the input pulse at PHSIN pin to determine the phase number. This information is used to have symmetrical phase delay between phase switching without the need of any external component.

Single Phase Operation

In an architecture where only a single phase is needed the switching frequency is determined by the clock frequency.

Current Share Loop Compensation

The internal compensation of current share loop ensures that crossover frequency of the current share loop is at least one decade lower than that of the voltage loop so that the interaction between the two loops is eliminated. The crossover frequency of current share loop is approximately 8 kHz.

Fault Operation Table

	Fault Type									
	Open Daisy	**Open Control Loop**	**Open Sense Line**	**Over Voltage**	**VID**	**Disable**	**VCCL UVLO**	**OC Before Start-up**	**OC After Start-up**	**VOUT UVLO**
Fault Clearing Method	Recycle VCCL			Recycle VCCL, ENABLE	Recycle VCCL	Resume Normal Operation when Condition Clears				
Error Amp Disabled	Yes									No
ROSC/OVP & IIN drive high until OV clears	No			Yes	No					
SS/DEL Discharge	Yes									No
Flags PGood	Yes									
Delay	32 Clock Pulses	8 PHSOUT Pulses	No	No	1.3us Blank Time	250 ns Blank Time	No	PHSOUT Pulses. Count Programmed by ROSC value	SS/DEL Discharge Threshold	No

DESIGN PROCEDURES - IR3503 AND IR3529 CHIPSET

IR3503 EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

The oscillator of IR3503 generates square-wave pulses to synchronize the phase ICs. The switching frequency of the each phase converter equals the PHSOUT frequency, which is set by the external resistor ROSC according to the curve in Figure 6. The CLKOUT frequency equals the switching frequency multiplied by the phase number. The Rosc sets the reference current used for no load offset which can be calculated by the equation shown below:

$$ISETPT = \frac{0.595}{Rosc} \tag{1}$$

Soft Start Capacitor *CSS/DEL*

The soft start capacitor CSS/DEL programs five different time parameters. They include soft start delay time, soft start time, VID sample delay time, VR ready delay time and over-current fault latch delay time after VR ready.

For the converter using VID with boot voltage, the SS/DEL pin voltage controls the slew rate of the converter output voltage, as shown in Figure 11. After the ENABLE pin voltage rises above 0.85V, there is a soft-start delay time TD1, after which the error amplifier output is released to allow the soft start of output voltage. The soft start time TD2 represents the time during which converter voltage rises from 0 to 1.1V. The VID sample delay time (TD3) is the time period when VID stays at boot voltage of 1.1V. VID rise or fall time (TD4) is the time when VID changes from boot voltage to the final voltage. The VRRDY delay time (TD5) is the time period from VR reaching the final voltage to the VRRDY signal being issued, which is determined by the delay comparator threshold.

CSS/DEL = 0.1uF meets all the specifications of TD1 to TD5, which are determined by (2) to (6) respectively.

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{C_{SS/DEL} * 1.4}{52.5 * 10^{-6}} \tag{2}$$

$$TD2 = \frac{C_{SS/DEL} * 1.1}{I_{CHG}} = \frac{C_{SS/DEL} * 1.1}{52.5 * 10^{-6}} \tag{3}$$

$$TD3 = \frac{C_{SS/DEL} * (3 - 1.4 - 1.1)}{I_{CHG}} = \frac{C_{SS/DEL} * 0.7}{52.5 * 10^{-6}} \tag{4}$$

$$TD4 = \frac{C_{SS/DEL} * |V_{DAC} - 1.1|}{I_{CHG}} = \frac{C_{SS/DEL} * |V_{DAC} - 1.1|}{52.5 * 10^{-6}} \tag{5}$$

$$TD5 = \frac{C_{SS/DEL} * (3.92 - 3)}{I_{CHG}} - TD4 = \frac{C_{SS/DEL} * 0.92}{52.5 * 10^{-6}} - TD4 \tag{6}$$

$$C_{SS/DEL} = \frac{TD2 * I_{CHG}}{V_O} = \frac{TD2 * 52.5 * 10^{-6}}{V_O} \quad (7)$$

The soft start delay time (TD1) and VR ready delay time (TD3) are determined by (8) to (9) respectively.

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{C_{SS/DEL} * 1.4}{52.5 * 10^{-6}} \quad (8)$$

$$TD3 = \frac{C_{SS/DEL} * (4.0 - V_O)}{I_{CHG}} = \frac{C_{SS/DEL} * (4.0 - V_O)}{52.5 * 10^{-6}} \quad (9)$$

Once $C_{SS/DEL}$ is chosen, the minimum over-current fault latch delay time t_{OCDEL} is fixed and can be quantified as

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.12}{I_{DISCHG}} = \frac{C_{SS/DEL} * 0.12}{55 * 10^{-6}} \quad (10)$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

The slew rate of VDAC slope SR_{DOWN} can be programmed by the external capacitor C_{VDAC} as defined in (11), where I_{SINK} is the sink current of VDAC pin. The slew rate of VDAC up-slope is the same as that of down-slope. The resistor R_{VDAC} is used to compensate VDAC circuit and can be calculated as follows

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{44 * 10^{-6}}{SR_{DOWN}} \quad (11)$$

$$R_{VDAC} = \frac{1}{2 \cdot \pi \cdot 900kHz \cdot C_{VDAC}} \quad (12)$$

Current Report Gain and Thermal Compensation

Intel VR11.1 specifications require IMON to report the core maximum load current of the CPU be reported as 1 V nominal. The core maximum current can be different for different platforms. The IMON tuning resistors can therefore be adjusted and thermally compensated to adjust the load current gain with respect to the IMON. The expressions that govern the relationship between load current, IMON, and VDRP at room temperature are given by

$$VDRP = VDAC + \frac{1}{3} \cdot \left(\frac{R_{L\_room} \cdot G_{cs}}{n} \right) \cdot \left[1 + \frac{(RTCMP3) II (RTCMP1 + RTHERM\_room)}{RTCMP3} \right] \cdot I_o \quad (13)$$

$$IMON = \frac{1}{3} \cdot \left(\frac{R_{L\_room} \cdot G_{cs}}{n} \right) \cdot \left[1 + \frac{(RTCMP3) II (RTCMP1 + RTHERM\_room)}{RTCMP3} \right] \cdot I_o \quad (14)$$

The change in inductor DCR with temperature is compensated by an equivalent variation in the RTHERM. The following equations derive the R_{TCMP1} and R_{TCMP2} if R_{TCMP3} and the thermistor (R_{THERM} and β_{THERM}) are fixed.

$$R_{L\_MAX} = R_{L\_room} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{room})] \quad (15)$$

$$K_{THERM\_room} = \frac{1V}{I_{o\max}}, K_{c\_room} = \frac{(R_{L\_room} \cdot G_{cs})}{n}, K_{c\_t\max} = \frac{(R_{L\_\max} \cdot G_{cs})}{n} \quad (16)$$

$$R_{t\_room} = \left(\frac{3 \cdot K_{THERM\_room}}{K_{c\_room}} - 1 \right) \cdot RTCMP3 \quad (17)$$

$$R_{t\_t\max} = \left(\frac{3 \cdot K_{THERM\_room}}{K_{c\_t\max}} - 1 \right) \cdot RTCMP3 \quad (18)$$

$$RTHERM_{t\max} = RTHERM_{room} \cdot e^{\beta_{THERM} \cdot \left(\frac{1}{273+T_{\max}} - \frac{1}{273+T_{room}} \right)} \quad (19)$$

$$B_{TH} = RTHERM_{room} + RTHERM_{t\max} \quad (20)$$

$$C_{TH} = RTHERM_{room} \cdot RTHERM_{t\max} - \left(\frac{RTHERM_{room} - RTHERM_{t\max}}{\frac{1}{R_{t\_t\max}} - \frac{1}{R_{t\_room}}} \right) \quad (21)$$

$$RTCMP1 = \frac{-B_{TH} + \sqrt{(B_{TH})^2 - 4 \cdot C_{TH}}}{2} \quad (22)$$

$$RTCMP2 = \frac{1}{\left(\frac{1}{R_{t\_t\max}} - \frac{1}{R_{t\_t\max} + RTCMP1} \right)} \quad (23)$$

Droop Resistor

The inductor DC resistance is utilized to sense the inductor current. The copper wire of inductor has a constant temperature coefficient of 3850 ppm/℃, and therefore the maximum inductor DCR can be calculated from (15), where R_{L_tmax} and R_{L_room} are the inductor DCR at maximum temperature T_{max} and room temperature T_{room} respectively. After the thermal compensation is achieved using the procedure given above, the droop resistance can be calculated using the following equation.

$$R_{DRP} = \frac{1}{3} * \frac{R_{FB}}{R_o} * \left(\frac{G_{CS} * R_{L\_ROOM}}{n} \right) * \left[1 + \frac{R_{t\_room}}{RTCMP3} \right] \quad (24)$$

Over-current Threshold

Once the current report gain and the thermal compensation are calculated the OCP threshold is calculated using the following expression.

$$I_{OCP} = \frac{1.17}{\frac{1}{3} \cdot \left(\frac{R_{L\_room} \cdot G_{cs}}{n} \right) \cdot \left[1 + \frac{(RTCMP2) // (RTCMP1 + RTHERM\_room)}{RTCMP3} \right]} \times \left(\frac{Number\_of\_active\_phases}{Maximum\_number\_of\_phases} \right) \quad (25)$$

No Load Output Voltage Setting Resistor *RVSETPT*,

A resistor between VSETPT pin and VDAC is used to create output voltage offset V_{O_NLOFST}, which is the difference between V_{DAC} voltage and output voltage at no load condition. R_{VSETPT} is determined by (26), where I_{VSETPT} is the current flowing out of VSETPT pin as shown in Figure 19.

$$R_{VSETPT} = \frac{V_{O\_NLOFST}}{I_{VSETPT}} \quad (26)$$

Thermistor *RTHERM* and Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

The threshold voltage of VRHOT comparator is fixed at 1.6V, and a negative temperature coefficient (NTC) thermistor R_{THERM} is required to sense the temperature of the power stage. If we pre-select R_{THERM}, the NTC thermistor resistance at allowed maximum temperature T_{MAX} is calculated from (27).

$$R_{TMAX} = R_{THERM} * EXP[B_{THERM} * (\frac{1}{T_{L\_MAX}} - \frac{1}{T_{\_ROOM}})] \quad (27)$$

Select the series resistor $R_{HOTSET2}$ to linearize the NTC thermistor, which has non-linear characteristics in the operational temperature range. Then calculate $R_{HOTSET1}$ corresponding to the allowed maximum temperature T_{MAX} from (28).

$$R_{HOTSET1} = \frac{(R_{TMAX} + R_{HOTSET2}) * (VCCL - 1.6)}{1.6} \quad (28)$$

VCCL Capacitor *CVCCL*

The capacitor is selected based on the stability requirement of the linear regulator and the load current to be driven. The linear regulator supplies the bias and gate drive current of the phase ICs. A 4.7uF normally ensures a stable VCCL performance for Intel VR11.1 applications.

Current Monitor Filter

A filter is added to isolate the CPU from rapid changes in the load current and trigger false response. A filter with 300 µs time constant provides adequate delay for Intel VR11.1 response. A 1k resistor between IMON and local ground helps equalize the source and sink current of the IMON pin.

DESIGN EXAMPLE

SPECIFICATIONS

Input Voltage: V_{IN} =12 V
DAC Voltage: V_{DAC} = 1.2 V
No Load Output Voltage Offset: V_{O_NLOFST} = 10 mV
Continuous Output Current: I_{OTDC} = 110 A
Current for Gain Setting for IMON: $I_{O, PEAK}$=180 A
Current Report Gain = 0.95 V represents $I_{O, PEAK}$
Output Impedance: R_O = 0.8 mΩ
Soft Start Delay Time: TD1 = 0-5 ms
Soft Start Time: TD2 = 0.05 ms - 10 ms
VID Sample Delay Time: TD3 = 0.05-3 ms
VID Rise Time: TD4 = 0 - 3.5 ms
VR Ready Delay Time: TD5 = 0.05 - 3 ms
Maximum Over Current Delay Time: t_{OCDEL} < 2.5 ms
Dynamic VID Up-Slope Slew Rate: SR_{up} = 10 mV/µs
Over Temperature Threshold: T_{MAX} = 100 ºC

POWER STAGE

Phase Number: n = 5
Switching Frequency: f_{SW} = 400 kHz
Output Inductors: L = 150 nH, R_L = 0.29 mΩ
Output Capacitors: Ceramic: C = 22µF, Number N_C = 50
SP : C = 470 µF, Number N_{SP}= 4

IR3503 EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

Once the switching frequency is chosen, R_{OSC} can be determined from the curve in Figure 6 of this data sheet. For a switching frequency of 400 kHz per phase, choose R_{OSC} = 30.1 kΩ. The reference current is given by 19.9 µA. This will also be the bias current for the VSETPT pin.

Soft Start Capacitor *$C_{SS/DEL}$*

Determine the soft start capacitor to meet the specifications of the delay time.

Choose $C_{SS/DEL}$ = 0.1µF. The soft start delay time is

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{0.1 * 10^{-6} * 1.4}{52.5 * 10^{-6}} = 2.67mS$$

The soft start time is

$$TD2 = \frac{C_{SS/DEL} * 1.1}{I_{CHG}} = \frac{0.1 * 10^{-6} * 1.1}{52.5 * 10^{-6}} = 2.1mS$$

The VID sample delay time is

$$TD3 = \frac{C_{SS/DEL} * (3.2 - 1.4 - 1.1)}{I_{CHG}} = \frac{0.1 * 10^{-6} * 0.7}{52.5 * 10^{-6}} = 1.33mS$$

VID rise time is

$$TD4 = \frac{C_{SS/DEL} * |V_{DAC} - 1.1|}{I_{CHG}} = \frac{0.1*10^{-6} * |1.3 - 1.1|}{52.5*10^{-6}} = 0.38mS$$

The VRRDY delay time is

$$TD5 = \frac{C_{SS/DEL} * (3.92 - 3)}{I_{CHG}} - TD4 = \frac{0.1*10^{-6} * 0.92}{52.5*10^{-6}} - TD4 = 1.37mS$$

Minimum over current fault latch delay time is

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.12}{I_{OCDISCHG}} = \frac{0.1*10^{-6} * 0.12}{55*10^{-6}} = 0.21ms$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

Calculate the VDAC down-slope slew-rate programming capacitor from the required down-slope slew rate. The up-slope slew rate is the same as the down-slope slew rate.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{44*10^{-6}}{10*10^{-3}/10^{-6}} = 4.4nF$$

A 3.3 nF capacitor can be used. A series resistor is used to stabilize the VDAC buffer.

$R_{VDAC} = \frac{1}{2 \cdot \pi \cdot 900kHz \cdot C_{VDAC}} = 53\Omega$. A 50 Ω resistor is selected.

No Load Output Voltage Setting Resistor *RVSETPT*

The bias current of VSETPT pin is 19.9 µA with ROSC = 30.1 kΩ.

$$R_{VSETPT} = \frac{V_{O\_NLOFST}}{I_{VSETPT}} = \frac{10*10^{-3}}{19.9*10^{-6}} = 499\Omega$$

Current Report Gain and Thermal Compensation

The reporting gain specifies the maximum load current in the form of a voltage. For this example, the 180 A current represents 0.95 V at IMON. If the thermal effects are neglected (14) can be used to find the reporting gain. However, as the inductor DCR increases with temperature, the thermal compensation string (RTCMP1, RTCMP2, and RTHERM) can be used to compensate this change in DCR.

Assuming T_{room} =25 ºC, T_{max}=100 ºC the change in DCR can be found using (15)

$$R_{L\_MAX} = 0.29m * [1 + 3850*10^{-6} * (100 - 25)] = 0.374m\Omega$$

Pre-select RTCMP3 =1 kΩ, and R_{THERM_room}=10 kΩ with β_{THERM} = 3380K. RTCMP1 and RTCMP2 can be found out using (16)-(23)

RTCMP1 = 9.411 kΩ
RTCMP2 = 9.24 kΩ

Droop Resistor

Based on the above calculation R_{DRP} can be selected to obtain specific output impedance.

Pre-select R_{FB} = 2 kΩ and using R_O = 0.8 mΩ, G_{CS} = 33 along with the converter parameters can be plugged into (24) to find out R_{DRP}.

$$R_{DRP} = \frac{1}{3} * \frac{2k\Omega}{0.8m\Omega} * \left(\frac{33 * 0.29m}{5}\right) * \left[1 + \frac{7.699k}{1k}\right] = 13.87k\Omega$$

Over Current Threshold

The OCP threshold is fixed at 1.17 V above the VDAC voltage. Therefore, it can be determined based on (25) depending upon the number of active phases in the system as shown below:

$$5\_phase\_system\_I_{OCP} = \frac{1.17}{\left[\frac{1}{3}\cdot\left(\frac{0.29m\cdot 33}{5}\right)\cdot\left(1+\frac{(9.24k)II(9.411k+10k)}{1k}\right)\right]} \times \left(\frac{5}{5}\right) = 252.6A$$

$$4\_phase\_system\_I_{OCP} = \frac{1.17}{\left[\frac{1}{3}\cdot\left(\frac{0.29m\cdot 33}{5}\right)\cdot\left(1+\frac{(9.24k)II(9.411k+10k)}{1k}\right)\right]} \times \left(\frac{4}{5}\right) = 202A$$

$$1\_phase\_system\_I_{OCP} = \frac{1.17}{\left[\frac{1}{3}\cdot\left(\frac{0.29m\cdot 33}{5}\right)\cdot\left(1+\frac{(9.24k)II(9.411k+10k)}{1k}\right)\right]} \times \left(\frac{1}{5}\right) = 50.5A$$

Thermistor *RTHERM* and Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

Choose NTC thermistor RTHERM = 2.2 kΩ, which has a constant of B_{THERM} = 3520, and the NTC thermistor resistance at the allowed maximum temperature T_{MAX} is,

$$R_{TMAX} = R_{THERM} * EXP[B_{THERM} * (\frac{1}{T_{L\_MAX}} - \frac{1}{T_{\_ROOM}})] = 2.2 * 10^3 * EXP[3520 * (\frac{1}{273+115} - \frac{1}{273+25})] = 142\Omega$$

Select RHOTSET2 = 931 Ω to linearize the NTC, which has non-linear characteristics in the operational temperature range.

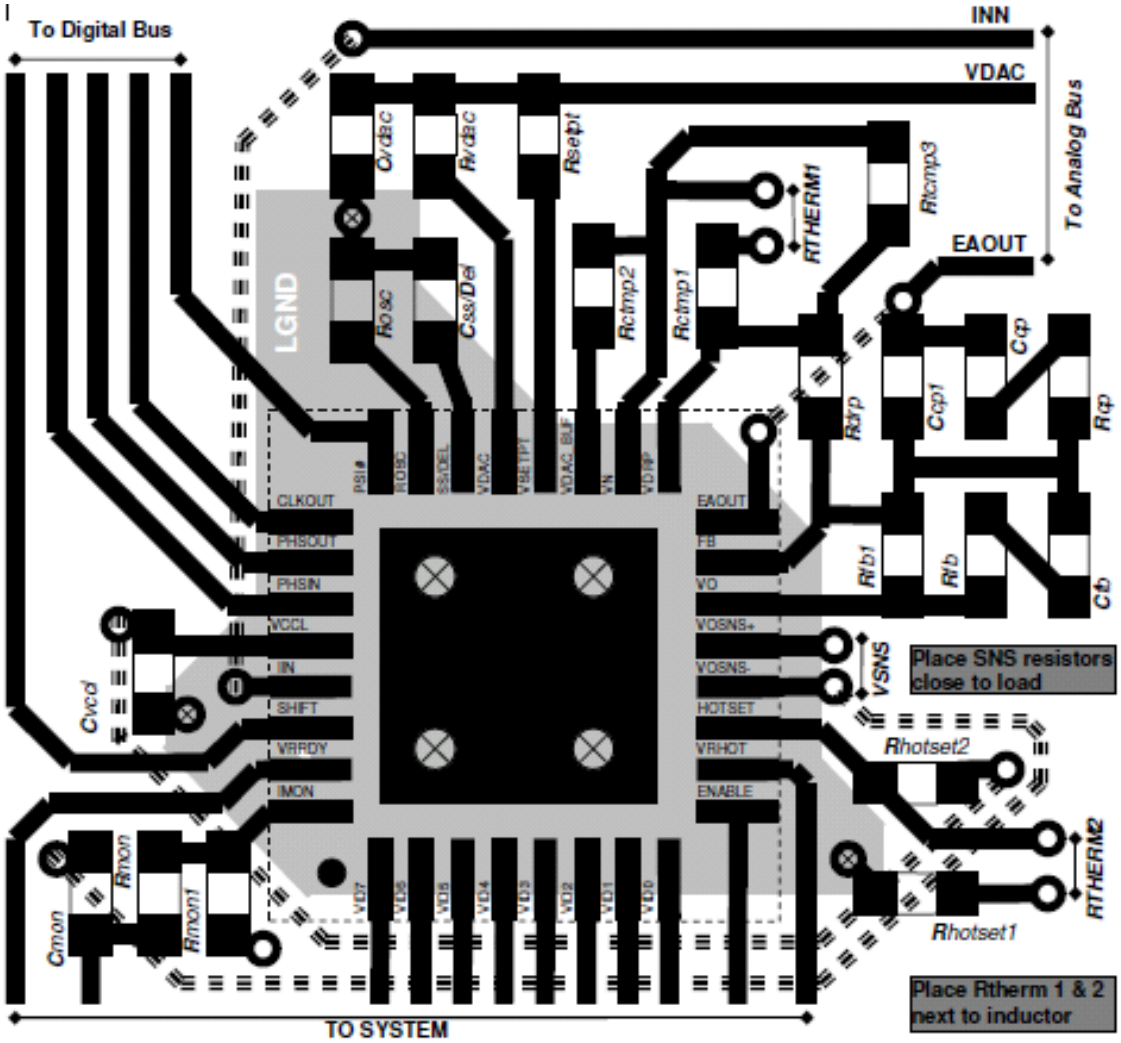
Then calculate RHOTSET1 corresponding to the allowed maximum temperature T_{MAX} as shown below:

$$R_{HOTSET1} = \frac{(R_{TMAX} + R_{HOTSET2}) * (VCCL - 1.6)}{1.6} = \frac{(142 + 931) * (7 - 1.6)}{1.6} = 3.63k\Omega$$, choose RHOTSET1 = 3.65 kΩ

Layout Guidelines

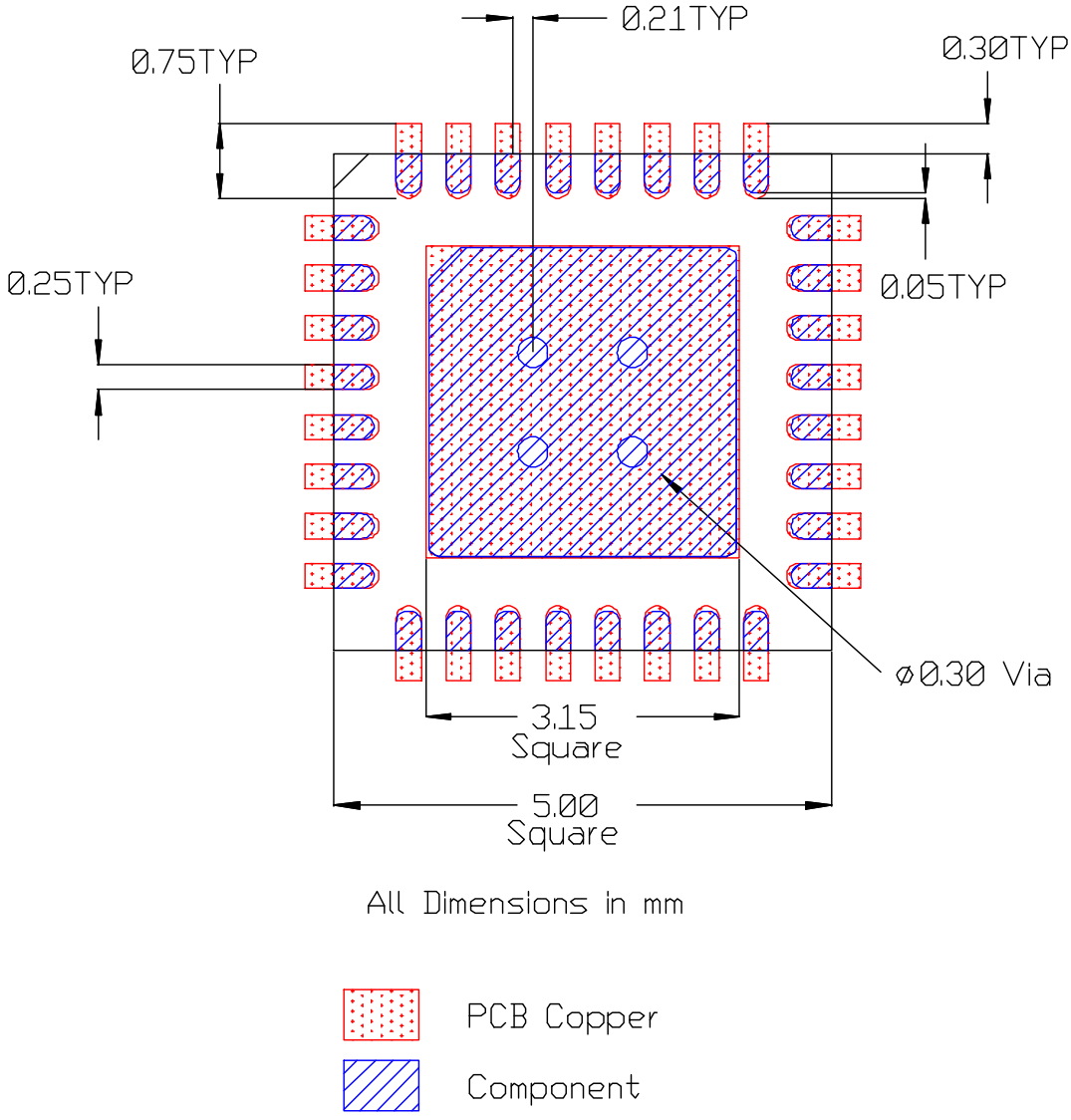
The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane LGND.
- Since, the centre pad under the IC is the LGND, connect it to the ground plane through at least 4 vias to reduce the routing lengths for components around the control IC
- Connect the ground tab under the control IC to LGND plane through a via.
- Place VCCL decoupling capacitor VCCL as close as possible to VCCL and LGND pins.
- Place the following critical components on the same layer as control IC and position them as close as possible to the respective pins, ROSC, RVDAC, CVDAC, and CSS/DEL. Avoid using any via for the connection.
- Place the compensation components on the same layer as control IC and position them as close as possible to EAOUT, FB, VO and VDRP pins. Avoid using any via for the connection.
- Use Kelvin connections for the remote voltage sense signals, VOSNS+ and VOSNS-, and avoid crossing over the fast transition nodes, i.e. switching nodes, gate drive signals and bootstrap nodes.
- Avoid analog control bus signals, VDAC, IIN, and especially EAOUT, crossing over the fast transition nodes.
- Separate digital bus, CLKOUT, PHSIN and PHSOUT from the analog control bus and other compensation components.



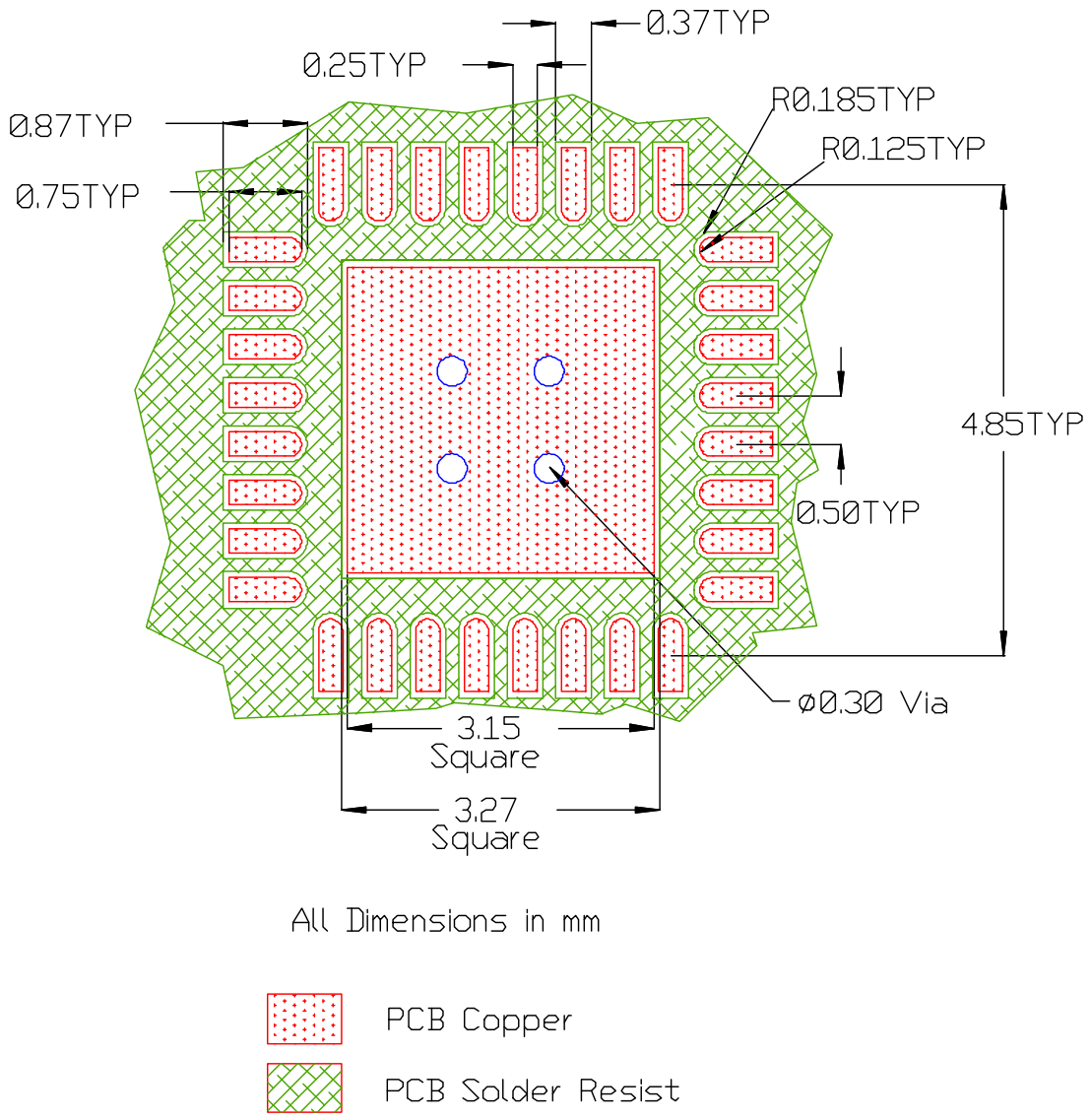
PCB Metal and Component Placement

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- At least four 0.30mm diameter vias shall be placed in the center of the pad land and connected to ground to reduce the routing lengths for all the components around the control IC.
- No PCB traces should be routed nor vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the PCB resulting in poor solder joints to the IC leads.



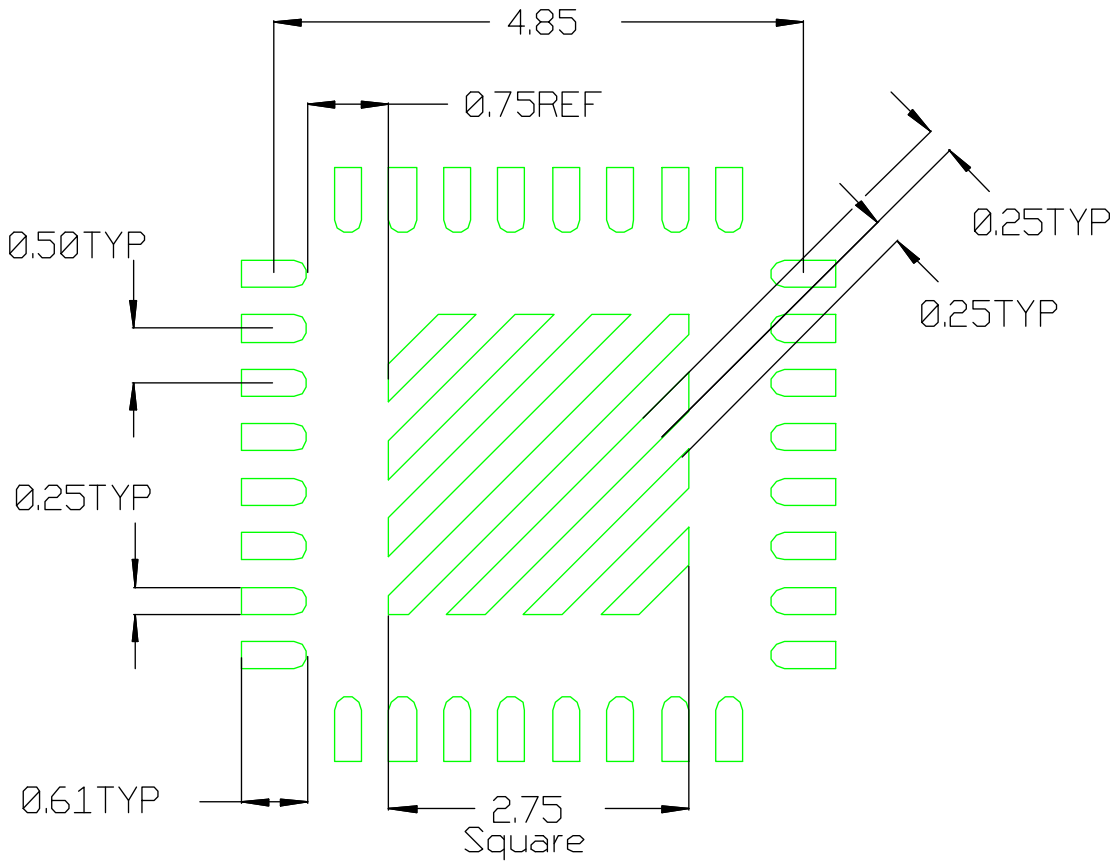
Solder Resist

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The vias in the land pad should be tented or plugged from bottom board side with solder resist.



Stencil Design

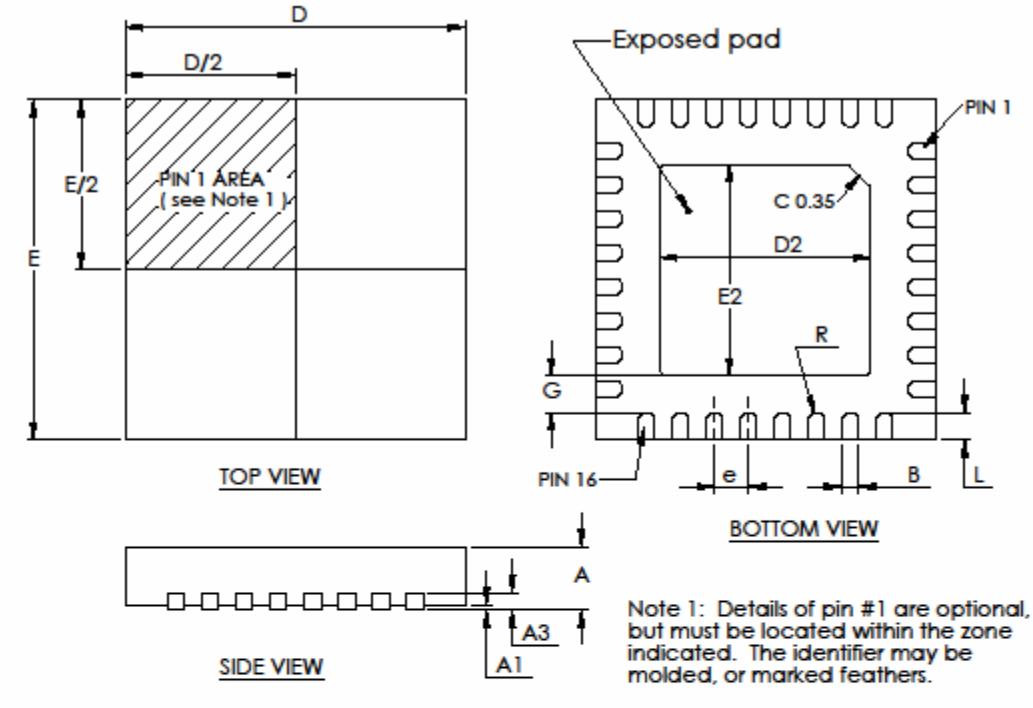
- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm

PACKAGE INFORMATION

32L MLPQ (5 x 5 mm Body) – θ_{JA} = 33 °C/W, θ_{JC} =2.4 °C/W



32-PIN 5x5 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0.00		0.05
A3	0.20 REF		
B	0.20	0.25	0.30
D	4.95	5.00	5.05
D2	3.00	3.10	3.20
E	4.95	5.00	5.05
E2	3.00	3.10	3.20
e	0.5 REF		
G	0.55 REF		
L	0.30	0.40	0.50
R	0.125 TYP		

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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