International
IOR Rectifier

REFERENCE DESIGN IRDCiP2005A-A

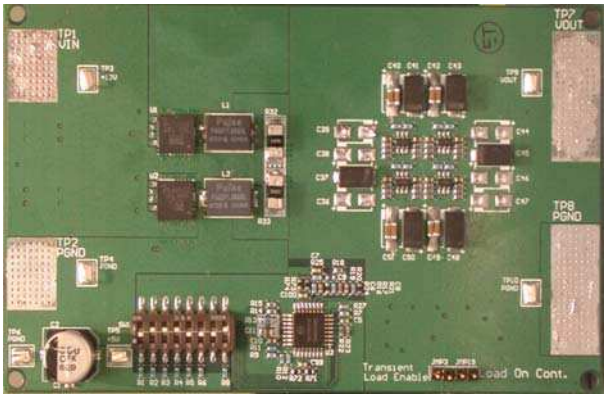
International Rectifier • 233 Kansas Street, El Segundo, CA 90245 USA

IRDCiP2005A-A: 1MHz, 65A DC, 80A Peak, Dual Phase, Sync Buck Converter using iP2005

iPOWIR™ TECHNOLOGY

Overview

This reference design is capable of delivering a current of 65A DC or 80A peak (with heatsink) at an ambient temperature of 45ºC and airflow of 300LFM. Figures 1–19 provide performance graphs, thermal images, and waveforms. The shunt resistors are added for load line preciseness and can be changed to DCR sensing for higher efficiency. Figures 19-23, and Table 1 are provided to engineers as design references for implementing a dual phase iP2005 solution. The components installed on this demo board were selected based on operation at an input voltage of 12V and at a switching frequency of 1MHz. Changes from these set points may require optimizing the control loop and/or adjusting the values of input/output filters in order to meet the user's specific application requirements. Refer to the iP2005 datasheet for more information.



Demo board Quick Start Guide

Initial Settings:

V_{OUT} is set to 1.25V, but can be adjusted from 0.8375V to 1.6V by changing the settings of VID0 through VID5 according to the OnSemi data sheet of NCP5318.

Power Up Procedure:

1. Apply drive power supply across Vdd and PGND.
2. Apply input voltage across VIN and PGND.
3. Turn on the enable signal through the DIP switch (SW1-pin 8).
4. Apply load and adjust to desired level. See recommendations below.
5. Install/uninstall a jumper to JMP3 to turn on and turn off current transient load (65A step)*

* Note: the transient current load is a resistive load and the voltage across it is measured instead of current due to ESL limitations. For more details, please refer to figure 11 through 15.

IRDCiP2005A-A Recommended Operating Conditions

(refer to the iP2005 datasheet for maximum operating conditions)

Input voltage:	9.5 – 13.2V
Output voltage:	0.8375 -1.6V
Switching Freq:	1MHz

Output current: This reference design is capable of delivering a continuous current of 65A (with heatsink) or 80A repetitive pulse current load (50A DC + 10% duty 30A DC) at an ambient temperature of 45ºC and an airflow of 300LFM.

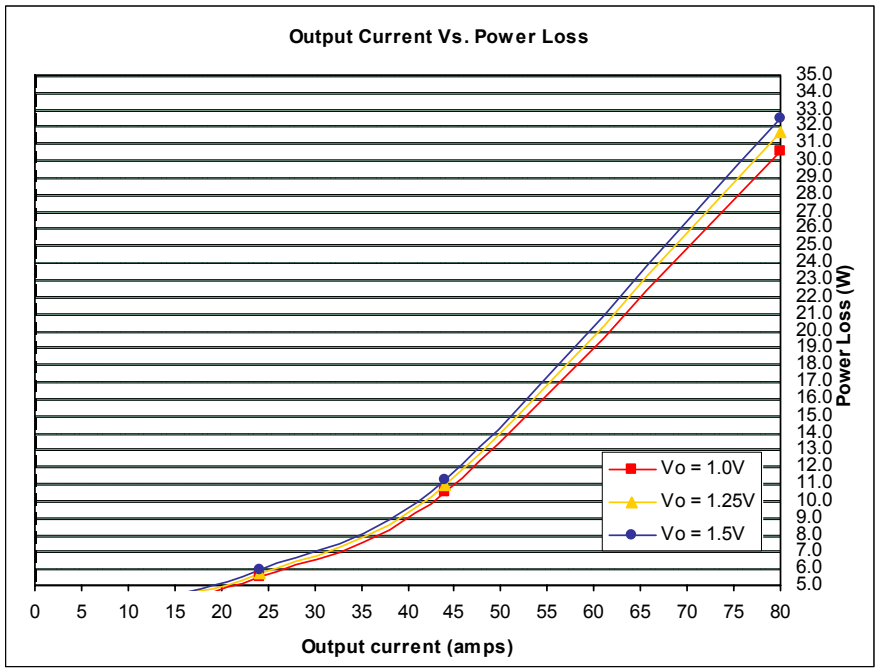


Fig. 1 Power Loss vs. Output Current for Vin=12V

Fsw=1MHz, Vdd=5V, Ta=45dgC, Airflow=300LFM, with Heat Sink

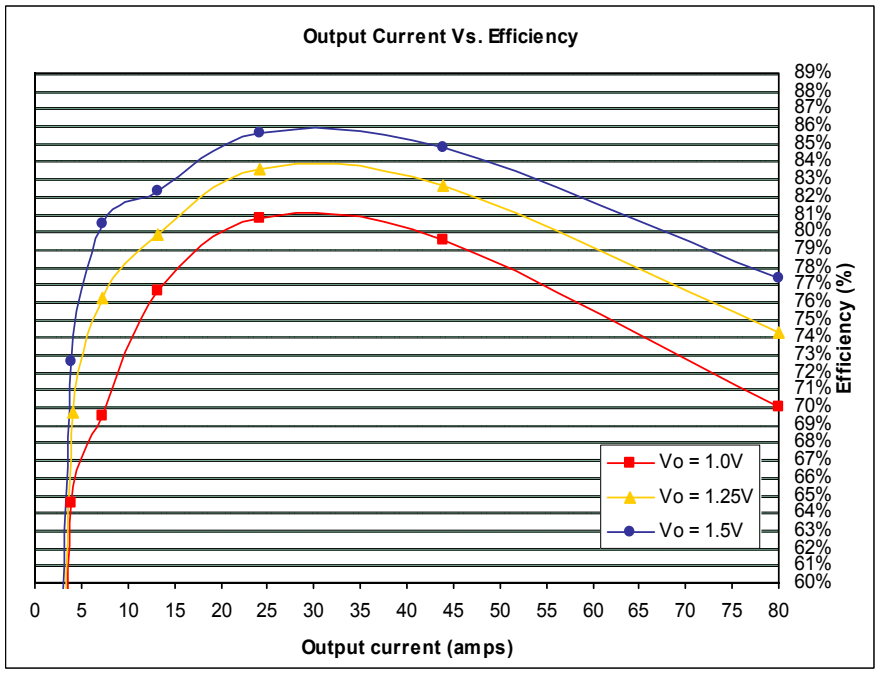


Fig. 2 Efficiency vs. Output Current for Vin=12V

Fsw=1MHz, Vdd=5V, Ta=45dgC, Airflow=300LFM, with Heat Sink

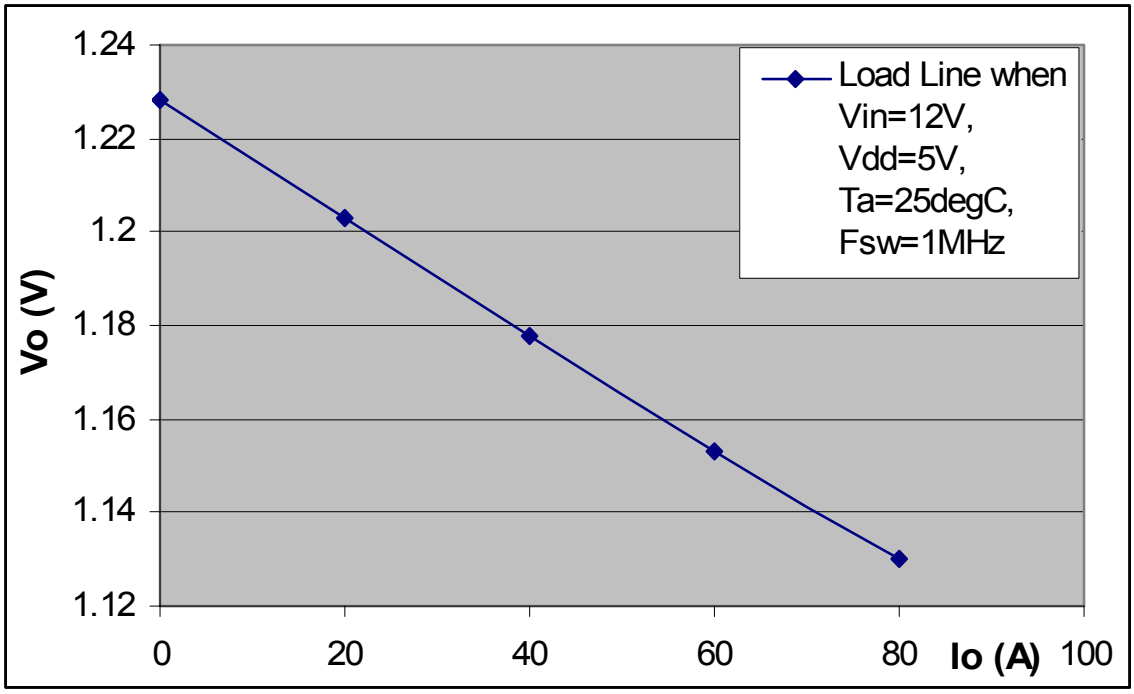


Fig. 3 Load Line R_{LL} = 1.2 mΩ

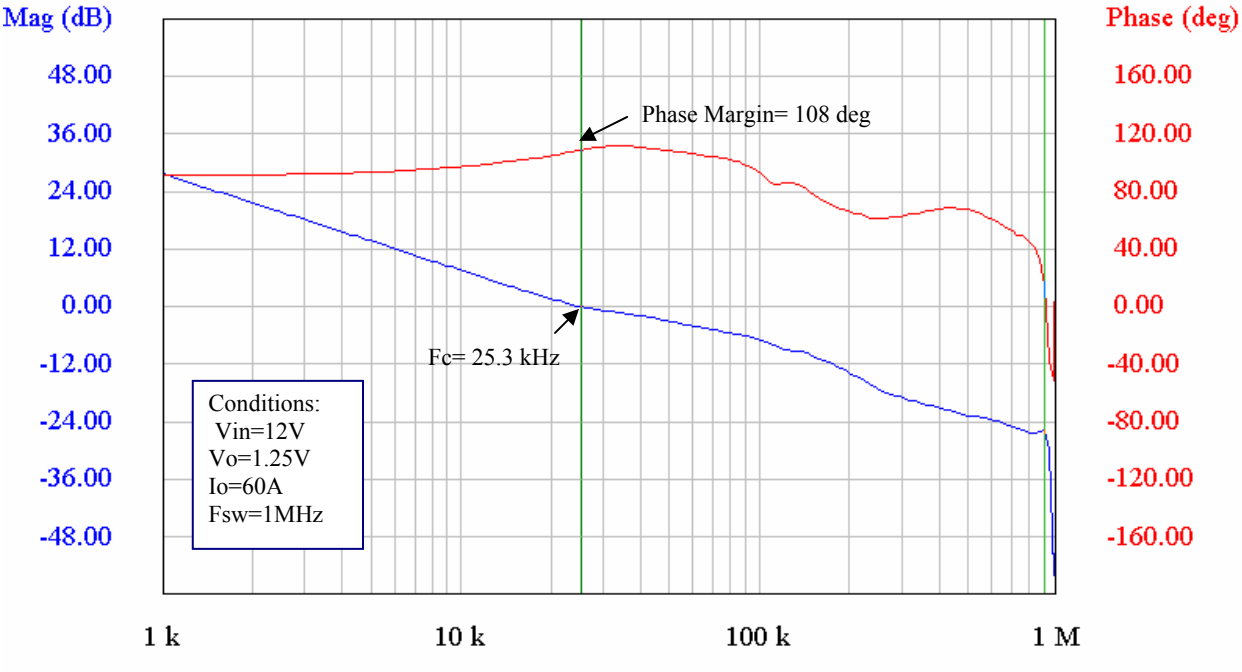


Fig. 4 Bode Plot

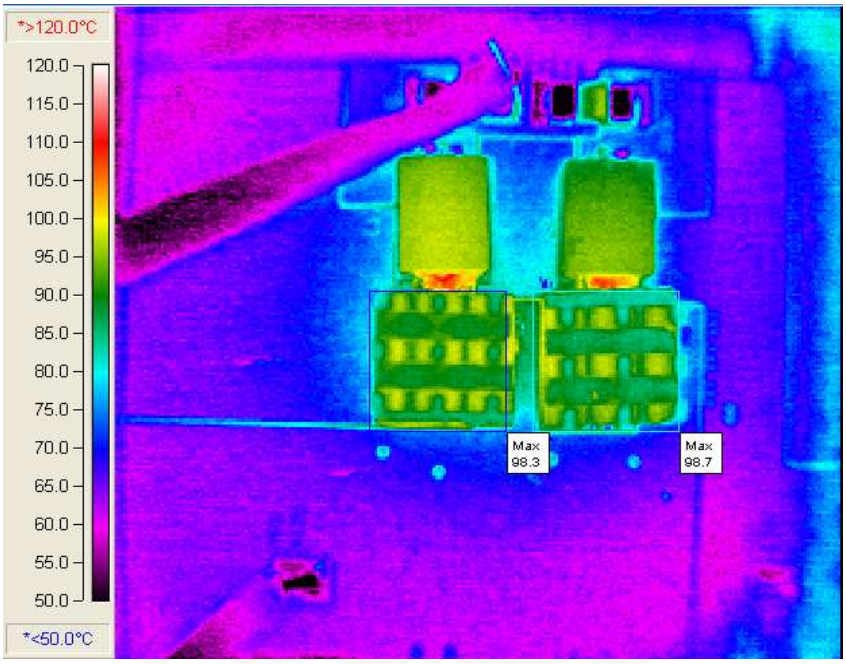


Fig. 5 Thermal Graph 1

Fsw=1MHz, Vdd=5V, Ta=45 ºC, Airflow=300LFM, Vin=12V, Vo=1.25V, Io=65A, with heat sink

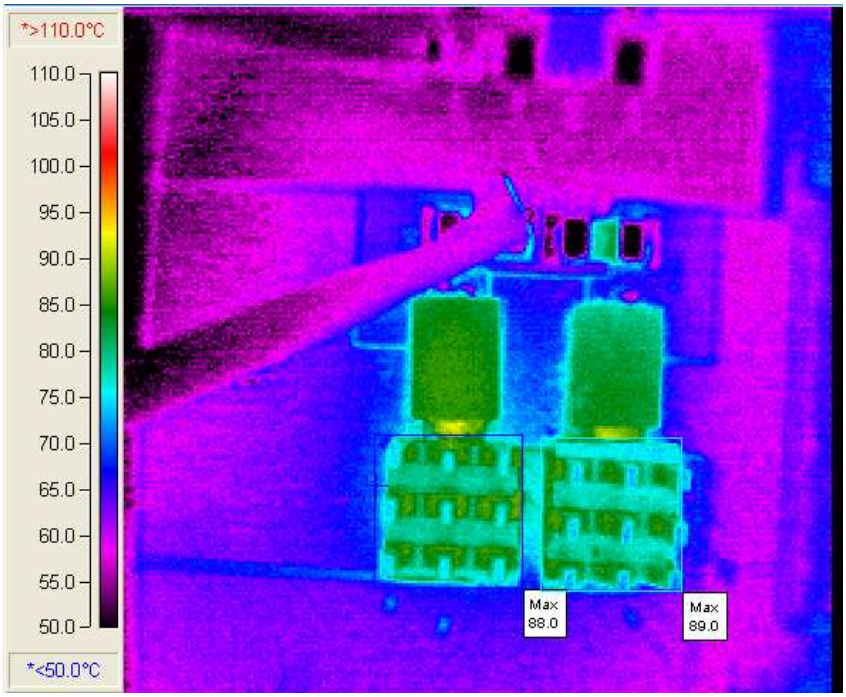


Fig. 6 Thermal Graph 2

Fsw=1MHz, Vdd=5V, Ta=45 ºC, Airflow=300LFM, Vin=12V, Vo=1.25V, Io=50A+30A (pulse), with heat sink

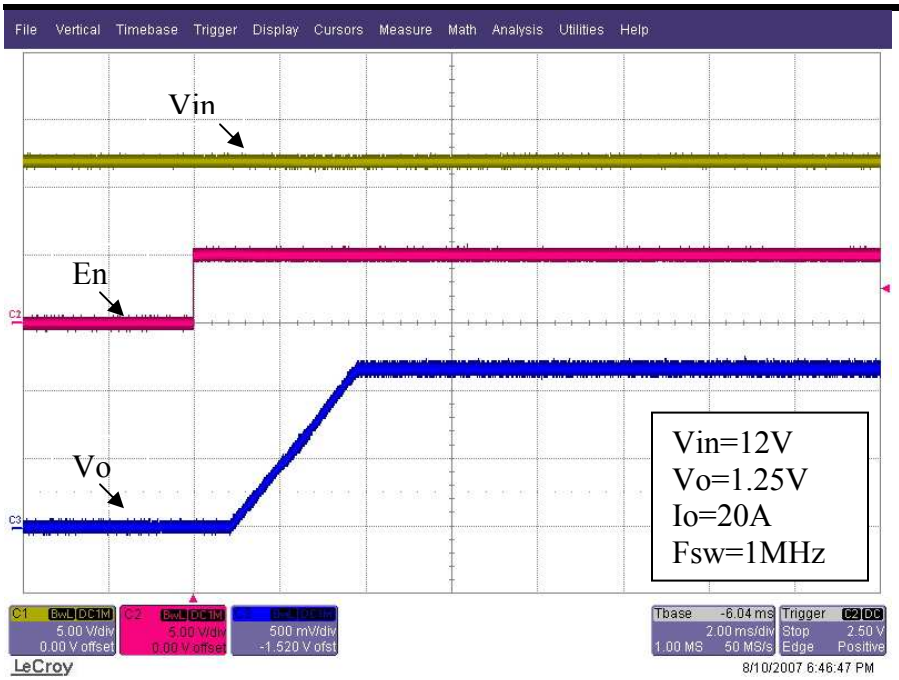


Fig. 7 Power-Up Sequence

Fig. 8 Power-Down Sequence

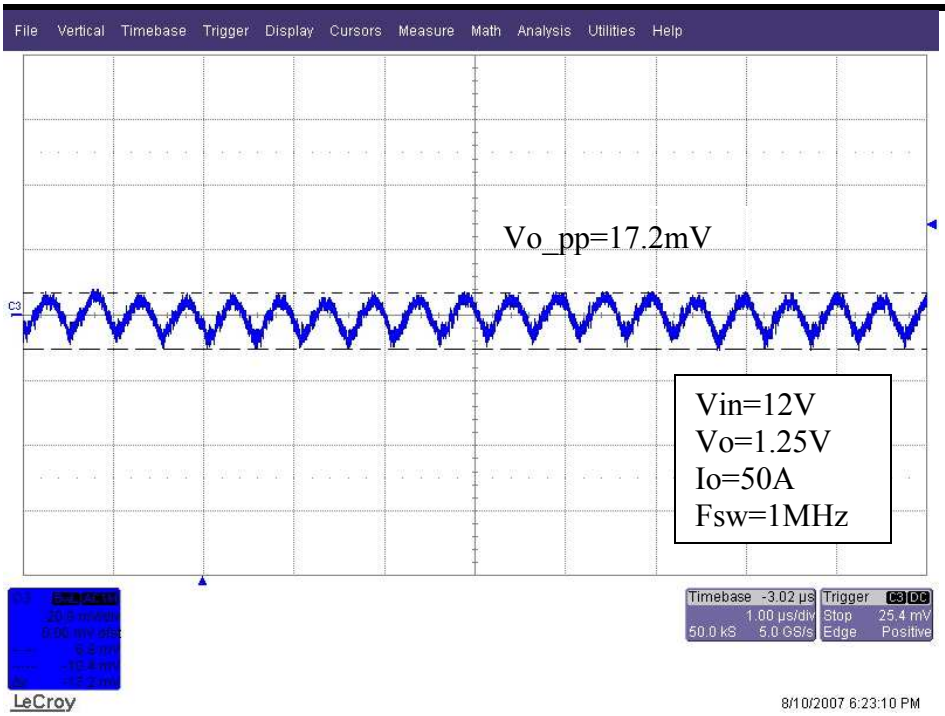


Fig. 9 Output Voltage Ripple

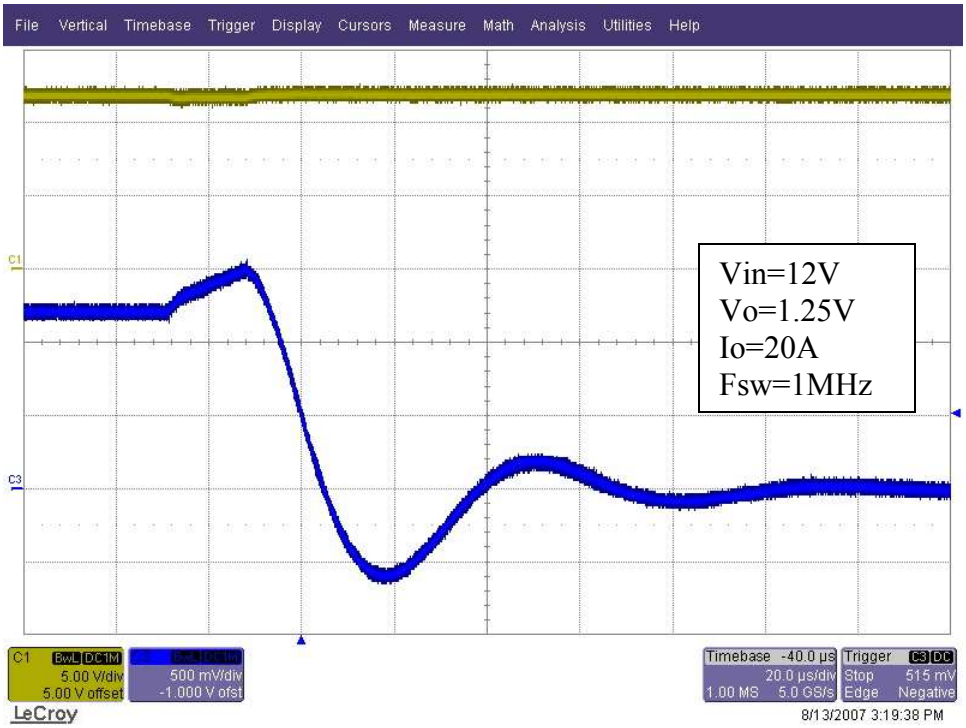


Fig. 10 Over-Voltage Protection

Transient Load Overview

Many of today's high performance CPU's can easily draw transient currents with slew rate greater than 1000A/µs. Unfortunately, replicating and demonstrating such a load event with such a high current slew rate on an evaluation board is not a trivial task. The smallest amount of stray inductance can quickly limit the slew rate of your load design and cause large voltage spikes. For example, a stray inductance of 30pH will create 30mV of over/undershoot for a given transient event with a slew rate of 1000A/µs. Such an over/undershoot may already exceed the amount of voltage variation allowed in your design. A new approach over a traditional load design needs to be implemented.

This reference design has an embedded load that is capable of delivering a 65A current step at slew rate of 1000A/µs. The load design uses a parallel network of very small, low charge MOSFETs, 0402 capacitors, and 0603 load resistors (see Figure 1). This new approach greatly minimizes the parasitic inductance through the use of low ESL components and by distributing the switching current amongst many high speed switching MOSFETs. The pulsed current is run at a duty cycle of less than 2% which results in very little power dissipation and minimal device temperature rise. The net result closely replicates the dynamic load response of a high performance CPU.

Validating the current waveform could only be done by measuring the voltage drop differentially across the load resistors during the switching event. Placing a current probe is not an option due to the ESL adder. Since the resistive load is a passive element, current flowing through the resistor is in phase with the voltage across the resistor. If the voltage across the resistive element changes at a rate of 1000V/µs, one can assume the current is changing at the same rate (1000A/µs).

Figures 12, 14 & 15 show the validation of the load design for this particular demonstration tool. Four MOSFETs stages were used to create a 65A load step at a minimum of slew rate of 1000A/µs. The parallel network of load resistors in this design creates an equivalent impedance of 9mΩ. Differentially measuring the voltage drop across the load resistors of each MOSFET stage yields a voltage change of approximately 0.575V. Using Ohm's law we approximately get 65A of total load current (see Figure 12). Zooming in at the rising and falling edges of the load step, we can then measure the slew rate of the load step. In this particular design, we are achieving about40ns rise and fall times for 40A change which translate to about 1000A/µs (see Figures 14 & 15).

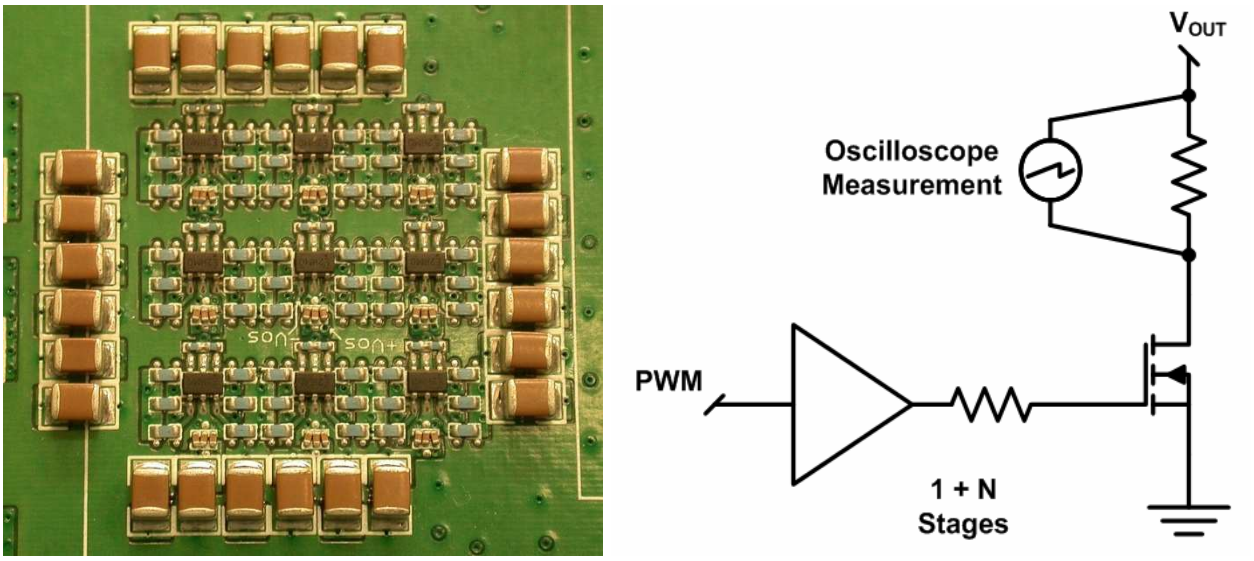


Fig. 11 Embedded High Slew Rate Load Design

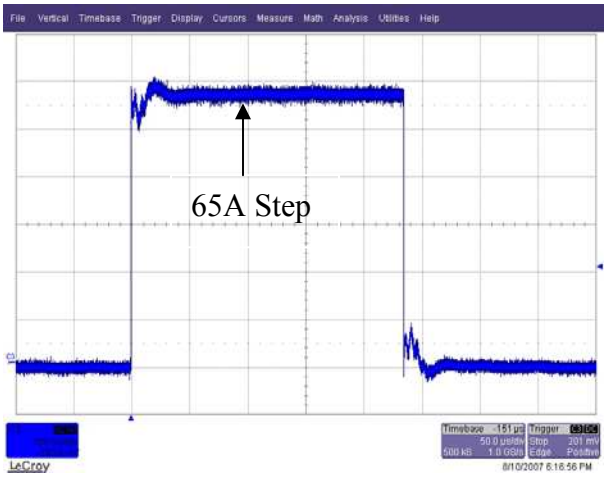


Fig. 12 Transient Load Current

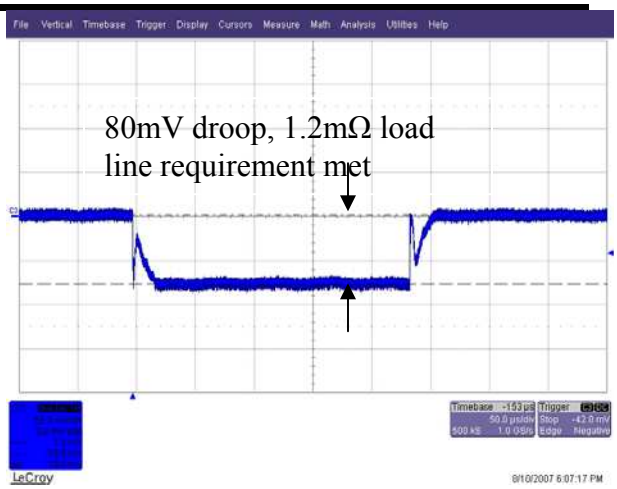


Fig. 13 Vout under Transient Load

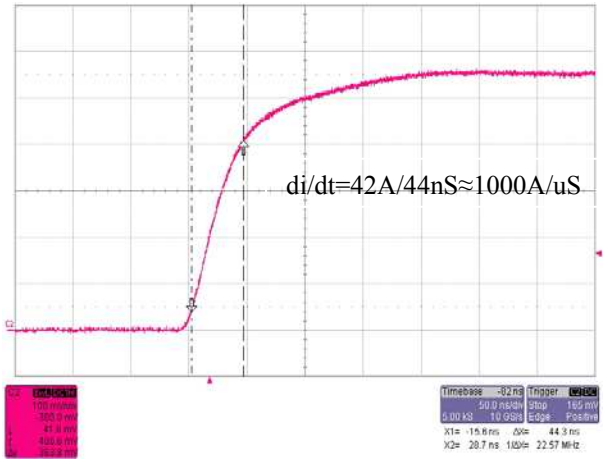


Fig. 14 Zoom-in rising edge of load

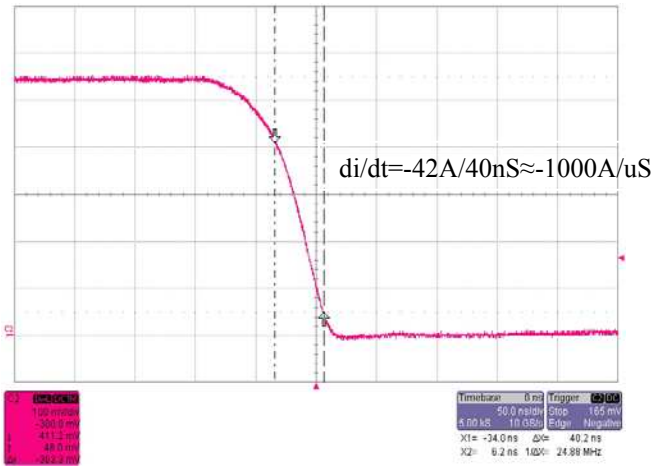


Fig. 15 Zoom-in falling edge of load

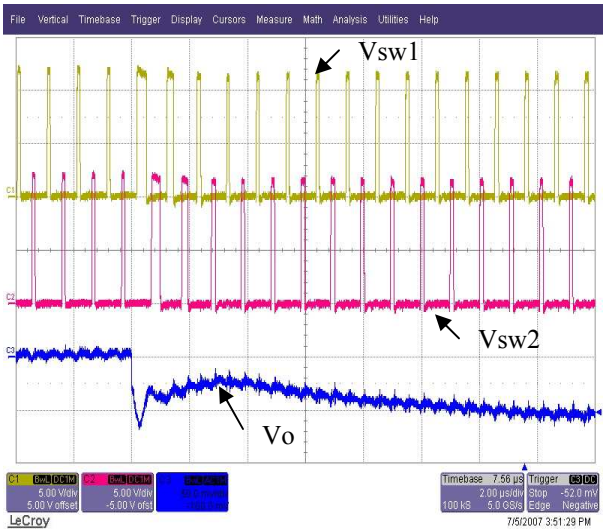


Fig. 16 Transient load step-up

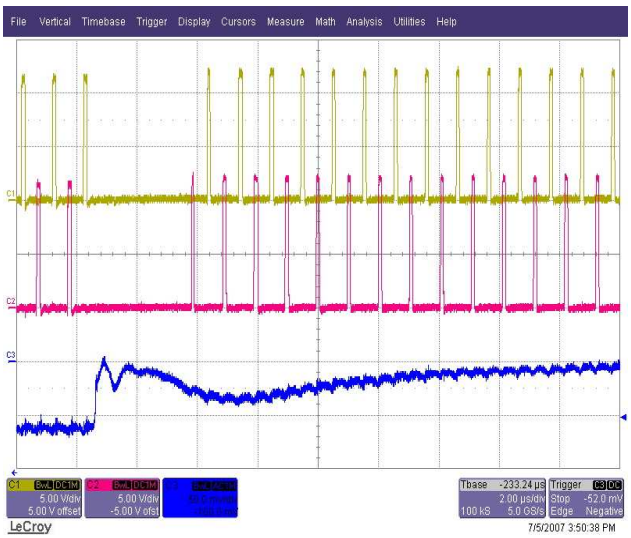


Fig. 17 Transient load step-down

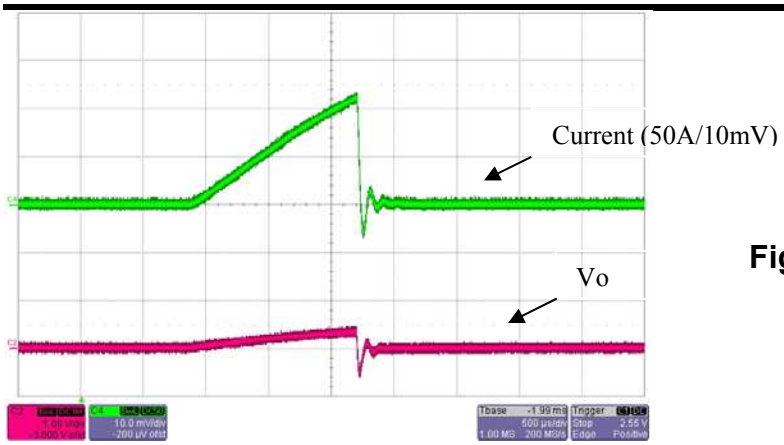


Fig. 18 Over-Current Protection

Adjusting the Over-Current Limit

R10 and R12 are the resistors used to adjust the over-current trip point. The trip point corresponds to the peak inductor current, refer to equation below to determine R10 and R12 values given the over current limit:

$$R10+R12 = (70.5 \times I_{Limit} - 90)\ ohm$$

More details can be found in On-Semi data sheet of NCP5318.

Mechanical Drawings

Fig. 19 Heat Sink Photo

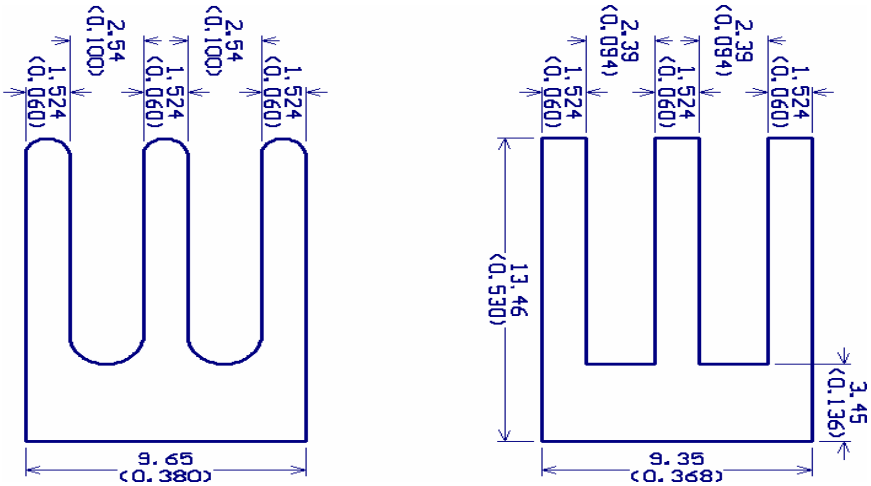


Fig. 20 Mechanical Outline Drawing of Heatsink

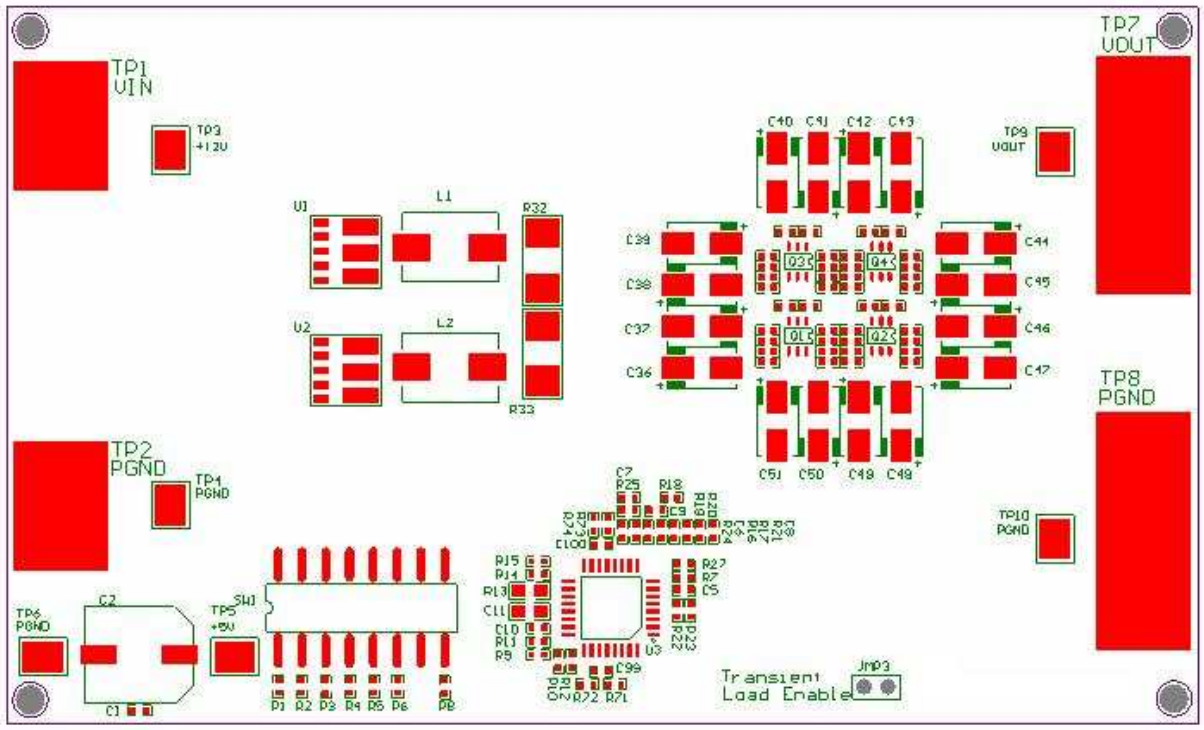


Fig. 21 Top Layer View

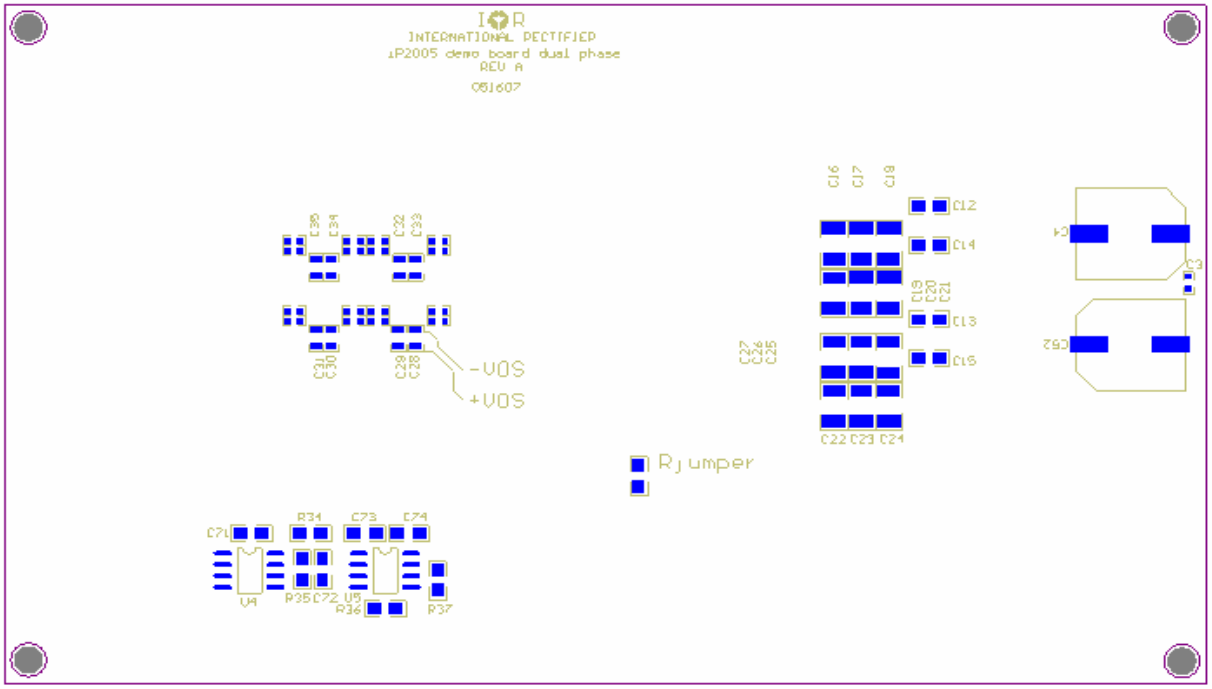


Fig. 22 Bottom Layer View

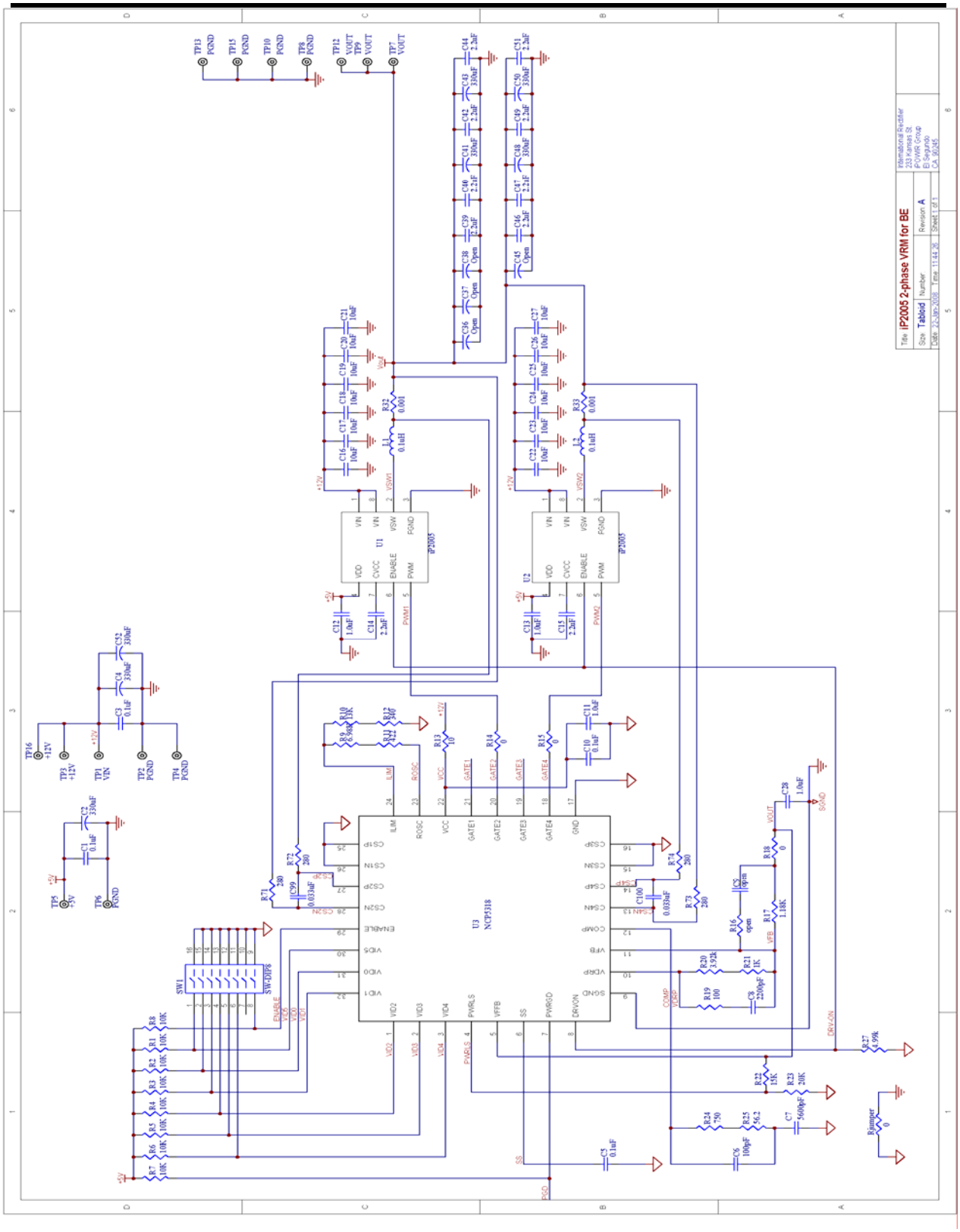


Fig. 23 Reference Design Schematic

Quantity	Designator	Type 1	Type 2	Value 1	Value 2	Tolerance	Package	Manufac 1	Manufac 1No
4	C1,C10, C3, C5	capacitor	X7R	0.100uF	50V	10%	0603	TDK	C1608X7R1H104K
11	C11, C12, C13, C28, C29, C30, C31, C32, C33, C34, C35	capacitor	X7R	1.00uF	16V	10%	0805	MuRata	GRM40X7R105K016
2	C14, C15	capacitor	X7R	2.20uF	16V	10%	0805	TDK	C2012X7R1C225K
12	C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27	capacitor	X7R	10.0uF	16V	20%	1210	TDK	C3225X7R1C106M
3	C2, C4, C53	capacitor	polymer	330uF	16V	20%	SMD	United Chemi-Con	APXA160ARA331MJC0S
20	C36, C37, C38, C45, C9, R16, TP1, TP10, TP12, TP13, TP15, TP16, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	open	-	-	-	-	-	-	-
8	C39, C40, C42, C44, C46, C47, C49, C51	capacitor	X7R	2.20uF	16V	10%	1206	MuRata	GRM31MR71C225KC11L
4	C41, C43, C48, C50	capacitor	tantalum	330uF	2V	20%	7343	Panasonic	EEFSX0D331XE
1	C6	capacitor	NPO	100pF	50V	5%	0603	Phycomp	0603CG101J9B20
1	C7	capacitor	X7R	5600pF	50V	10%	0603	KOA	X7R0603HTTD562K
1	C8	capacitor	COG	2200pF	50V	5%	0603	TDK	C1608C0G1H222J
2	C99,C100	capacitor	X7R	0.033uF	16V	10%	0603	KOA	X7R0603HTTD333K
1	JMP3	hardware	test point	233 mils	40 mils	-	2 pin	Samtec	TSW-102-08-LS
2	L1,L2	inductor	ferrite	0.10uH	80A	20%	SMD	Pulse	PA0511.900NL
8	R1, R2, R3, R4, R5, R6, R7, R8	resistor	thick film	10.0K	1/10W	1%	0603	KOA	RK73H1JU002F
1	R27	resistor	thick film	4.99K	1/10W	1%	0603	Phycomp	9C06031A4991FKRFT
1	R10	resistor	thick film	13.0K	1/10W	1%	0603	KOA	RK73H1JLTD1302F
1	R11	resistor	thick film	422	1/10W	1%	0603	KOA	RK73H1JLTD4220F
1	R12	resistor	thick film	340	1/10W	1%	0603	KOA	RK73H1JLTD3400F
1	R13	resistor	thick film	10	1/8W	1%	0805	KOA	RK73H2A10R0F
3	R14, R15, R18	resistor	thick film	0	1/10W	1%	0603	KOA	RK7321JLTD
1	Rjumper	resistor	thick film	0	1/10W	<50m	0805	KOA	MCR10EZHJ000
1	R17	resistor	thick film	1.18K	1/10W	1%	0603	KOA	RK73H1JLTD1181F
1	R20	resistor	thick film	3.92K	1/10W	1%	0603	KOA	RK73H1JU392F
1	R21	resistor	thick film	1.00K	1/10W	1%	0603	KOA	RK73H1JU001F
1	R22	resistor	thick film	15.0K	1/10W	1%	0603	KOA	RK73H1JU502F
1	R23	resistor	thick film	20.0K	1/10W	1%	0603	KOA	RK73H1J2002F
1	R24	resistor	thick film	750	1/10W	1%	0603	KOA	RK73H1JLTD7500F
1	R25	resistor	thick film	56.2	1/10W	1%	0603	KOA	RK73H1JLTD56R2F
2	R32, R33	resistor	alloy metal	1.00m	1W	1%	2512	Panasonic	ERJM1WTF1M0U
1	R19	resistor	thick film	100	1/10W	1%	0603	KOA	RK73H1JU000F
1	R9	resistor	thick film	6.98K	1/10W	1%	0603	KOA	RK73H1JLTD698IF
1	SW1	switch	DIP	SPST	8 position	-	SMT	C&K Components	SD08H0SK
2	U1, U2	iP2005						International Rectifier	
1	U3	IC	Control	VRM10.1		0.50%	LQFP-32	On Semiconductor	NCP5318FTR2G

Table 1: Reference Design Bill of Materials

Refer to the following documents for more details and guidelines detailed guidelines for design:

iP2005A datasheet: Specifications and user guides about International Rectifier's integrated power modules used in this reference design

NCP5318 datasheet: Specifications and user guides about the On-Semi multiphase buck controller used in this reference design

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPowIR Technology BGA and LGA and Packages
This paper discusses optimization of the layout design for mounting iPowIR BGA and LGA packages on printed circuit boards, accounting for thermal and electrical performance and assembly considerations. Topics discussed includes PCB layout placement, and via interconnect suggestions, as well as soldering, pick and place, reflow, inspection, cleaning and reworking recommendations.

AN-1030: Applying iPOWIR Products in Your Thermal Environment
This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

AN-1047: Graphical solution for two branch heatsinking Safe Operating Area
Detailed explanation of the dual axis SOA graph and how it is derived.

Use of this design for any application should be fully verified by the customer. International Rectifier cannot guarantee suitability for your applications, and is not liable for any result of usage for such applications including, without limitation, personal or property damage or violation of third party intellectual property rights.

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