

IR2133/IR2135(J&S)&(PbF) IR2233/IR2235(J&S)&(PbF)

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V or +1200V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10V/12V to 20V DC and
up to 25V for transient
- Undervoltage lockout for all channels
- Over-current shut down turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- All parts are also available LEAD-FREE

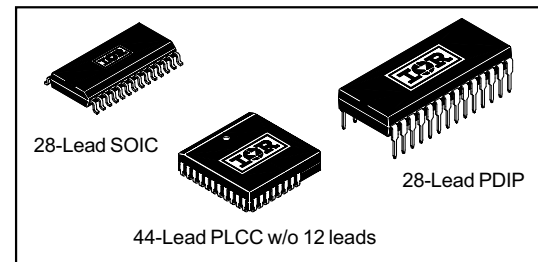
Description

The IR2133/IR2135/IR2233/IR2355 (J&S) are high voltage, high speed power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. An independent operational amplifier provides an analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs can also be derived from this resistor. A shutdown function is available to terminate all six outputs. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current or undervoltage shutdown has occurred. Fault conditions are cleared with the $\overline{\text{FLT-CLR}}$ lead. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts or 1200 volts.

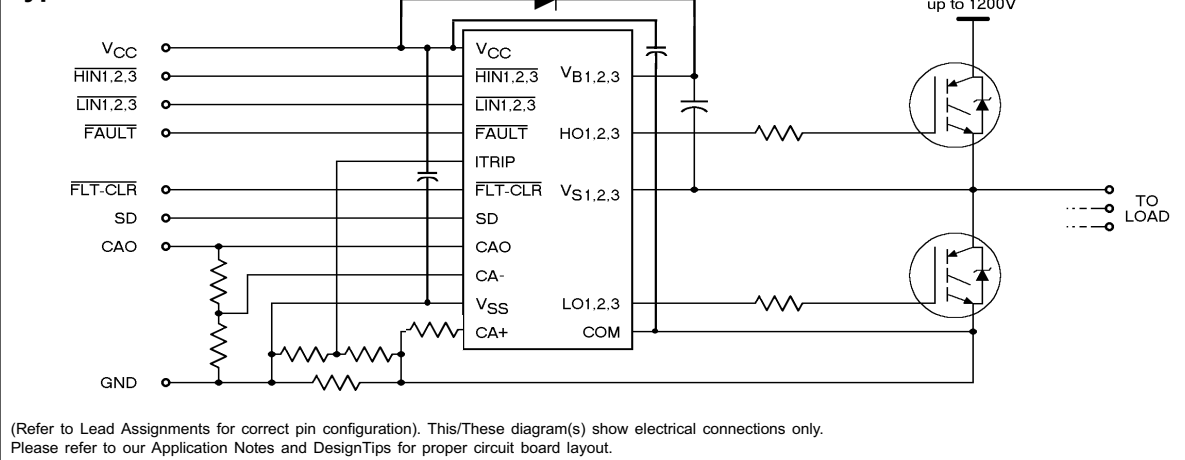
Product Summary

V_{OFFSET}	600V or 1200V max.
$I_{\text{O}+/-}$	200 mA / 420 mA
V_{OUT}	10 - 20V or 12 - 20V
$t_{\text{on/off (typ.)}}$	750/700 ns
Deadtime (typ.)	250 ns

Packages



Typical Connection



IR2133/IR2135/IR2233/IR2235(J&S)&(PbF)

International
IR Rectifier

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _{B1,2,3}	High side floating supply voltage	(IR2133/IR2135)	-0.3	625	V
		(IR2233/IR2235)	-0.3	1225	
V _{S1,2,3}	High side floating supply offset voltage	V _{B1,2,3} - 25	V _{B1,2,3} + 0.3		
V _{HO1,2,3}	High side floating output voltage	V _{S1,2,3} - 0.3	V _{B1,2,3} + 0.3		
V _{CC}	Fixed supply voltage	-0.3	25		
V _{SS}	Logic ground	V _{CC} - 25	V _{CC} + 0.3		
V _{LO1,2,3}	Low side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage ($\overline{\text{HIN}}$, $\overline{\text{LIN}}$, ITRIP, SD & $\overline{\text{FLT-CLR}}$)	V _{SS} - 0.3	(V _{SS} + 15) or (V _{CC} + 0.3) whichever is lower		
V _{IN,AMP}	Op amp input voltage (CA+ & CA-)	V _{SS} - 0.3	V _{CC} + 0.3		
V _{OUT,AMP}	Op amp output voltage (CAO)	V _{SS} - 0.3	V _{CC} + 0.3		
V _{FLT}	FAULT output voltage	V _{SS} - 0.3	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ 25°C	(28 Lead PDIP)	—	1.5	W
		(28 Lead SOIC)	—	1.6	
		(44 lead PLCC)	—	2.0	
R _{thJA}	Thermal resistance, junction to ambient	(28 Lead PDIP)	—	83	°C/W
		(28 Lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T _J	Junction temperature	—	125	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The VS offset rating is tested with all supplies biased at 15V differential.

Symbol	Parameter Definition	Min.	Max.	Units	
V _{B1,2,3}	High side floating supply voltage	V _{S1,2,3} + 10/12	V _{S1,2,3} + 20	V	
V _{S1,2,3}	High side floating supply offset voltage	(IR2133/IR2135)	Note 1		600
		(IR2233/IR2235)	Note 1		1200
V _{HO1,2,3}	High side floating output voltage	V _{S1,2,3}	V _{B1,2,3}		
V _{CC}	Fixed supply voltage	10 or 12	20		
V _{SS}	Low side driver return	-5	5		
V _{LO1,2,3}	Low side output voltage	0	V _{CC}		
V _{IN}	Logic input voltage ($\overline{\text{HIN}}$, $\overline{\text{LIN}}$, ITRIP, SD & $\overline{\text{FLT-CLR}}$)	V _{SS}	V _{SS} + 5		
V _{IN,AMP}	Op amp input voltage (CA+ & CA-)	V _{SS}	V _{SS} + 5		
V _{OUT,AMP}	Op amp output voltage (CAO)	V _{SS}	V _{SS} + 5		
V _{FLT}	FAULT output voltage	V _{SS}	V _{CC}		

Note 1: Logic operational for V_S of COM - 5V to COM + 600V/1200V. Logic state held for V_S of COM -5V to COM -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins, op amp input and output pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS1,2,3}) = 15V, V_{S1,2,3} = V_{SS}, T_A = 25°C and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t _{on}	Turn-on propagation delay	500	750	1000	ns	V _{IN} = 0 & 5V V _{S1,2,3} = 0 to 600V or 1200V
t _{off}	Turn-off propagation delay	450	700	950		
t _r	Turn-on rise time	—	90	150		
t _f	Turn-off fall time	—	40	70		
t _{sd}	SD to output shutdown propagation delay	500	750	1000		
t _{itrip}	ITRIP to output shutdown propagation delay	600	850	1100		
t _{bl}	ITRIP blanking time	—	400	—		
t _{flt}	ITRIP to $\overline{\text{FAULT}}$ propagation delay	400	650	900		
t _{fil,in}	Input filter time (HIN, LIN and SD)	—	310	—		
t _{fltclr}	FLT-CLR to $\overline{\text{FAULT}}$ clear time	600	850	1100		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on	100	250	400	V/μs	V _{IN} , V _{ITRIP} = 0 & 5V
SR+	Amplifier slew rate (positive)	5	10	—		V _{IN} , V _{ITRIP} = 0 & 5V
SR-	Amplifier slew rate (negative)	2	2.5	—		V _{IN} = 0 & 5V

NOTE: For high side PWM, HIN pulse width must be ≥ 1μ sec

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS1,2,3}) = 15V unless otherwise specified and T_A = 25°C. All static parameters other than IO and VO are referenced to V_{SS} and are applicable to all six channels (H_{S1,2,3} & L_{S1,2,3}). The VO and IO parameters are referenced to COM and V_{S1,2,3} and are applicable to the respective output leads: H_{O1,2,3} or L_{O1,2,3}.

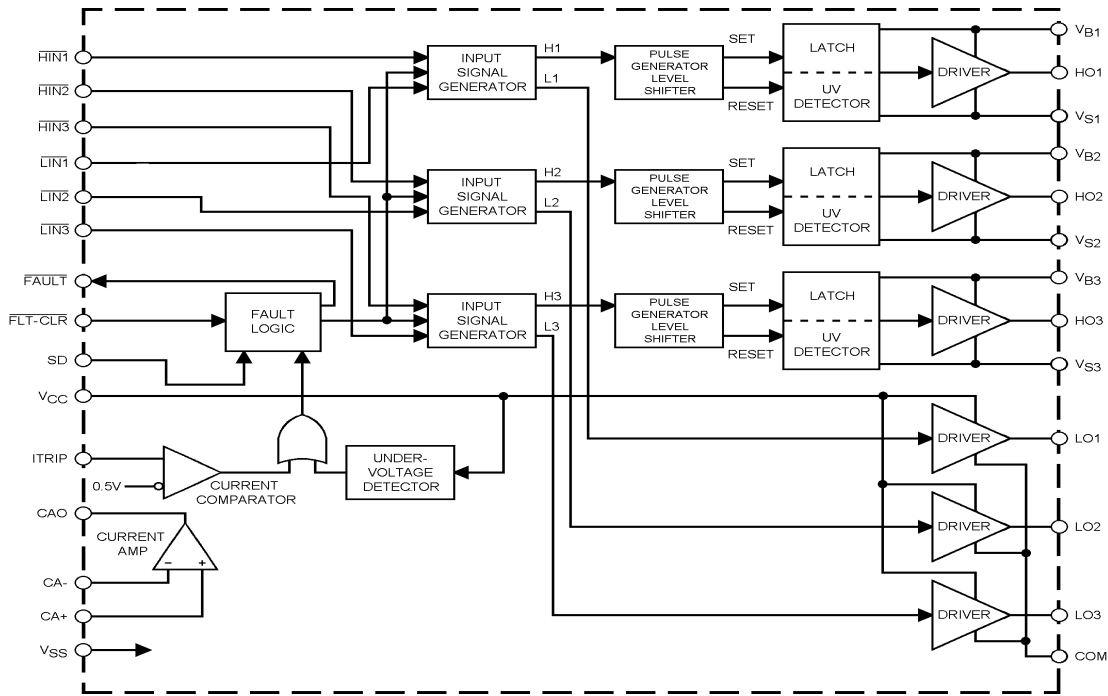
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V _{IH}	Logic "0" Input Voltage (OUT = LO)	2.2	—	—	V	
V _{IL}	Logic "1" Input Voltage (OUT = HI)	—	—	0.8		
V _{FCLR,IH}	Logic "0" Fault Clear Input Voltage	2.2	—	—		
V _{FCLR,IL}	Logic "1" Fault Clear Input Voltage	—	—	0.8		
V _{SD,TH+}	SD Input Positive Going Threshold	1.6	1.9	2.2		
V _{SD,TH-}	SD Input Negative Going Threshold	1.4	1.7	2.0		
V _{IT,TH+}	ITRIP Input Positive Going Threshold	470	570	670	mV	
V _{IT,TH-}	ITRIP Input Negative Going Threshold	360	460	560		
V _{OH}	High Level Output Voltage, V _{BIAS} - V _O	—	—	100	mV	V _{IN} = 0V, I _O = 0A
V _{OL}	Low Level Output Voltage, V _O	—	—	100		V _{IN} = 5V, I _O = 0A
I _{LK}	Offset Supply Leakage Current (IR2133/IR2135)	—	—	50	μA	V _{B1,2,3} =V _{S1,2,3} = 600V
		(IR2233/IR2235)	—	—		50
I _{QBS}	Quiescent V _{BS} Supply Current	—	50	100	mA	V _{IN} = 0V or 5V
I _{QCC}	Quiescent V _{CC} Supply Current	—	4	8		V _{IN} = 0V or 5V
I _{IN+}	Logic "1" Input Bias Current (OUT = HI)	—	200	350	μA	V _{IN} = 0V
I _{IN-}	Logic "0" Input Bias Current (OUT = LO)	—	100	250		V _{IN} = 5V
I _{SD+}	"High" Shutdown Bias Current	—	30	100	nA	SD = 5V
I _{SD-}	"Low" Shutdown Bias Current	—	—	100		SD = 0V
I _{ITRIP+}	"High" ITRIP Bias Current	—	30	100	μA	I _{ITRIP} = 5V
I _{ITRIP-}	"Low" ITRIP Bias Current	—	—	100		I _{ITRIP} = 0V

Static Electrical Characteristics — Continued

V_{BIAS} (V_{CC}, V_{BS1,2,3}) = 15V unless otherwise specified and T_A = 25°C. All static parameters other than IO and VO are referenced to V_{SS} and are applicable to all six channels (H_{S1,2,3} & L_{S1,2,3}). The VO and IO parameters are referenced to COM and V_{S1,2,3} and are applicable to the respective output leads: H_{O1,2,3} or L_{O1,2,3}.

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions
I _{FLTCLR+}	"High" Fault Clear Input Bias Current	—	200	350	μA	$\overline{\text{FLT-CLR}} = 0\text{V}$
I _{FLTCLR-}	"Low" Fault Clear Input Bias Current	—	100	250		$\overline{\text{FLT-CLR}} = 5\text{V}$
V _{BSUV+}	V _{BS} Supply Undervoltage Positive Going Threshold (for IR2133/IR2233)	7.6	8.6	9.6	V	
		(for IR2135/IR2235)	9.2	10.4		
V _{BSUV-}	V _{BS} Supply Undervoltage Negative Going Threshold (for IR2133/IR2233)	7.2	8.2	9.2		
		(for IR2135/IR2235)	8.3	9.4		
V _{BSUVH}	V _{BS} Supply Undervoltage Lockout Hysteresis (for IR2133/IR2233)	—	0.4	—		
		(for IR2135/IR2235)	—	1		
V _{CCUV+}	V _{CC} Supply Undervoltage Positive Going Threshold (for IR2133/IR2233)	7.6	8.6	9.6		
		(for IR2135/IR2235)	9.2	10.4		
V _{CCUV-}	V _{CC} Supply Undervoltage Negative Going Threshold (for IR2133/IR2233)	7.2	8.2	9.2		
		(for IR2135/IR2235)	8.3	9.4		
V _{CCUVH}	V _{CC} Supply Undervoltage Lockout Hysteresis (for IR2133/IR2233)	—	0.4	—		
		(for IR2135/IR2235)	—	1		
R _{on,FLT}	FAULT- Low On Resistance	—	70	100	Ω	
I _{o+}	Output High Short Circuit Pulsed Current	200	250	—	mA	V _{OUT} = 0V, V _{IN} = 0V PW ≤ 10 μs
I _{o-}	Output Low Short Circuit Pulsed Current	420	500	—		V _{OUT} = 15V, V _{IN} = 5V PW ≤ 10 μs
V _{OS}	Amplifier Input Offset Voltage	—	0	30	mV	CA+ = 0.2V, CA- = CAO
I _{IN,AMP}	Amplifier Input Bias Current	—	—	4	nA	CA+ = CA- = 2.5V
CMRR	Amplifier Common Mode Rejection Ratio	50	70	—	dB	CA+ = 0.1V & 5V, CA- = CAO
PSRR	Amplifier Power Supply Rejection Ratio	50	70	—		CA+ = 0.2V, CA- = CAO V _{CC} = 10V & 20V
V _{OH,Amp}	Amplifier High Level Output Voltage	5	5.2	5.4	V	CA+ = 1V, CA- = 0V
V _{OL,Amp}	Amplifier Low Level Output Voltage	—	—	20	mV	CA+ = 0V, CA- = 1V
I _{SRC,Amp}	Amplifier Output Source Current	4	7	—	mA	CA+ = 1V, CA- = 0V, CAO = 4V
I _{SNK,Amp}	Amplifier Output Sink Current	0.5	1	—		CA+ = 0V, CA- = 1V, CAO = 2V
I _{o+,Amp}	Amplifier Output High Short Circuit Current	—	10	—		CA+ = 5V, CA- = 0V, CAO = 0V
I _{o-,Amp}	Amplifier Output Low Short Circuit Current	—	4	—		CA+ = 0V, CA- = 5V, CAO = 5V

Functional Block Diagram



Lead Definitions

Symbol	Lead Description
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase.
LIN1,2,3	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase.
FAULT	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic.
Vcc	Logic and low side fixed supply.
ITRIP	Input for over-current shut down.
FLT-CLR	Logic input for fault clear, negative logic.
SD	Logic input for shut down.
CAO	Output of current amplifier.
CA-	Negative input of current amplifier.
CA+	Positive input of current amplifier.
Vss	Logic ground.
COM	Low side return.
VB1,2,3	High side floating supplies.
HO1,2,3	High side gate drive outputs.
VS1,2,3	High side floating supply returns.
LO1,2,3	Low side gate drive outputs

Lead Assignments

<p>28 Lead DIP</p>	<p>44 Lead PLCC w/o 12 Leads</p>	<p>28 Lead SOIC (Wide Body)</p>
<p>IR2133 IR2135</p>	<p>IR2133J IR2135J IR2233J IR2235J</p>	<p>IR2133S IR2135S IR2233S IR2235S</p>
<p>Part Number</p>		

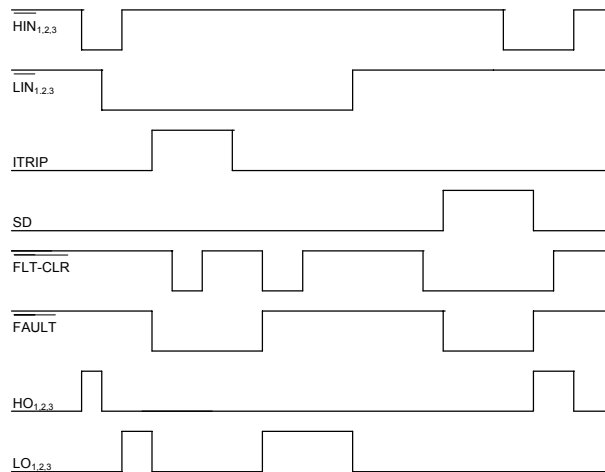


Figure 1. Input/Output Timing Diagram

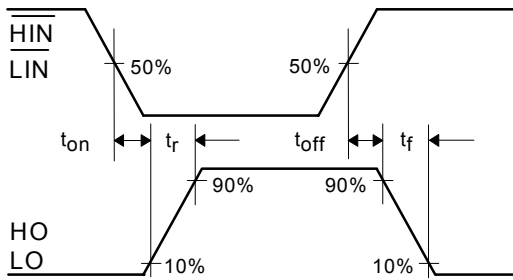


Figure 2. Switching Time Waveform Definitions

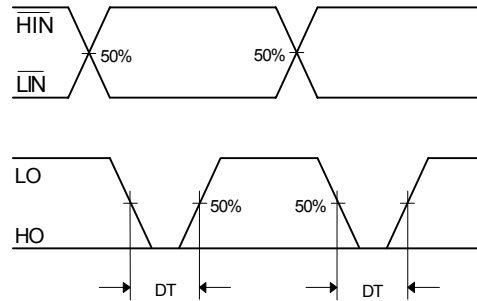


Figure 3. Deadtime Waveform Definitions

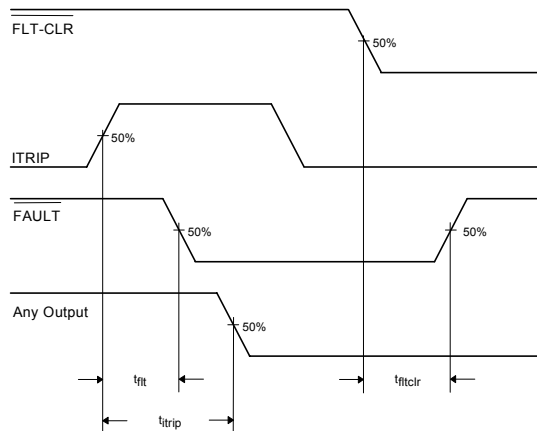


Figure 4. Overcurrent Shutdown Waveform

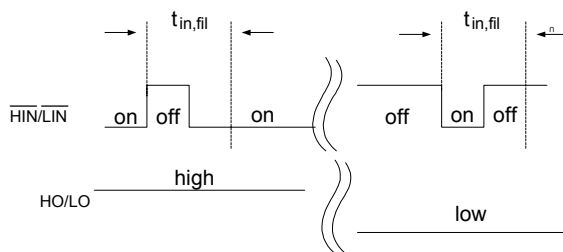


Figure 4.5. Input Filter Function

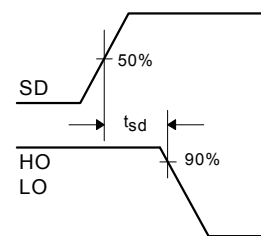


Figure 5. Shutdown Waveform Definitions

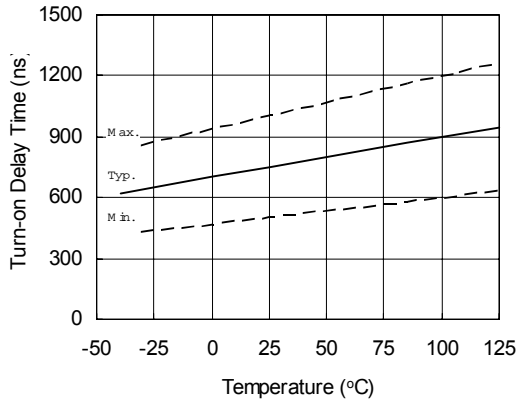


Figure 6A. Turn-On Time vs. Temperature

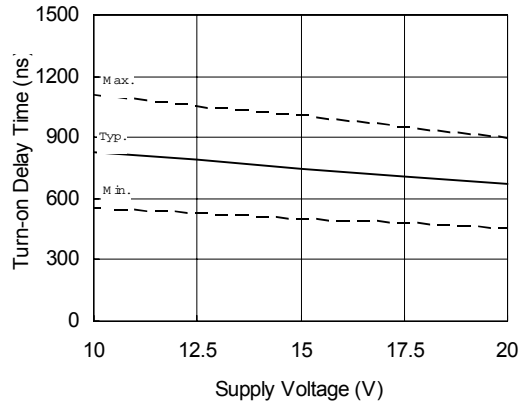


Figure 6B. Turn-On Time vs. Voltage



Figure 6C. Turn-On Time vs. Input Voltage

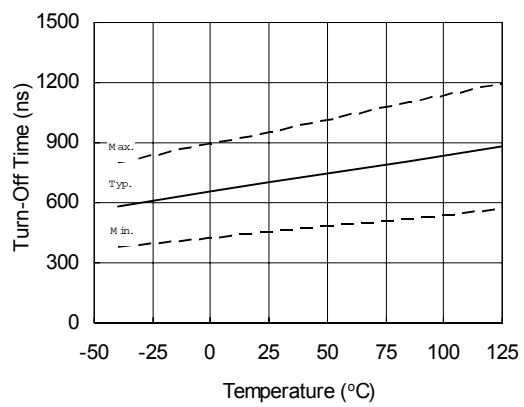


Figure 7A. Turn-Off Time vs. Temperature

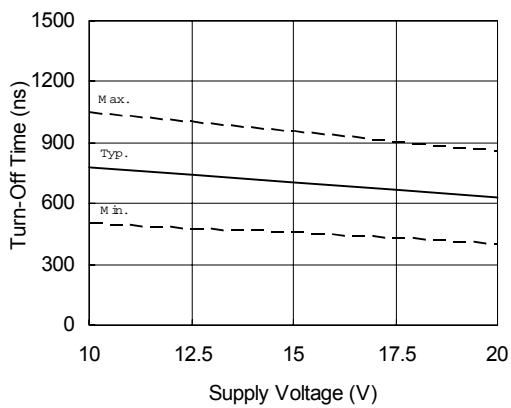


Figure 7B. Turn-Off Time vs. Voltage

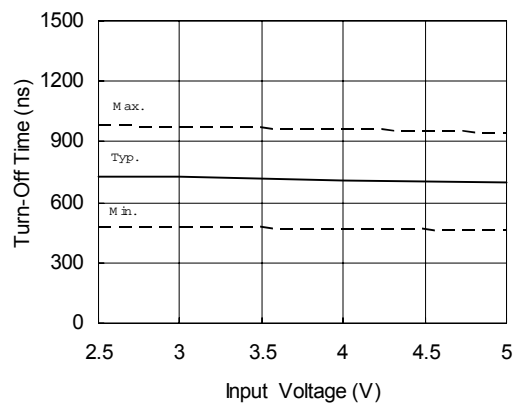


Figure 7C. Turn-Off Time vs. Input Voltage

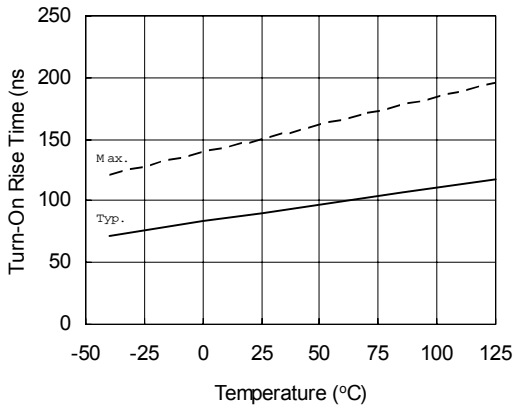


Figure 8A. Turn-On Rise Time vs. Temperature

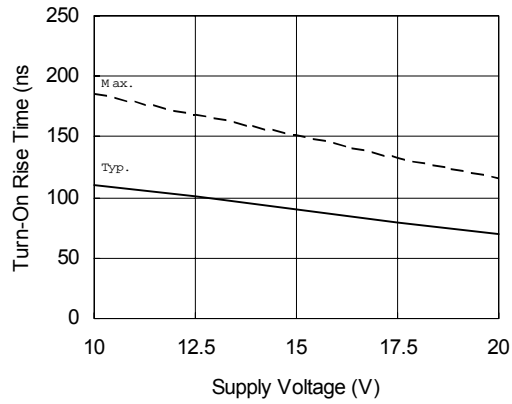


Figure 8B. Turn-On Rise Time vs. Voltage

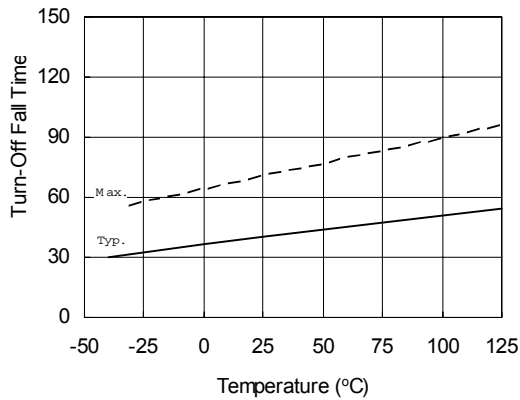


Figure 9A. Turn-Off Fall Time vs. Temperature

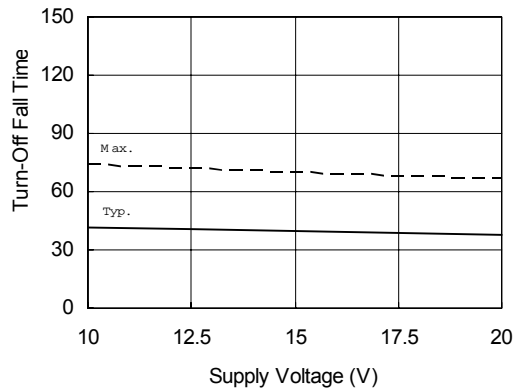


Figure 9B. Turn-Off Fall Time vs. Voltage



Figure 10A. SD to Output shutdown Time vs. Temperature

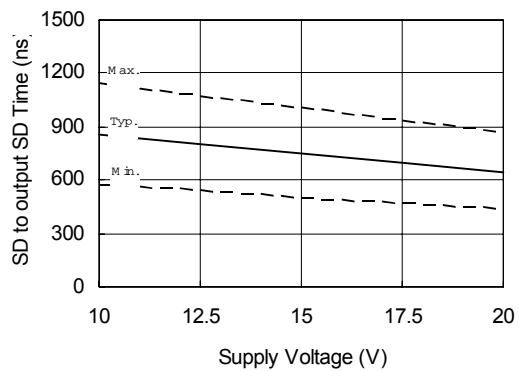


Figure 10B. SD to Output shutdown Time vs. Voltage

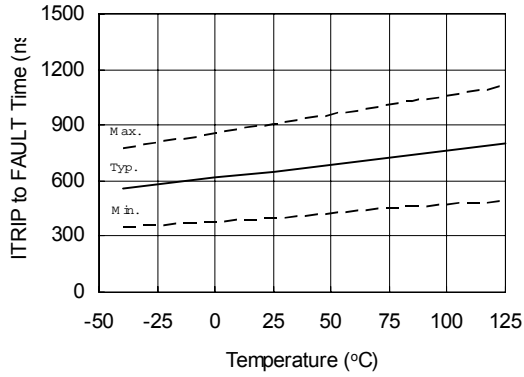


Figure 11A. ITRIP to FAULT Time vs. Temperature

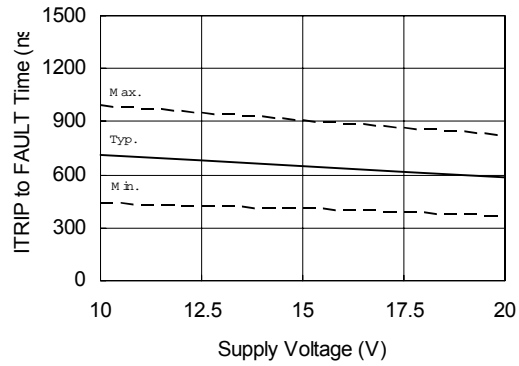


Figure 11B. ITRIP to FAULT Time vs. Voltage

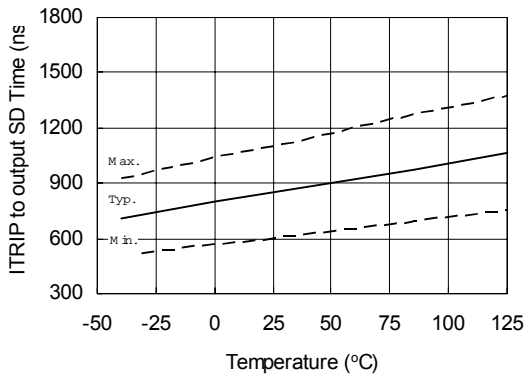


Figure 12A. ITRIP to output shutdown Time vs. Temperature

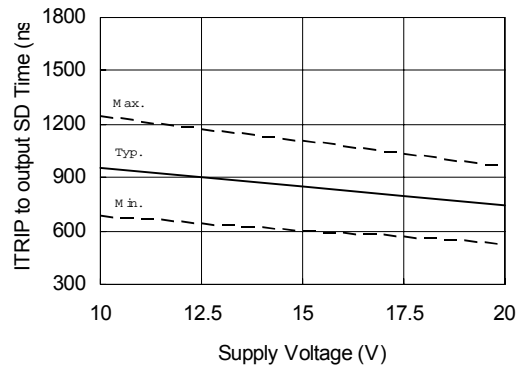


Figure 12B. ITRIP to output shutdown Time vs. Voltage

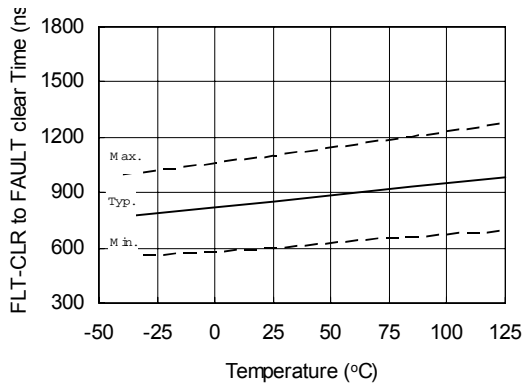


Figure 13A. FLT-CLR to FAULT clear Time vs. Temperature

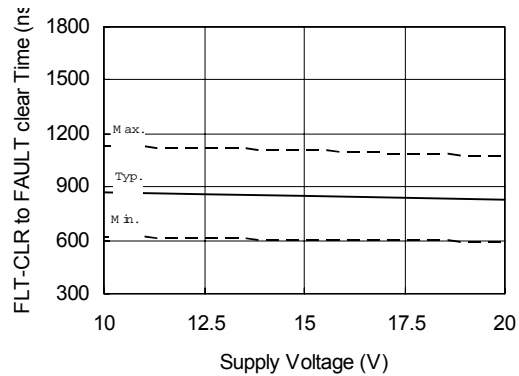


Figure 13B. FLT-CLR to FAULT clear Time vs. Voltage

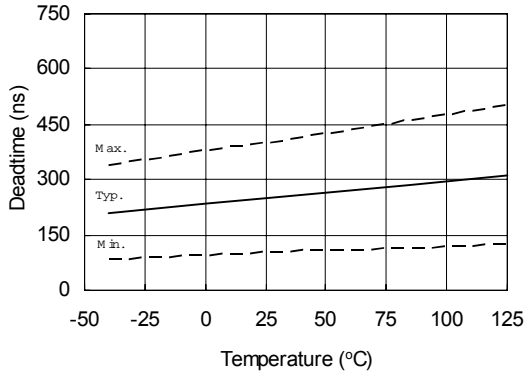


Figure 14A. Deadtime vs. Temperature

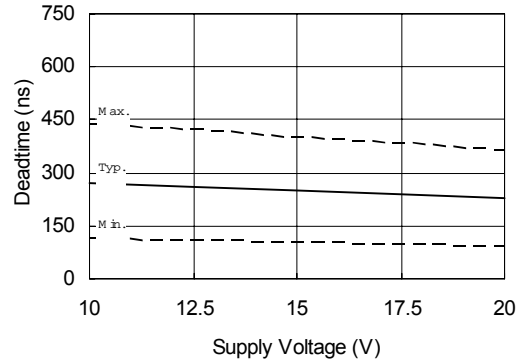


Figure 14B. Deadtime vs. Voltage

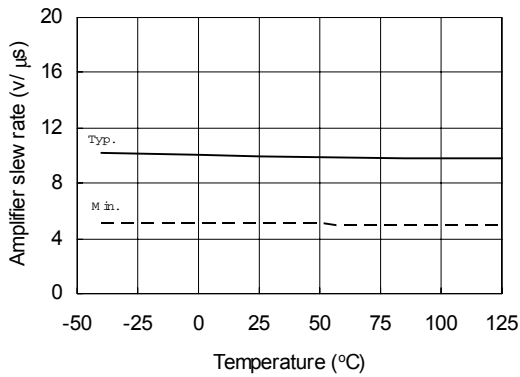


Figure 15A. Amplifier slew rate (+) vs. Temperature

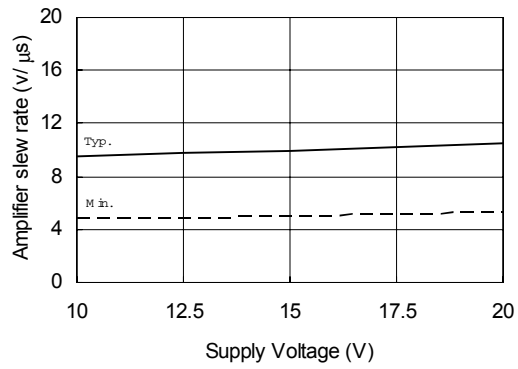


Figure 15B. Amplifier slew rate (+) vs. Voltage

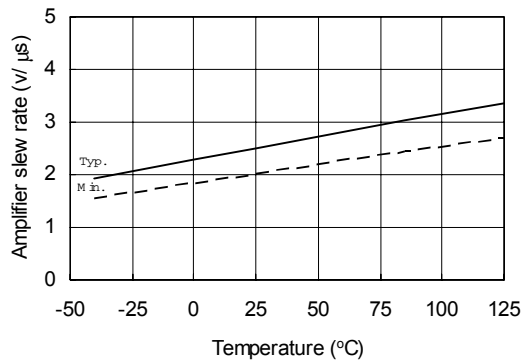


Figure 16A. Amplifier slew rate (-) vs. Temperature

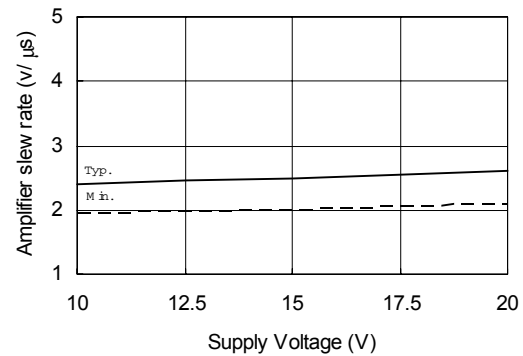


Figure 16B. Amplifier slew rate (-) vs. Voltage



Figure 17A. Logic "0" Input Voltage (OUT=LO), Fault Clear Voltage vs. Temperature

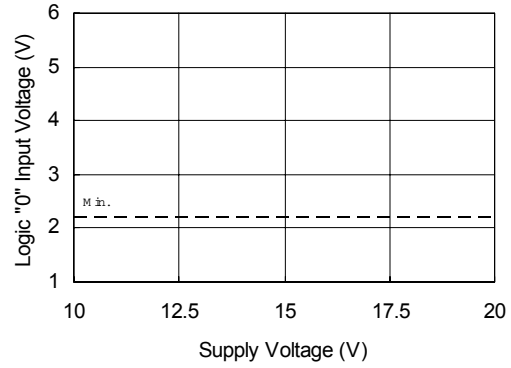


Figure 17B. Logic "0" Input Voltage (OUT=LO), Fault Clear Voltage vs. Voltage

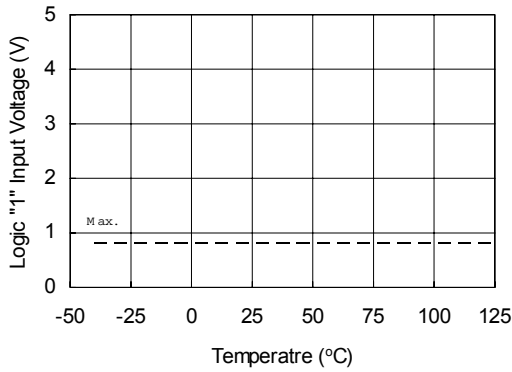


Figure 18A. Logic "1" Input (OUT=HI), Fault Clear Input Voltage vs. Temperature

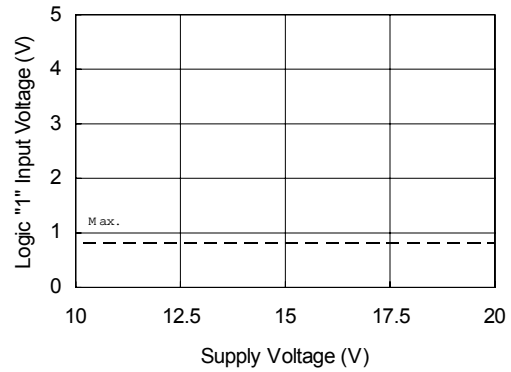


Figure 18B. Logic "1" Input (OUT=HI), Fault Clear Input Voltage vs. Voltage

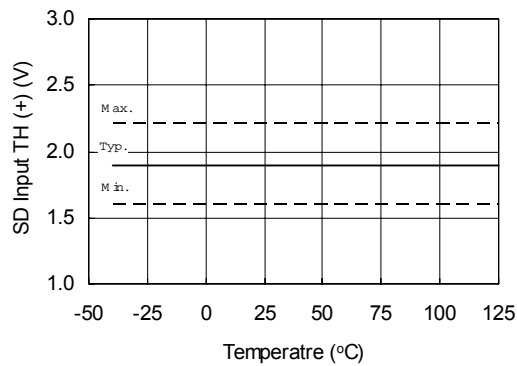


Figure 21A. SD Input TH(+) vs. Temperature

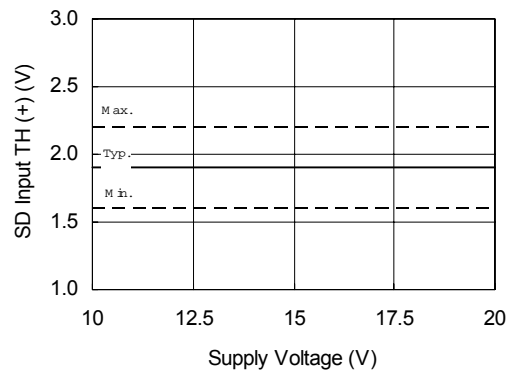


Figure 21B. SD Input TH(+) vs. Voltage

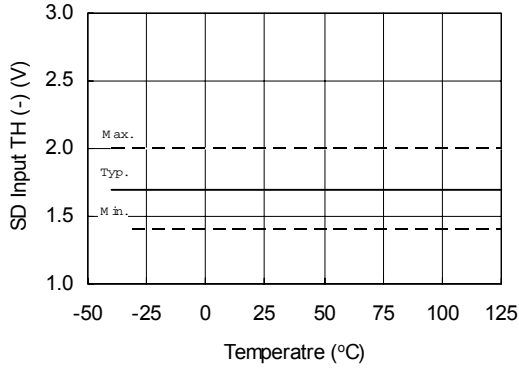


Figure 22A. SD Input TH(-) vs. Temperature

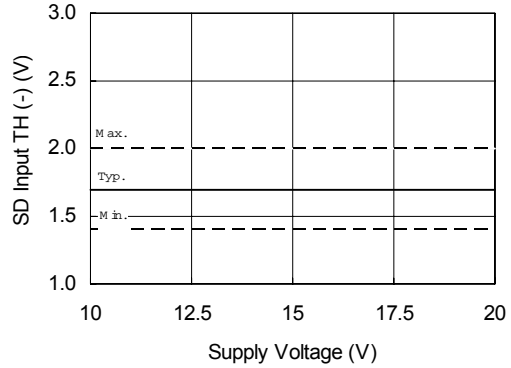


Figure 22B. SD Input TH(-) vs. Voltage

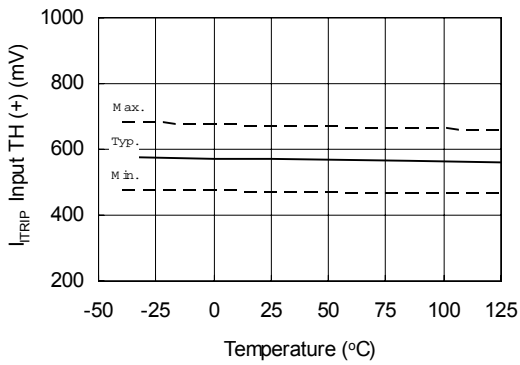


Figure 23A. I_{TRIP} Input TH(+) vs. Temperature

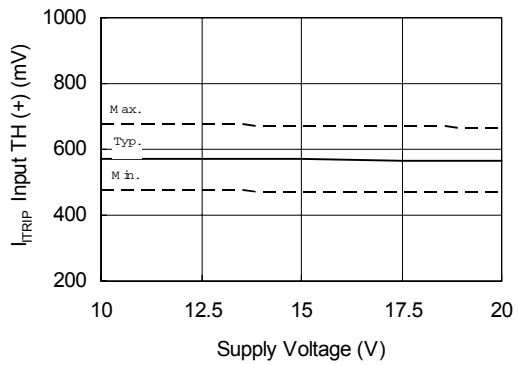


Figure 23B. I_{TRIP} Input TH(+) vs. Voltage

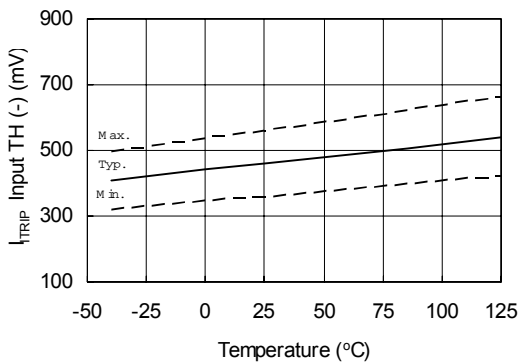


Figure 24A. I_{TRIP} Input TH(-) vs. Temperature

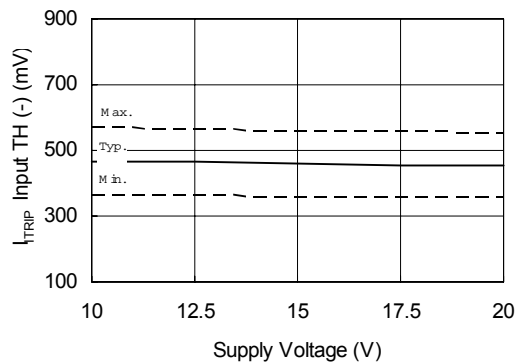


Figure 24B. I_{TRIP} Input TH(-) vs. Voltage

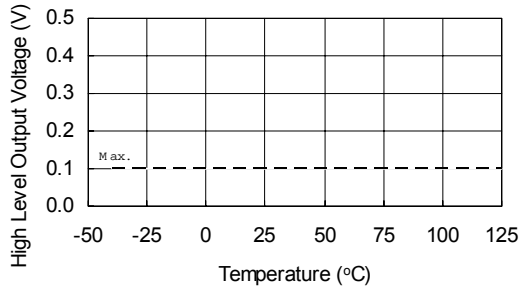


Figure 25A. High Level Output vs. Temperature

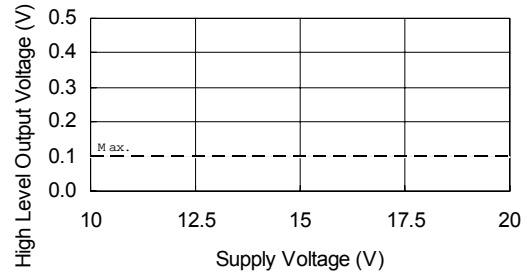


Figure 25B. High Level Output vs. Voltage

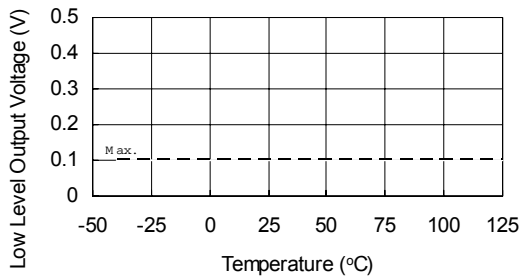


Figure 26A. Low Level Output vs. Temperature

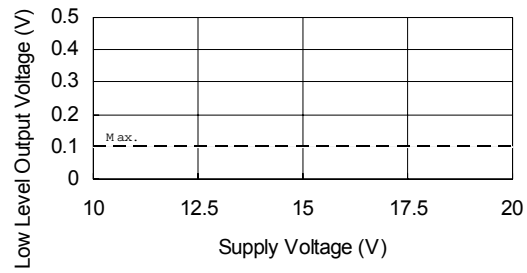


Figure 26B. Low Level Output vs. Voltage

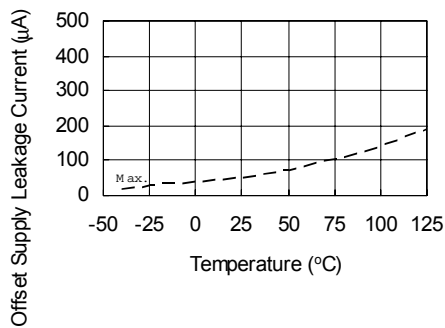


Figure 27A. Offset Supply Leakage Current vs. Temperature

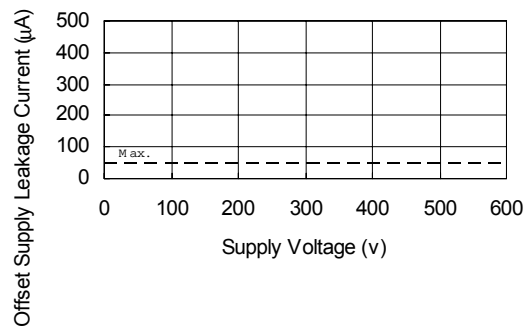


Figure 27B. Offset Supply Leakage Current vs. Voltage

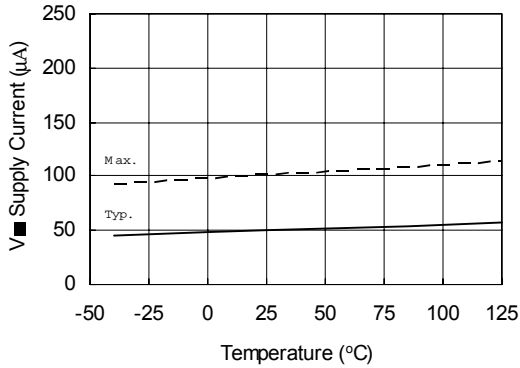


Figure 28A. V_{BS} Supply Current vs. Temperature

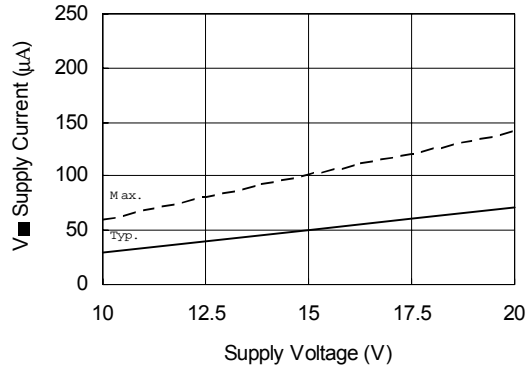


Figure 28B. V_{BS} Supply Current vs. Voltage

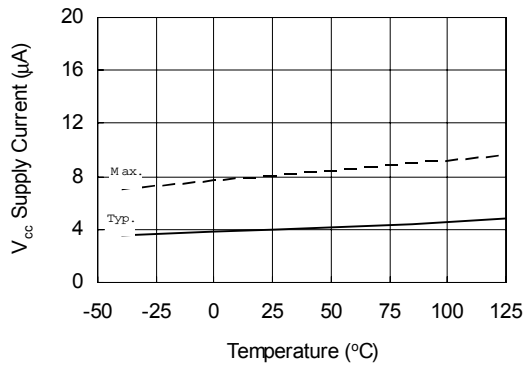


Figure 29A. V_{CC} Supply Current vs. Temperature

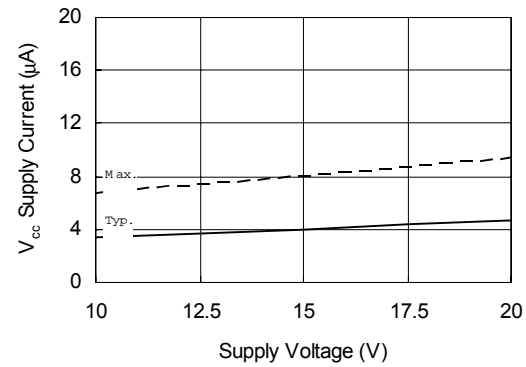


Figure 29B. V_{CC} Supply Current vs. Voltage

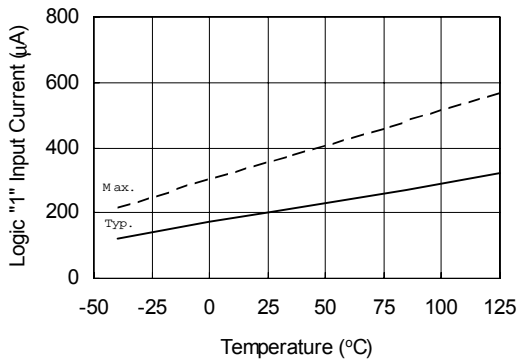


Figure 30A. Logic "1" Input Bias Current vs. Temperature

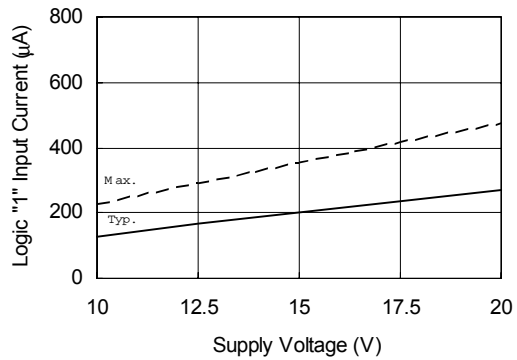


Figure 30B. Logic "1" Input Bias Current vs. Voltage

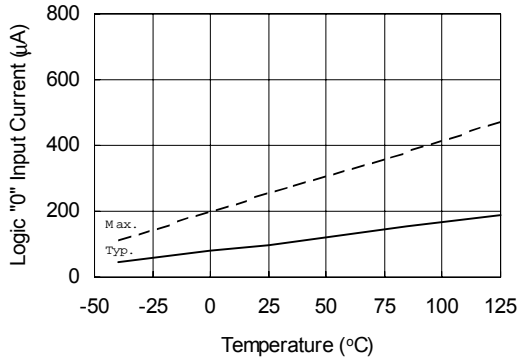


Figure 31A. Logic "0" Input Bais Current vs. Temperature

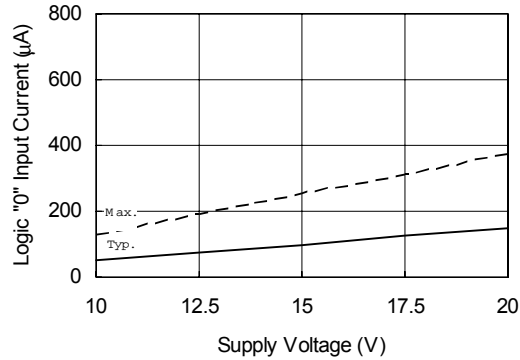


Figure 31B. Logic "0" Input Bais Current vs. Supply Voltage

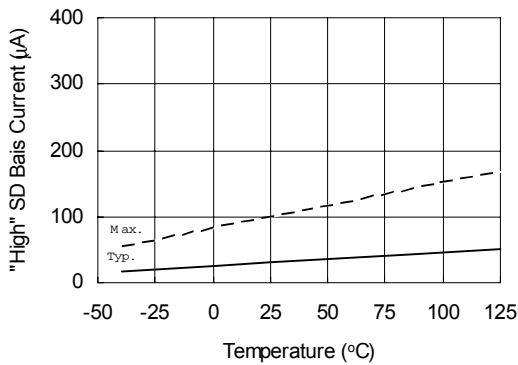


Figure 32A. "High" Shutdown Bais Current vs. Temperature

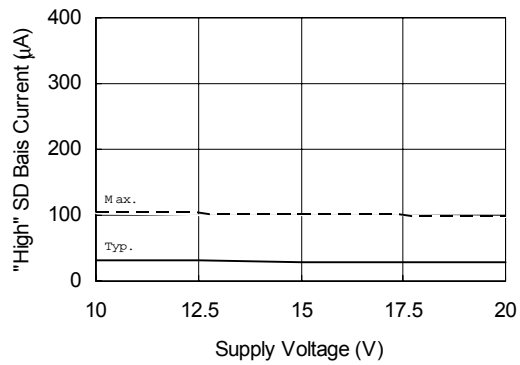


Figure 32B. "High" Shutdown Bais Current vs. Supply Voltage

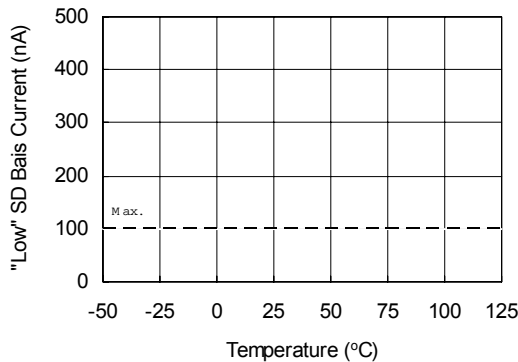


Figure 33A. "Low" Shutdown Bais Current vs. Temperature

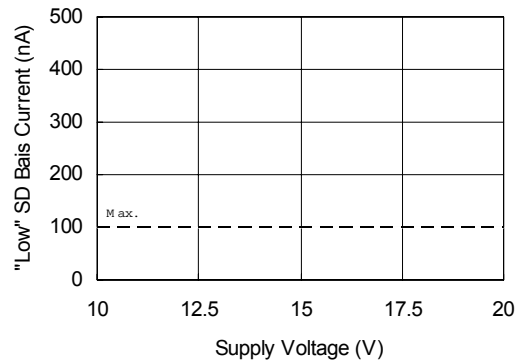


Figure 33B. "Low" Shutdown Bais Current vs. Supply Voltage

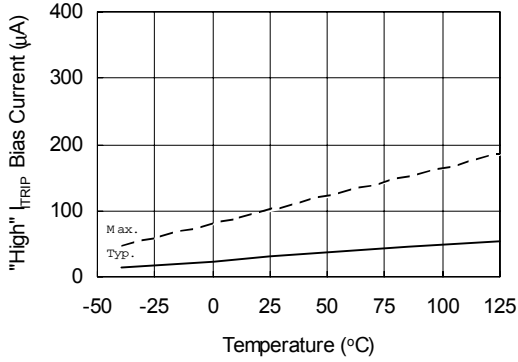


Figure 34A. "High" I_{TRIP} Bias Current vs. Temperature

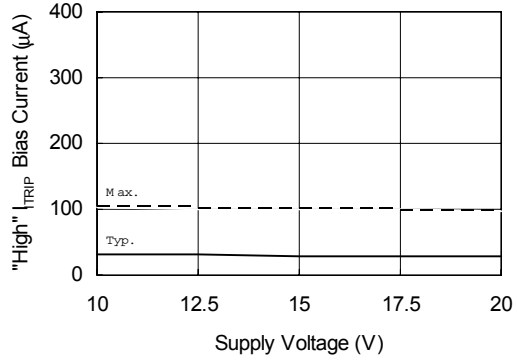


Figure 34B. "High" I_{TRIP} Bias Current vs. Supply Voltage

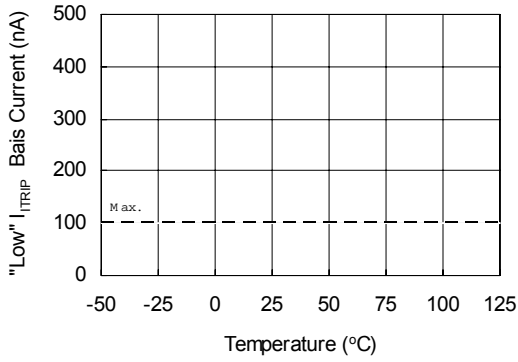


Figure 35A. "Low" I_{TRIP} Bias Current vs. Temperature

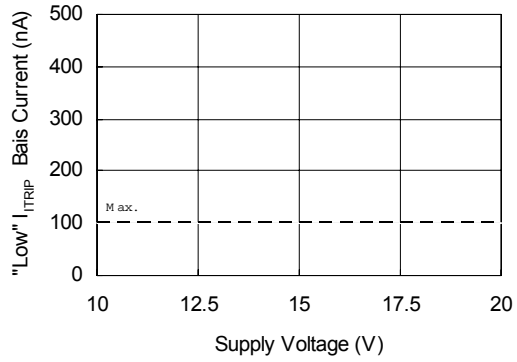


Figure 35B. "Low" I_{TRIP} Bias Current vs. Supply Voltage

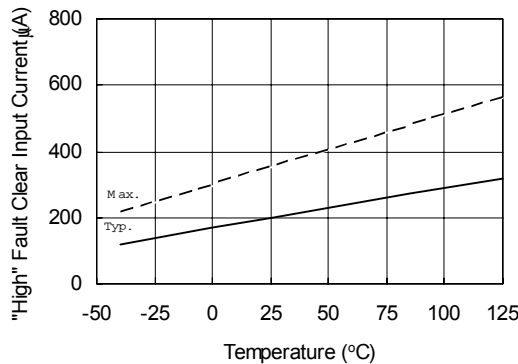


Figure 36A. "High" Fault Clear Input Bias Current vs. Temperature

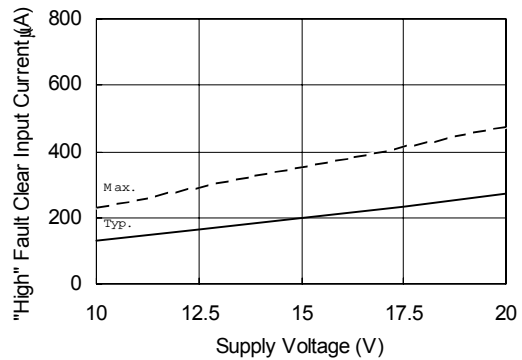


Figure 36B. "High" Fault Clear Input Bias Current vs. Supply voltage

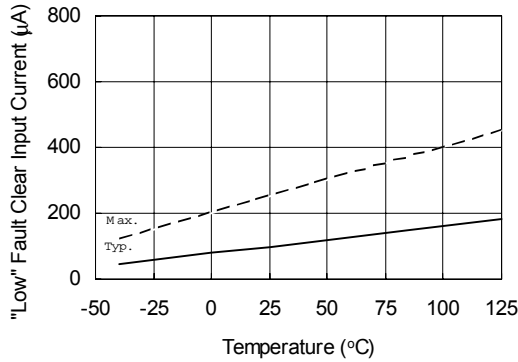


Figure 37A. "Low" Fault Clear Input Bias Current vs. Temperature

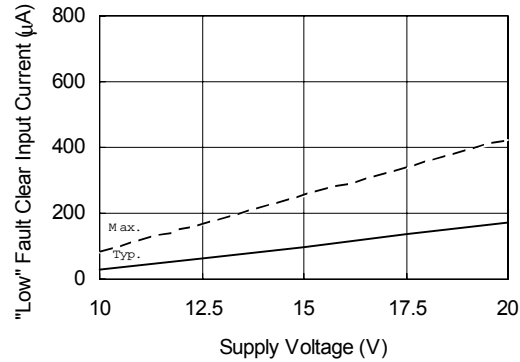


Figure 37B. "Low" Fault Clear Input Bias Current vs. Supply Voltage

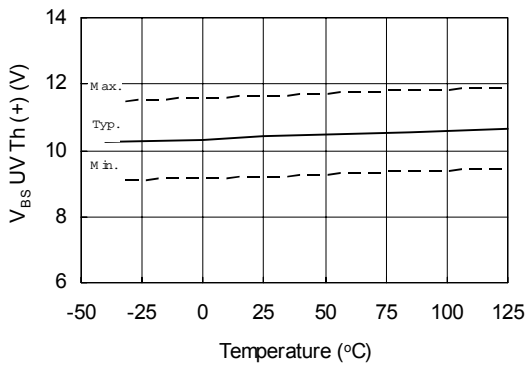


Figure 38A. IR2135/IR2235 V_{BS} Undervoltage Threshold (+) vs. Temperature

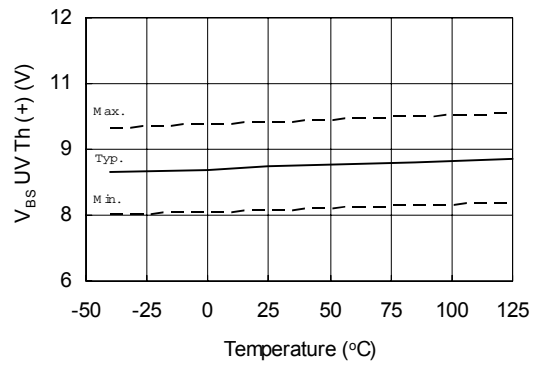


Figure 38B. IR2133/IR2233 V_{BS} Undervoltage Threshold (+) vs. Temperature

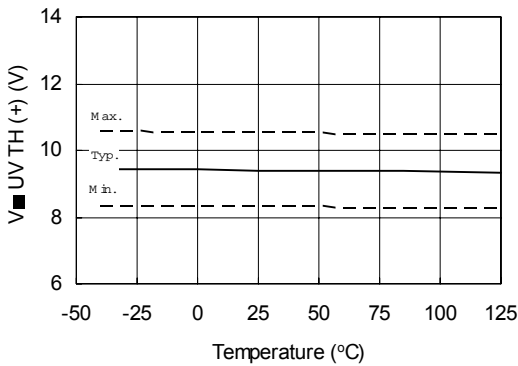


Figure 39A. IR2135/IR2235 V_{BS} Undervoltage Threshold (-) vs. Temperature

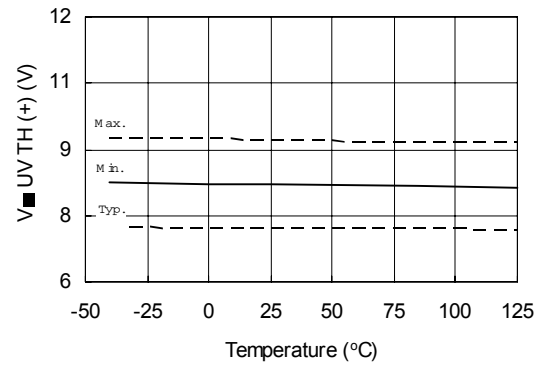


Figure 39B. IR2133/IR2233 V_{BS} Undervoltage Threshold (-) vs. Temperature

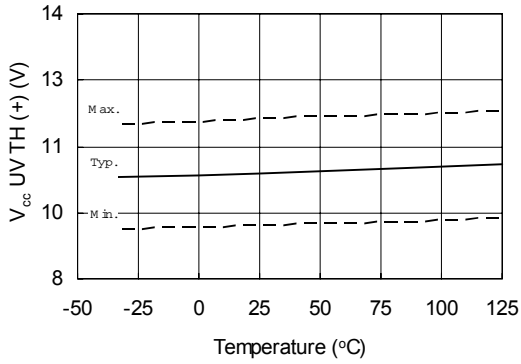


Figure 40A. IR2135/IR2235 V_{cc} Undervoltage Threshold (+) vs. Temperature

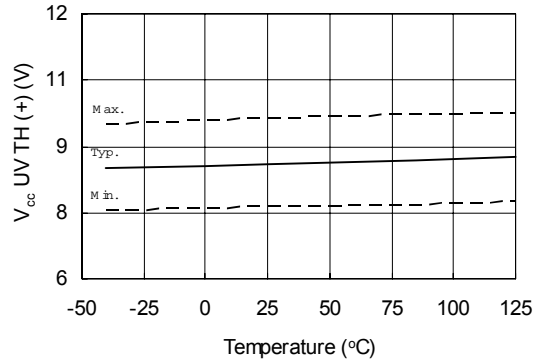


Figure 40B. IR2133/IR2233 V_{cc} Undervoltage Threshold (+) vs. Temperature

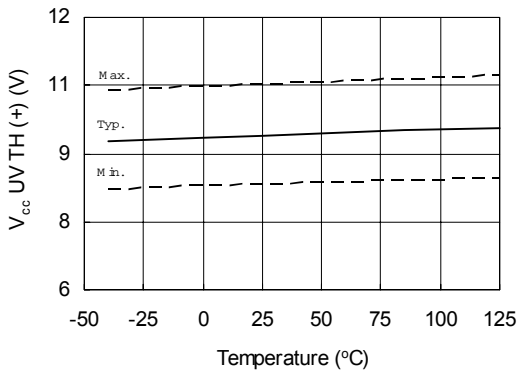


Figure 41A. IR2135/IR2235 V_{cc} Undervoltage Threshold (-) vs. Temperature

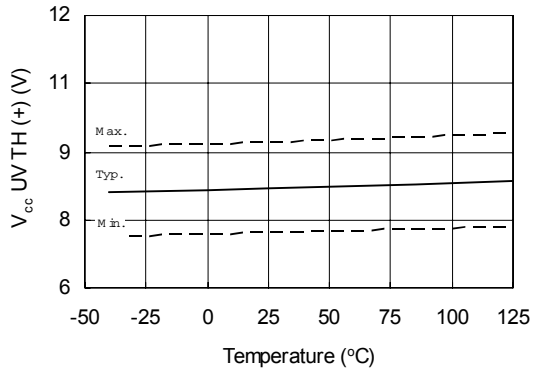


Figure 41B. IR2133/IR2233 V_{cc} Undervoltage Threshold (-) vs. Temperature

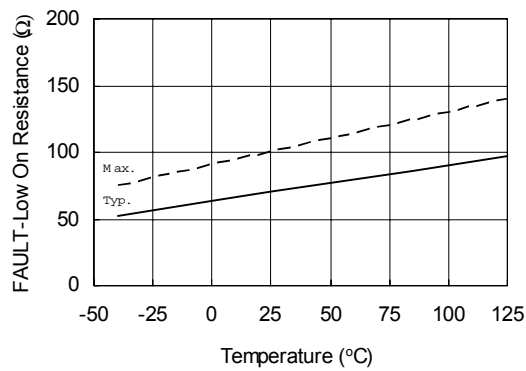


Figure 42A. FAULT- Low On Resistance vs. Temperature

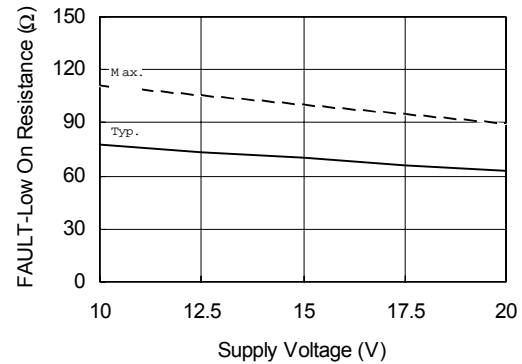


Figure 42B. FAULT- Low On Resistance vs. Supply Voltage

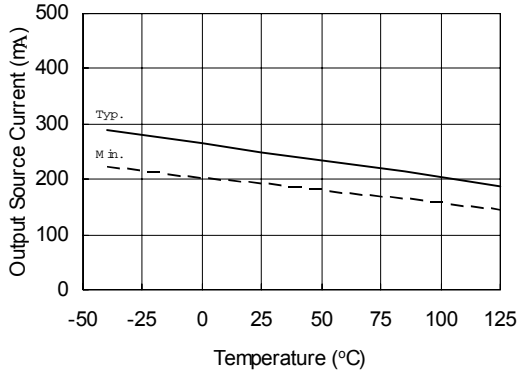


Figure 43A. Output Source Current vs. Temperature

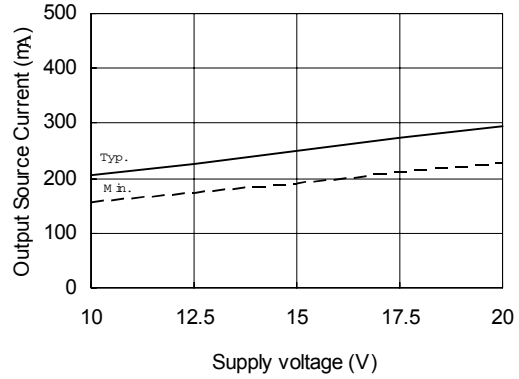


Figure 43B. Output Source Current vs. Supply Voltage

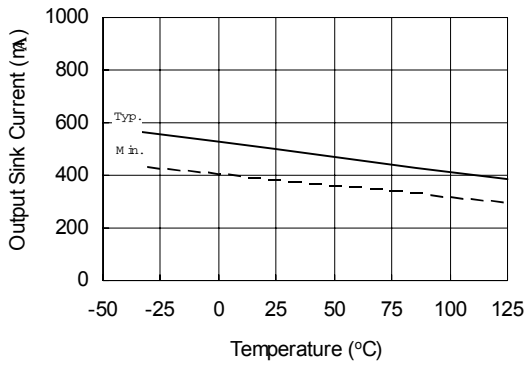


Figure 44A. Output Sink Current vs. Temperature



Figure 44B. Output Sink Current vs. Supply Voltage

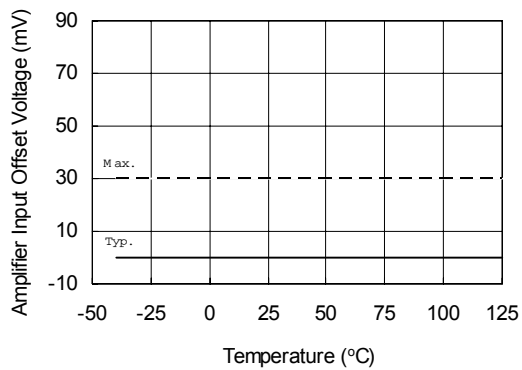


Figure 45A. Amplifier Input Offset Voltage vs. Temperature

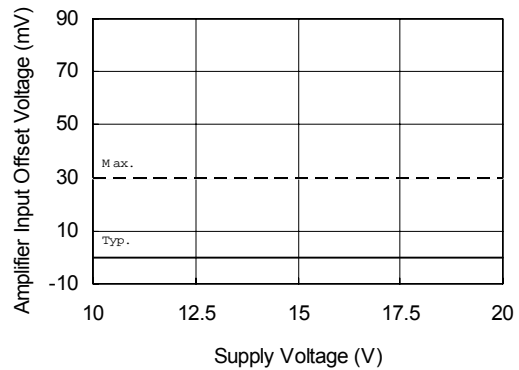


Figure 45B. Amplifier Input Offset Voltage vs. Supply Voltage

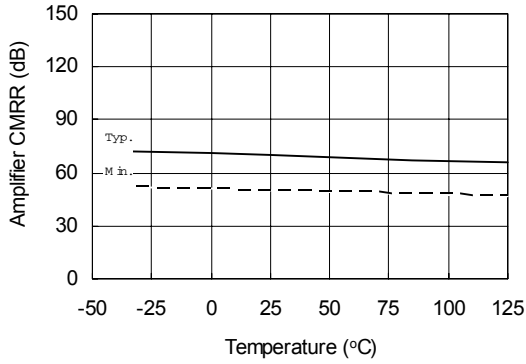


Figure 46A. Amplifier Common Mode Rejection Ratio vs. Temperature

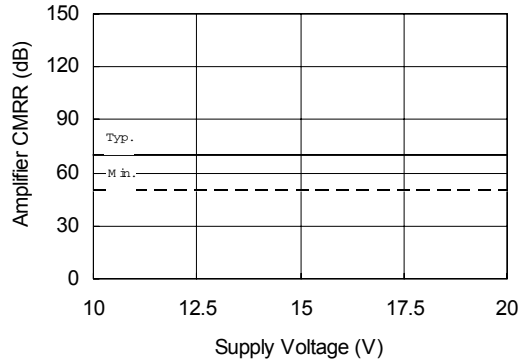


Figure 46B. Amplifier Common Mode Rejection Ratio vs. Supply Voltage

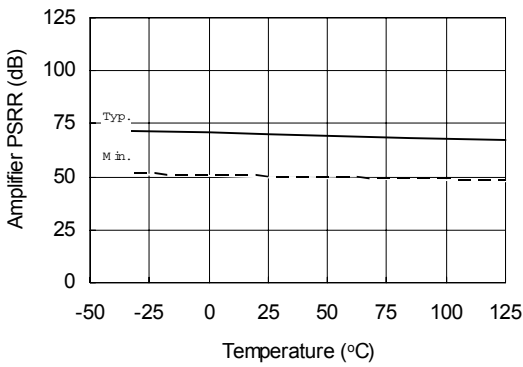


Figure 47A. Amplifier Power Supply Rejection Ratio vs. Temperature

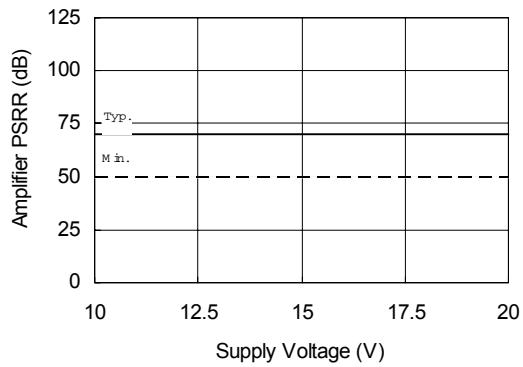


Figure 47B. Amplifier Power Supply Rejection Ratio vs. Supply Voltage

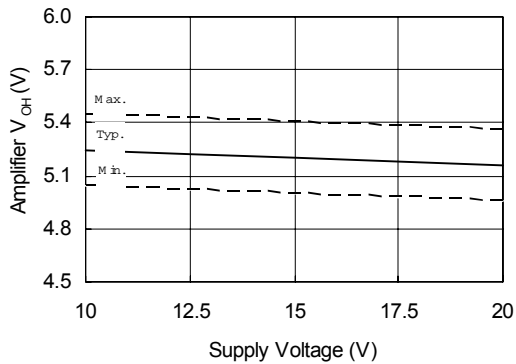


Figure 48. Amplifier High Level Output Voltage vs. Supply Voltage

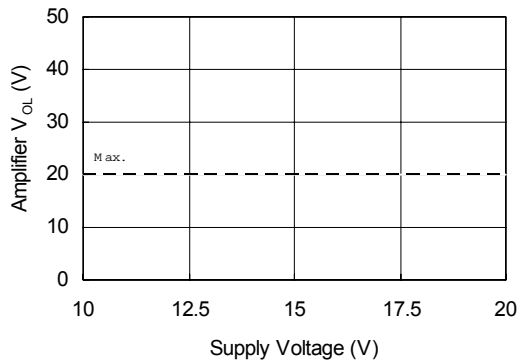


Figure 49. Amplifier Low Level Output Voltage vs. Supply Voltage

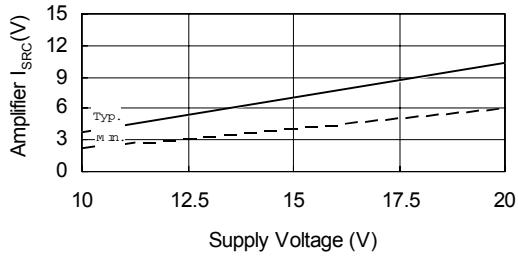


Figure 50. Amplifier Output Source Current vs. Supply Voltage

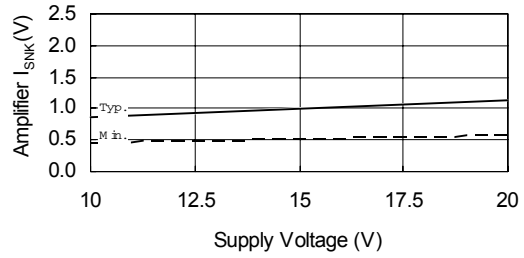


Figure 51. Amplifier Output Sink Current vs. Supply Voltage

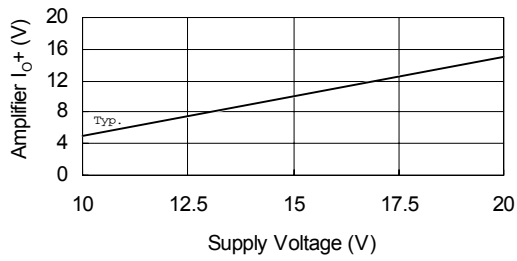


Figure 52. Amplifier Output High Short Circuit Current vs. Supply Voltage

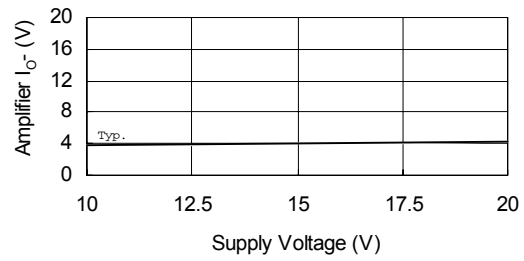


Figure 53. Amplifier Output Low Short Circuit Current vs. Supply Voltage

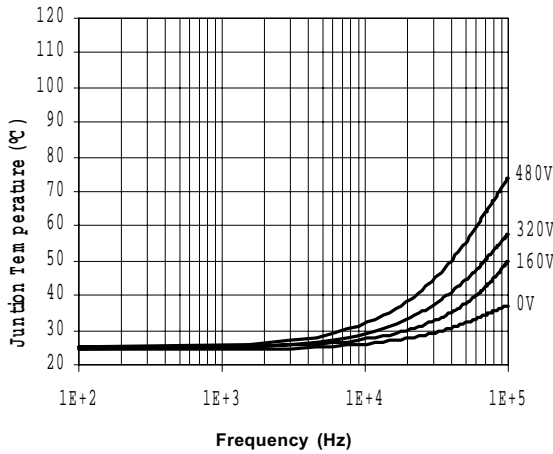


Figure 7. IR2133J Junction Temperature vs Frequency Driving (IRGPC20KD2) Rgate = 5.1Ω @ Vcc = 15V

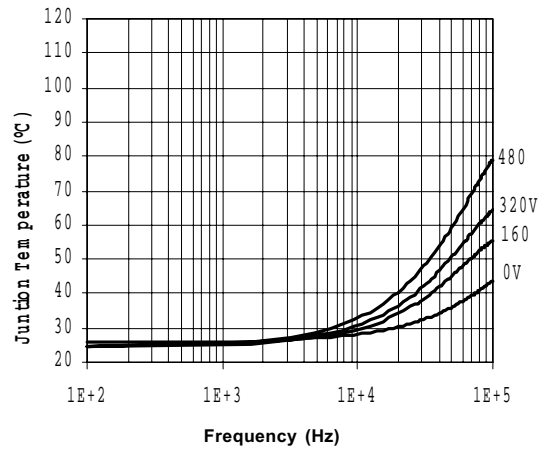


Figure 8. IR2133J Junction Temperature vs Frequency Driving (IRGPC30KD2) Rgate = 5.1Ω @ Vcc = 15V

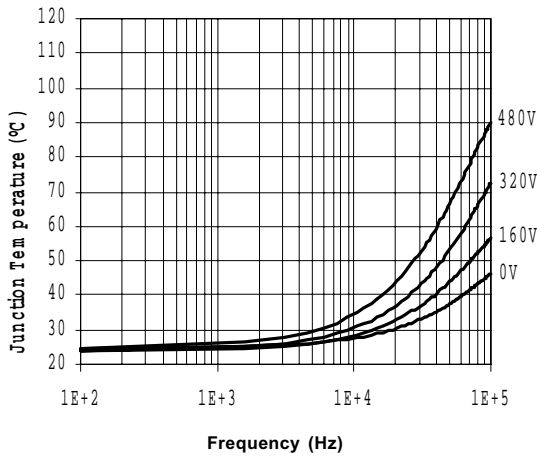


Figure 9. IR2133J Junction Temperature vs Frequency Driving (IRGPC40KD2) Rgate = 5.1Ω @ Vcc = 15V

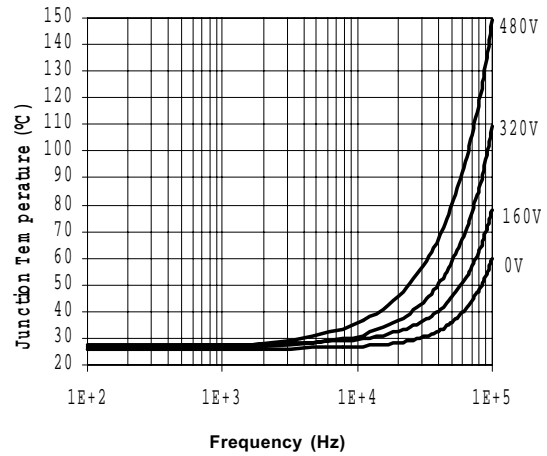


Figure 10. IR2133J Junction Temperature vs Frequency Driving (IRGPC50KD2) Rgate = 5.1Ω @ Vcc = 15V

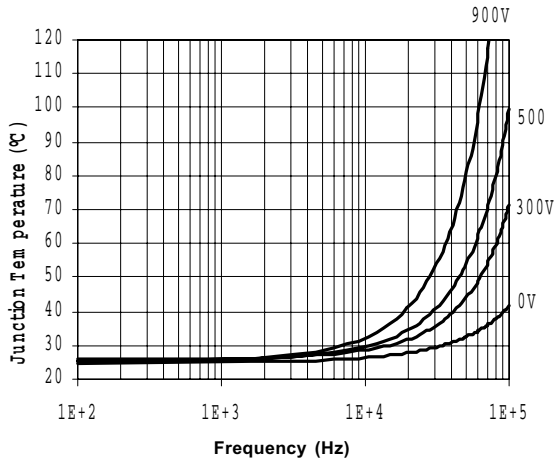


Figure 11. IR2233J Junction Temperature vs Frequency Driving (IRG4PH30KD) Rgate = 20Ω @ Vcc = 15V

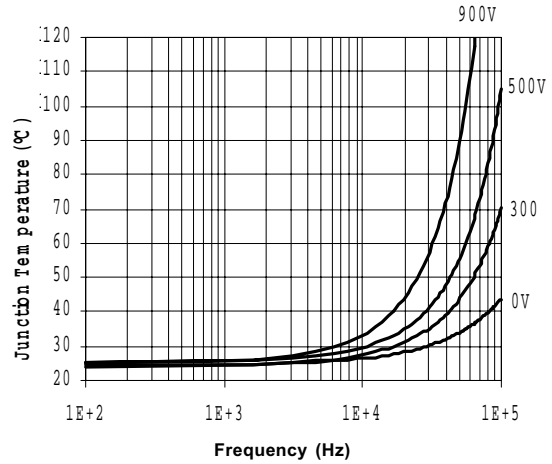


Figure 12. IR2233J Junction Temperature vs Frequency Driving (IRG4PH40KD) Rgate = 15Ω @ Vcc = 15V

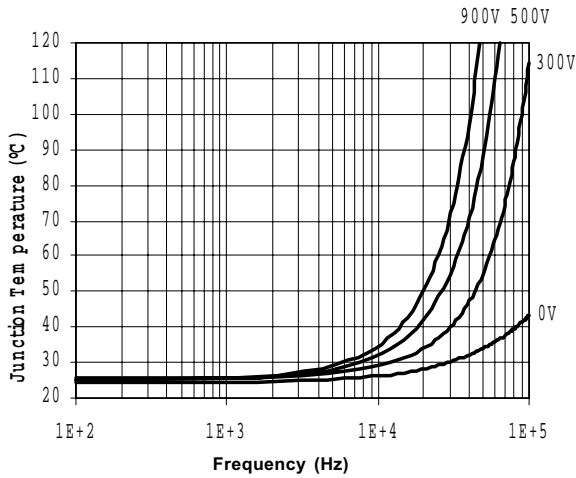


Figure 13. IR2233J Junction Temperature vs Frequency Driving (IRG4PH50KD) Rgate = 10Ω @ Vcc = 15V

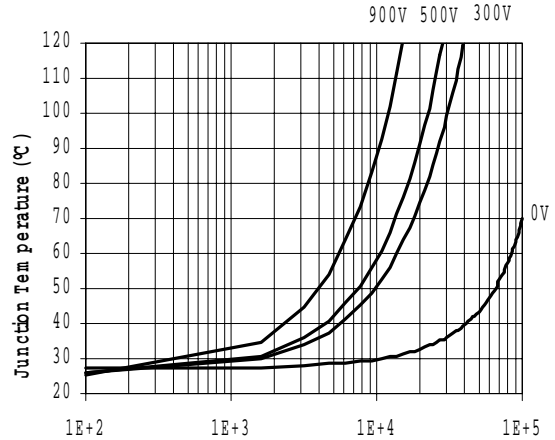
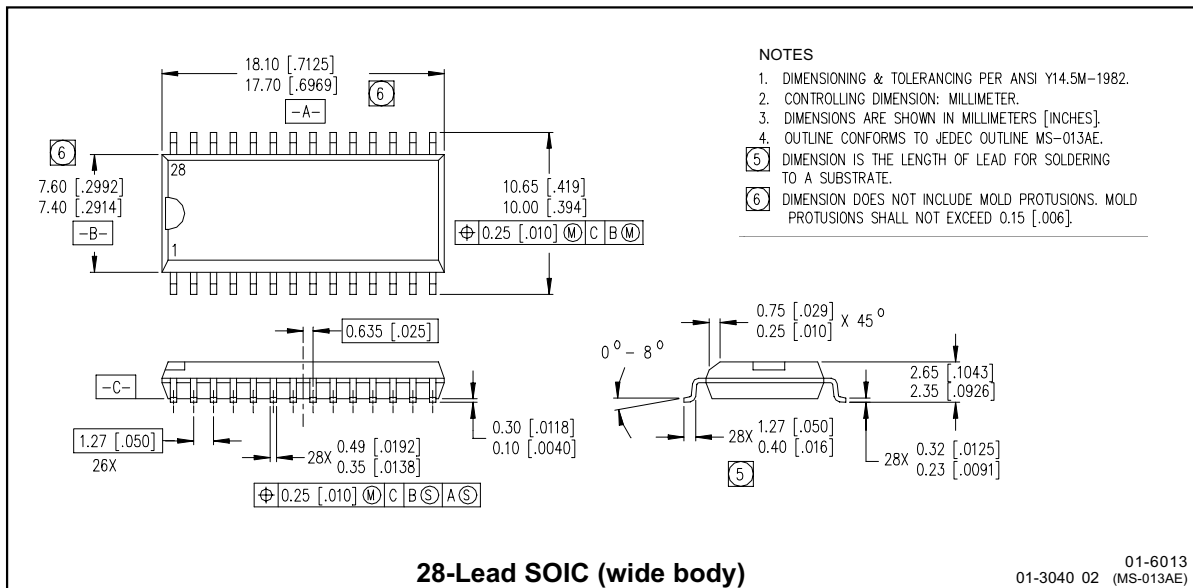
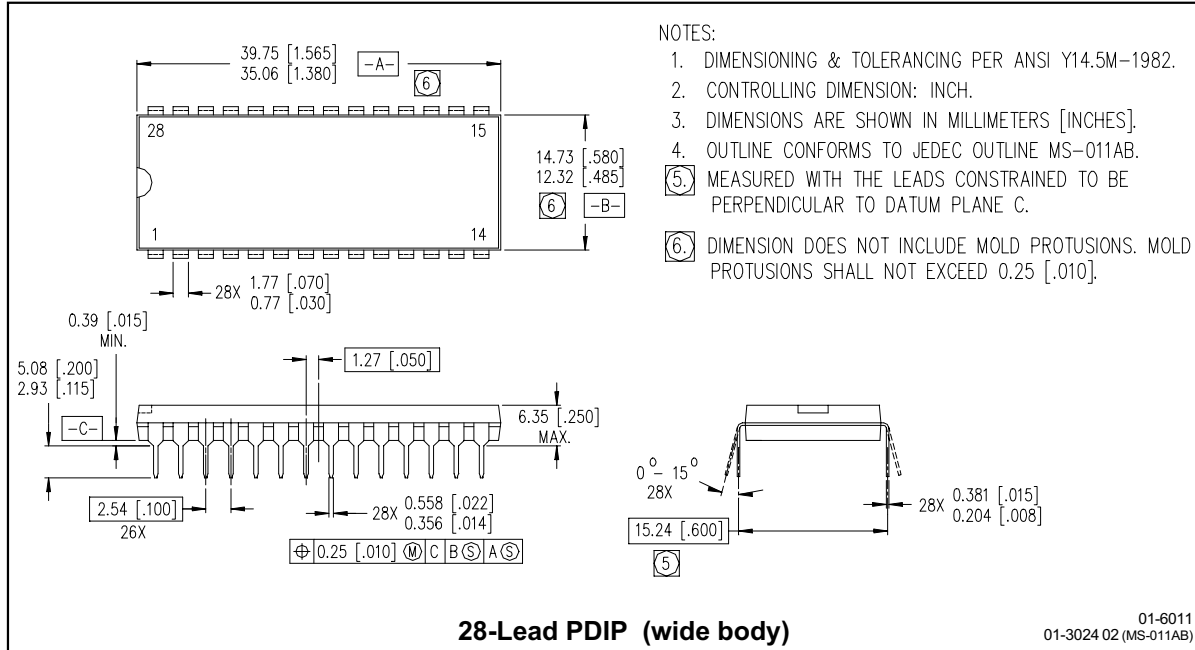


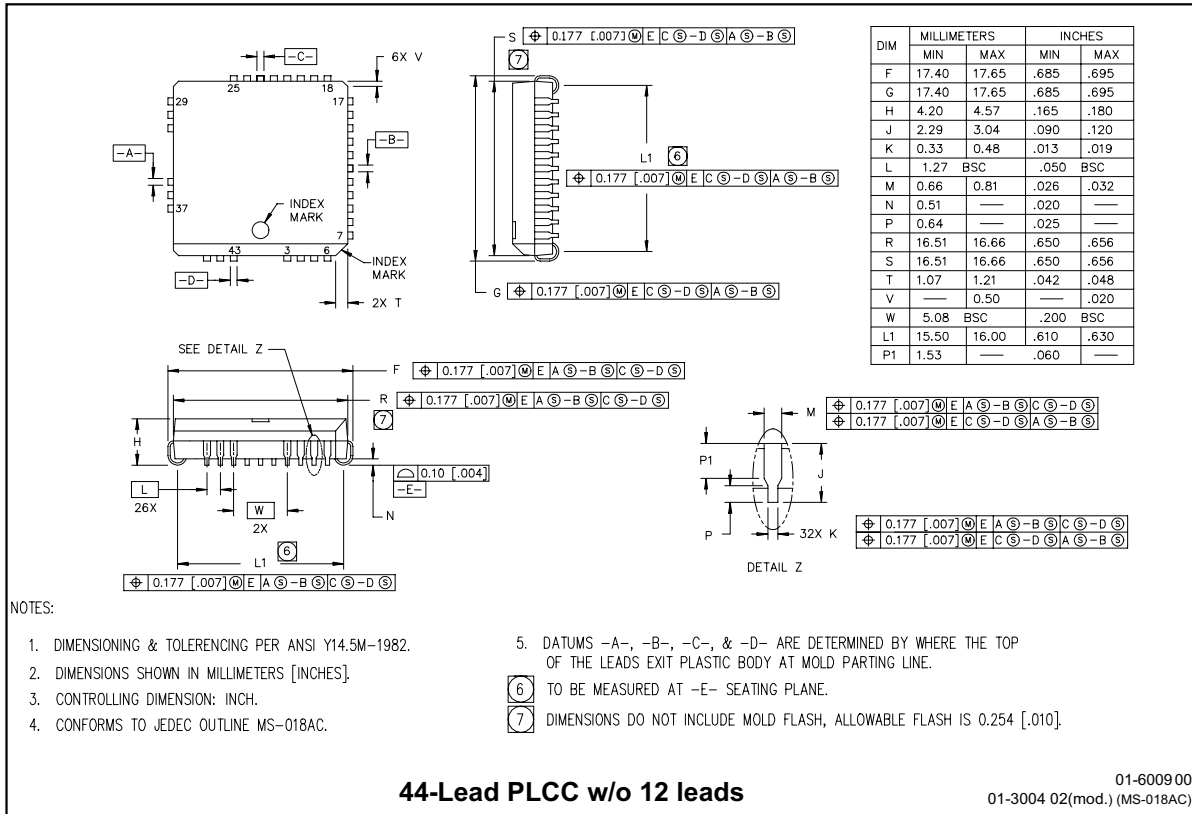
Figure 14. IR2233J Junction Temperature vs Frequency Driving (IRG4ZH71KD) Rgate = 5Ω @ Vcc = 15V

Package Dimensions



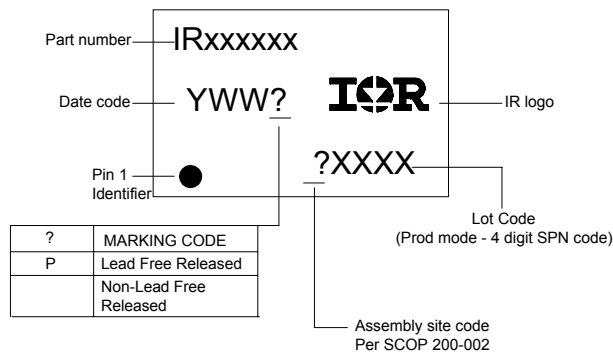
IR2133/IR2135/IR2233/IR2235(J&S)&(PbF)

International
IR Rectifier



IR2133/IR2135/IR2233/IR2235(J&S)&(PbF)

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

28-Lead PDIP IR2133 order IR2133 2
 8-Lead SOIC IR2133S order IR2133S
 28-Lead PDIP IR2135 order IR2135
 28-Lead SOIC IR2135S order IR2135S
 28-Lead PDIP IR2233 not available
 28-Lead SOIC IR2233S order IR2233S
 28-Lead PDIP IR2235 not available
 28-Lead SOIC IR2235S order IR2235S
 44-Lead PLCC IR2133J order IR2133J
 44-Lead PLCC IR2135J order IR2135J
 44-Lead PLCC IR2233J order IR2233J
 44-Lead PLCC IR2235J order IR2235J

Leadfree Part

28-Lead PDIP IR2133 order IR2133PbF
 28-Lead SOIC IR2133S order IR2133SPbF
 28-Lead PDIP IR2135 order IR2135PbF
 28-Lead SOIC IR2135S order IR2135SPbF
 28-Lead PDIP IR2233 order IR2233PbF
 28-Lead SOIC IR2233S order IR2233SPbF
 28-Lead PDIP IR2235 order IR2235PbF
 28-Lead SOIC IR2235S order IR2235SPbF
 44-Lead PLCC IR2133J order IR2133JPbF
 44-Lead PLCC IR2135J order IR2135JPbF
 44-Lead PLCC IR2233J order IR2233JPbF
 44-Lead PLCC IR2235J order IR2235JPbF