

IRS2304(S)PbF HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic input compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Internal 100 ns deadtime
- Output in phase with input
- RoHS compliant

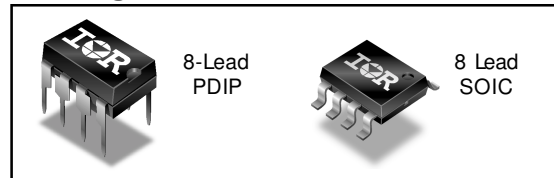
Description

The IRS2304 is a high voltage, high speed power MOSFET and IGBT driver with independent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Product Summary

V _{OFFSET}	600 V max.
I _{O+/-} (min)	60 mA/130 mA
V _{OUT}	10 V - 20 V
Delay Matching	50 ns
Internal deadtime	100 ns
ton/off (typ.)	150 ns/150 ns

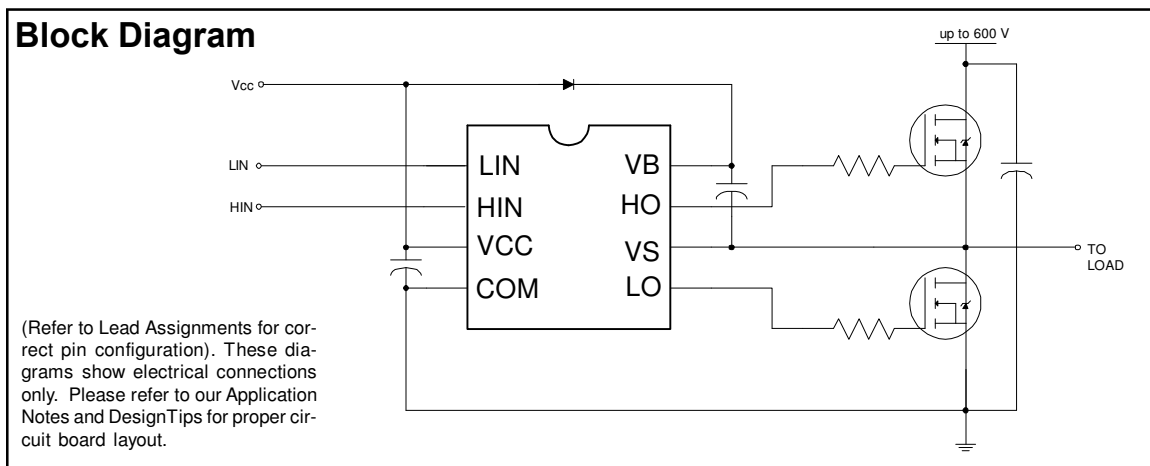
Package



Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Deadtime (ns)	Ground Pins	ton/toff (ns)
2106/2301	HIN/LIN	no	none	COM	220/200
21064				V _{SS} /COM	
2108	HIN/LIN	yes	Internal 540	COM	220/200
21084				V _{SS} /COM	
2109/2302	IN/SD	yes	Internal 540	COM	750/200
21094				V _{SS} /COM	
2304	HIN/LIN	yes	Internal 100	COM	160/140

Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _S	High-side offset voltage	V _B - 25	V _B + 0.3	V	
V _B	High-side floating supply voltage	-0.3	625		
V _{HO}	High-side floating output voltage HO	V _S - 0.3	V _B + 0.3		
V _{CC}	Low-side and logic fixed supply voltage	-0.3	25		
V _{LO}	Low-side output voltage LO	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (HIN, LIN)	-0.3	V _{CC} + 0.3		
Com	Logic ground	V _{CC} -25	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns	
P _D	Package power dissipation @ TA ≤ +25 °C	8-Lead SOIC	—	0.625	W
		8-Lead PDIP	—	1.0	
R _{thJA}	Thermal resistance, junction to ambient	8-Lead SOIC	—	200	°C/W
		8-Lead PDIP	—	125	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-50	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High-side floating supply voltage	V _S + 10	V _S + 20	V
V _S	High-side floating supply offset voltage	Note 1	600	
V _{HO}	High-side (HO) output voltage	V _S	V _B	
V _{LO}	Low-side (LO) output voltage	COM	V _{CC}	
V _{IN}	Logic input voltage (HIN, LIN)	COM	V _{CC}	
V _{CC}	Low-side supply voltage	10	20	
T _A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5 V to COM +600 V. Logic state held for V_S of COM -5 V to COM -V_{BS}.

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15 V and T_A = 25 °C unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and V_S is applicable to HO and LO.

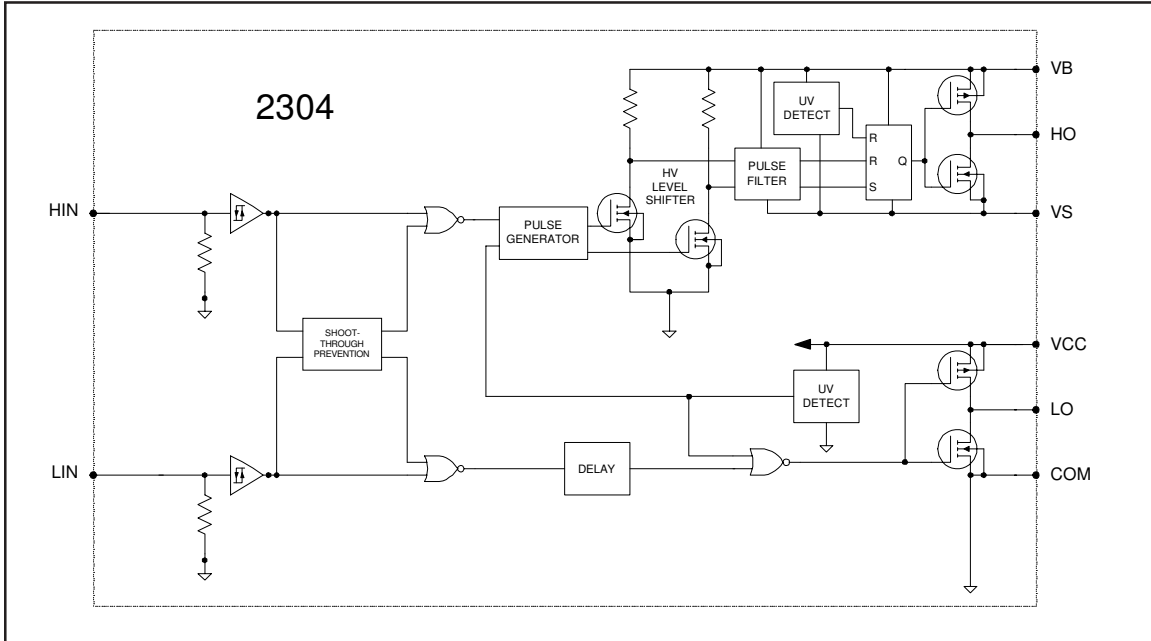
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9		
V_{CCUVH} V_{BSUVH}	V_{CC} supply undervoltage lockout hysteresis	0.3	0.7	—		
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600 V$
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		$V_{IN} = 0 V$ or 5 V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		
V_{IH}	Logic "1" input voltage	2.3	—	—	V	$I_O = 2 mA$
V_{IL}	Logic "0" input voltage	—	—	0.7		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.05	0.2		
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{IN+}	Logic "1" input bias current	—	5	40	μA	$V_{IN} = 5 V$
I_{IN-}	Logic "0" input bias current	—	1.0	5.0		$V_{IN} = 0 V$
I_{O+}	Output high short circuit pulse current	60	290	—	mA	$V_O = 0 V$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	130	600	—		

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15 V, $V_S = COM$, $C_L = 1000 pF$ and $T_A = 25 °C$ unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	90	150	210	ns	$V_S = 0 V$
t_{off}	Turn-off propagation delay	90	150	210		$V_S = 0 V$ or 600 V
t_r	Turn-on rise time	—	70	120		
t_f	Turn-off fall time	—	35	60		
DT	Deadtime	80	100	190		
MT	Delay matching, HS & LS turn-on/off	—	—	50		

Functional Block Diagram



Lead Definitions

Symbol	Description
VCC	Low-side supply voltage
COM	Logic ground and low-side driver return
HIN	Logic input for high-side gate driver output
LIN	Logic input for low-side gate driver output
VB	High-side floating supply
HO	High-side driver output
VS	High voltage floating supply return
LO	Low-side driver output

Lead Assignments

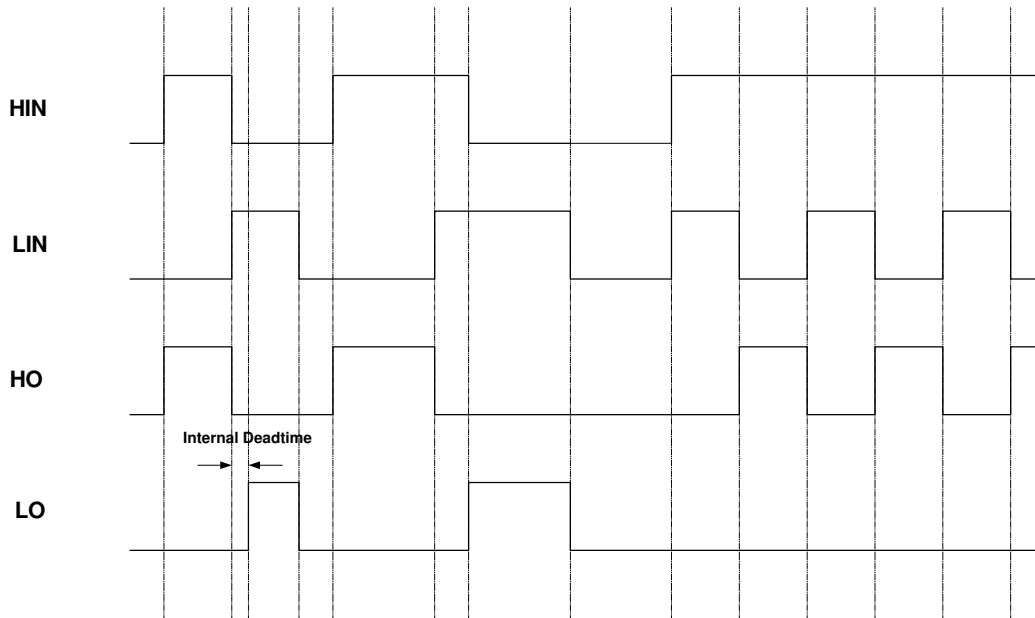
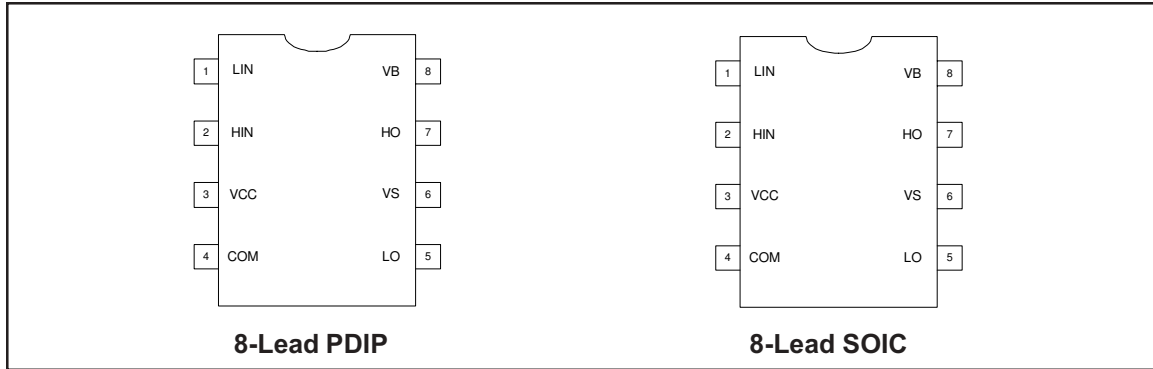


Figure 1. Input/Output Functionality Diagram

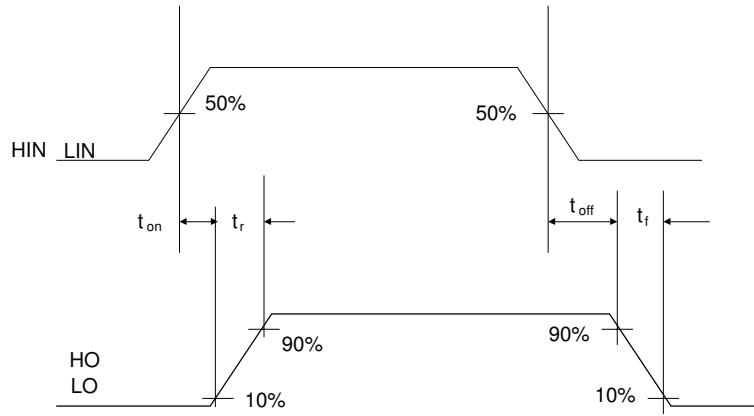


Figure 2. Switching Time Waveforms

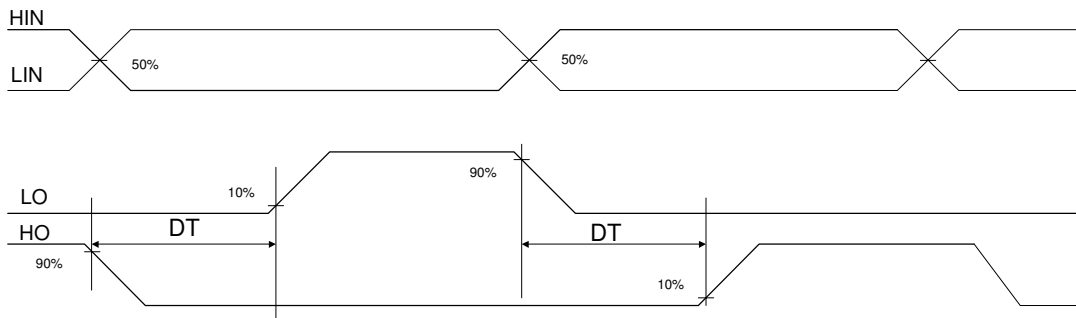


Figure 3. Internal Deadtime Timing

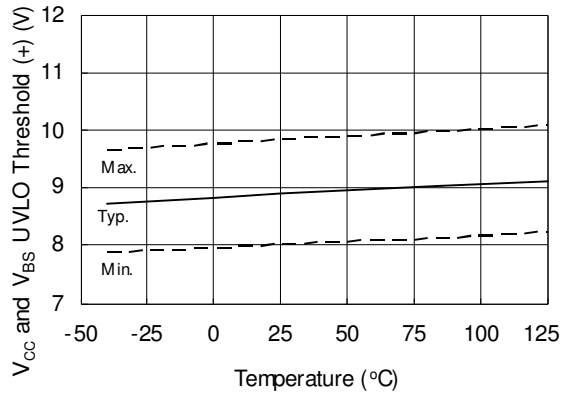


Figure 4. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature

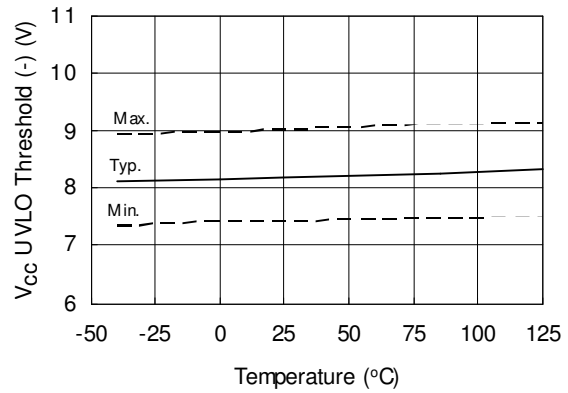


Figure 5. V_{CC} / V_{DD} Undervoltage Threshold (-) vs. Temperature

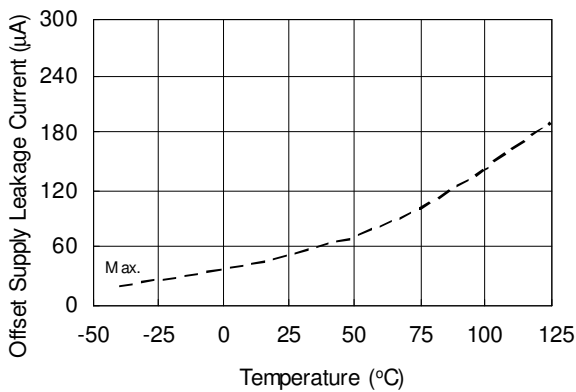


Figure 6A. Offset Supply Leakage Current vs. Temperature

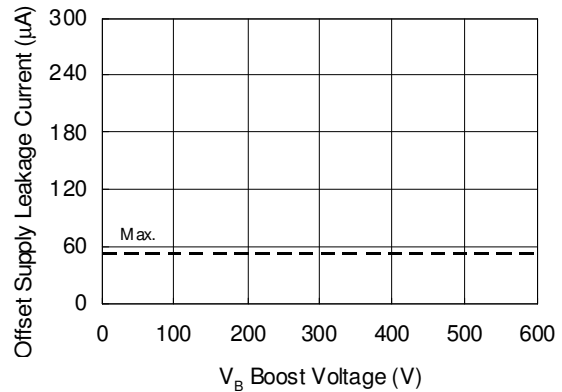


Figure 6B. Offset Supply Leakage Current vs. Supply Voltage

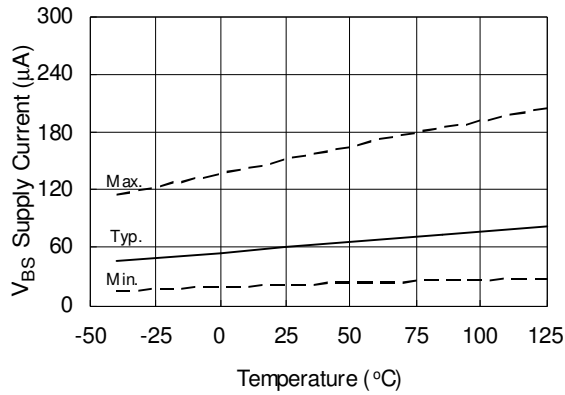


Figure 7A. V_{BS} Supply Current vs. Temperature

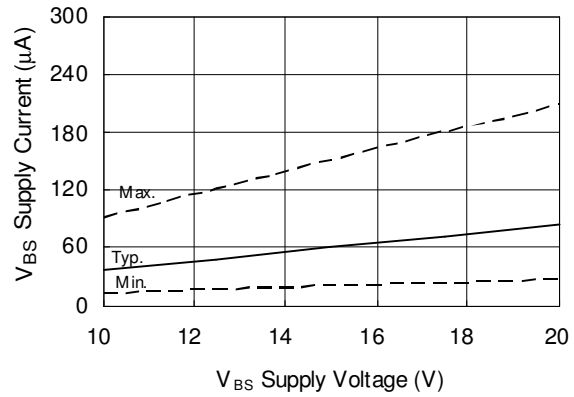


Figure 7B. V_{BS} Supply Current vs. Supply Voltage

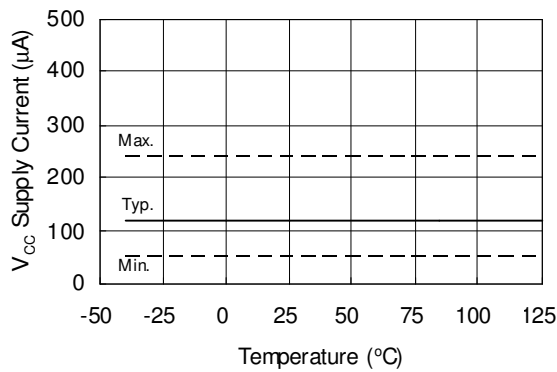


Figure 8A. Quiescent V_{CC} Supply Current vs. Temperature

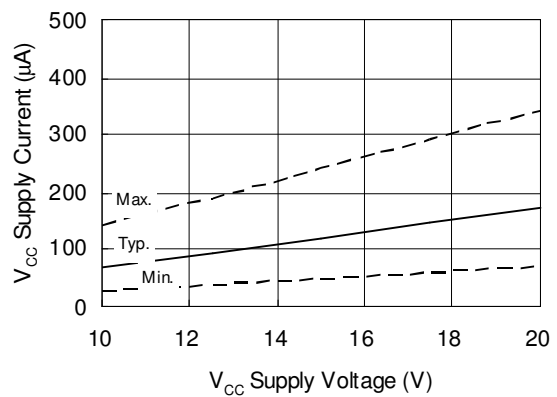


Figure 8B. Quiescent V_{CC} Supply Current vs. Supply Voltage

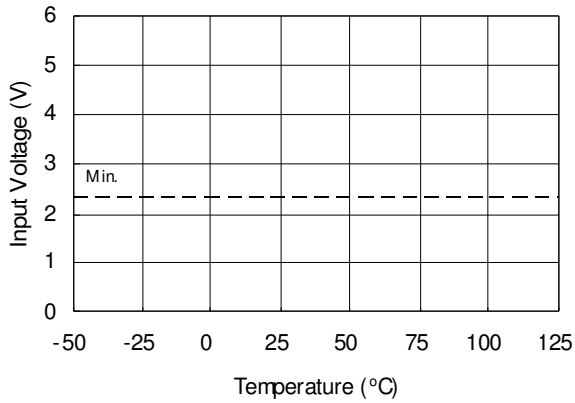


Figure 9A. Logic "1" Input Voltage vs. Temperature

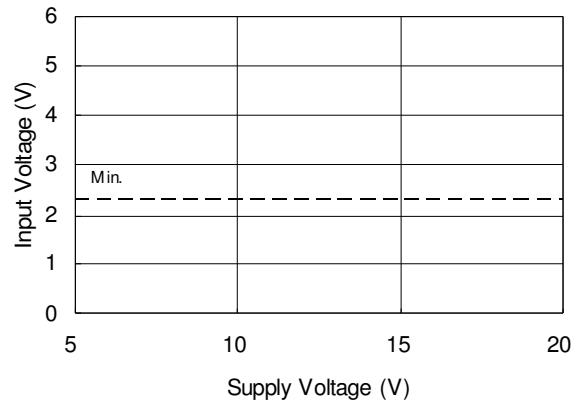


Figure 9B. Logic "1" Input Voltage vs. Supply Voltage

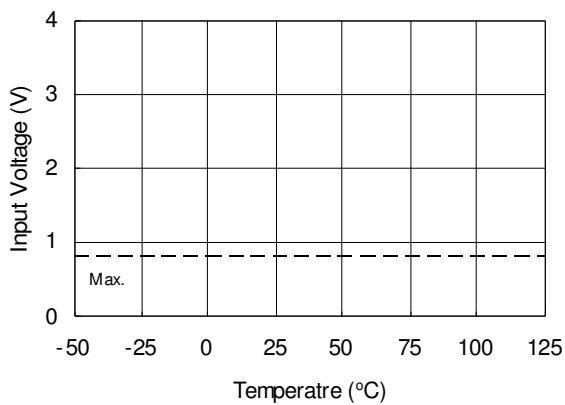


Figure 10A. Logic "0" Input Voltage vs. Temperature

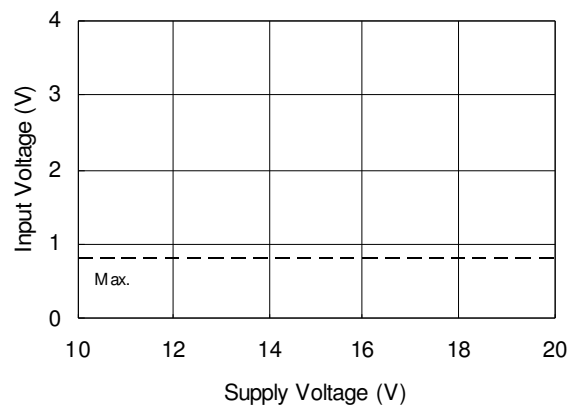


Figure 10B. Logic "0" Input Voltage vs. Supply Voltage

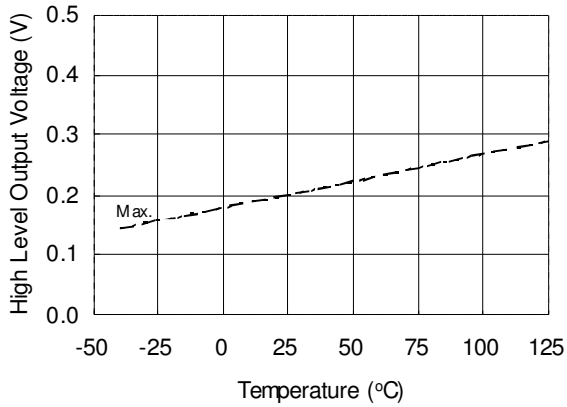


Figure 11A. High Level Output Voltage vs. Temperature ($I_O = 2\text{ mA}$)

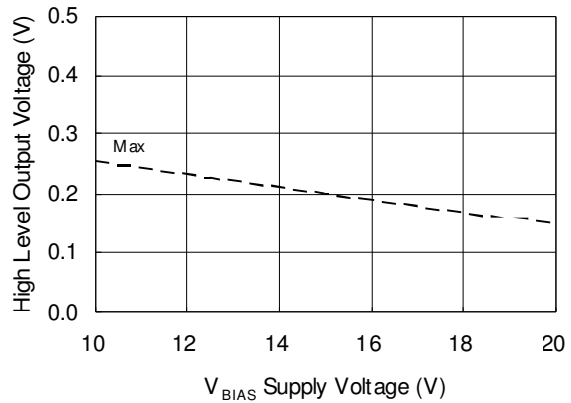


Figure 11B. High Level Output Voltage vs. Supply Voltage ($I_O = 2\text{ mA}$)

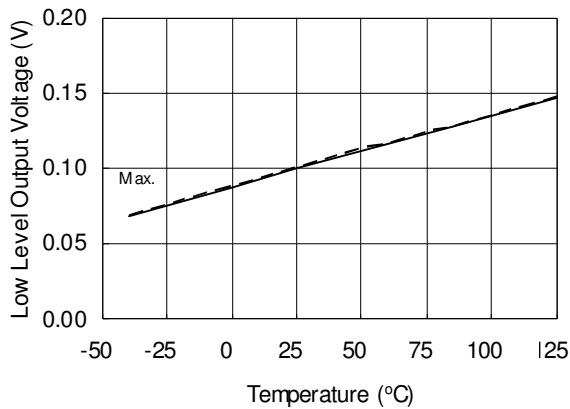


Figure 12A. Low Level Output Voltage vs. Temperature ($I_O = 2\text{ mA}$)

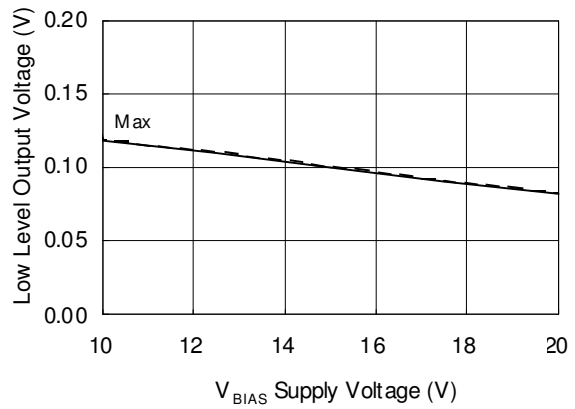


Figure 12B. Low Level Output vs. Supply Voltage ($I_O = 2\text{ mA}$)

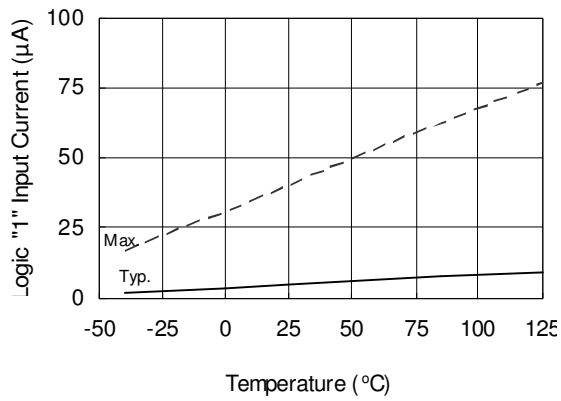


Figure 13A. Logic "1" Input Current vs. Temperature

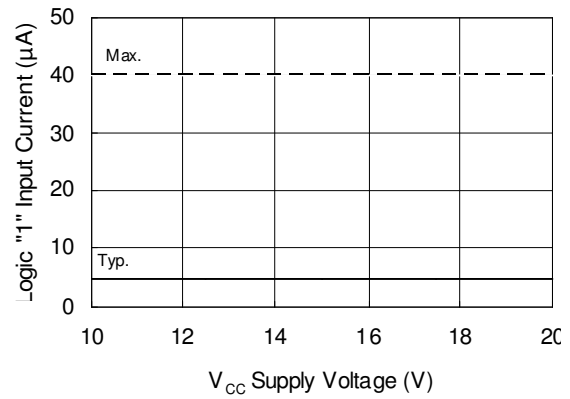


Figure 13B. Logic "1" Input Current vs. Supply Voltage

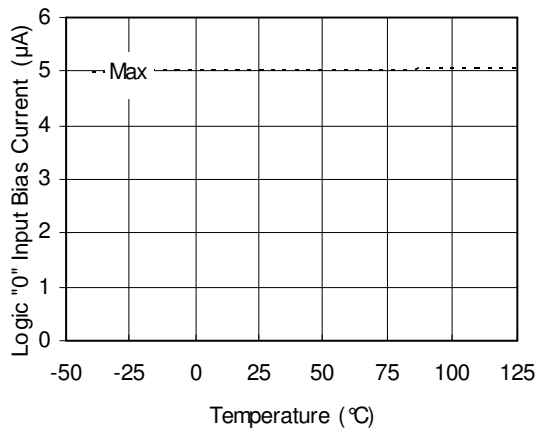


Figure 14A. Logic "0" Input Bias Current vs. Temperature

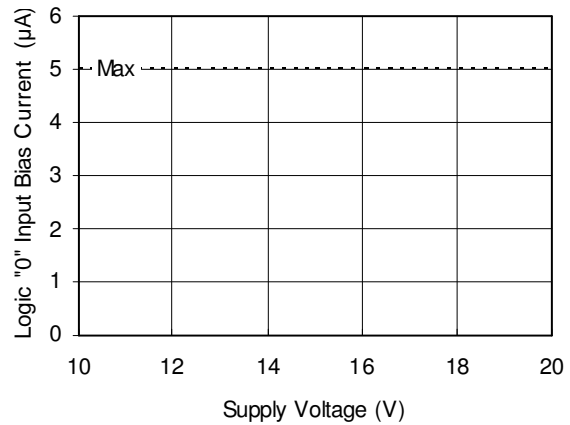


Figure 14B. Logic "0" Input Bias Current vs. Voltage

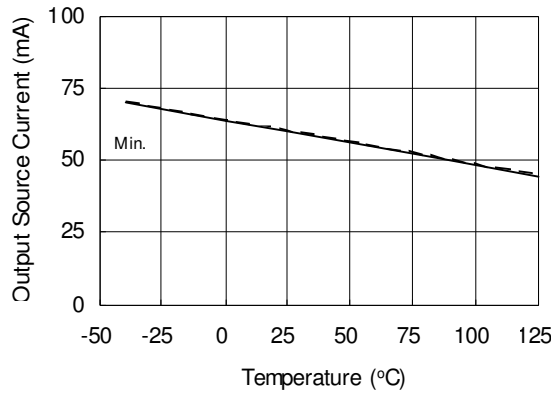


Figure 15A. Output Source Current vs. Temperature

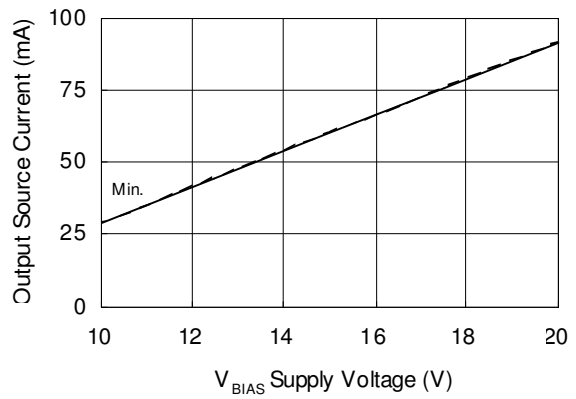


Figure 15B. Output Source Current vs. Supply Voltage

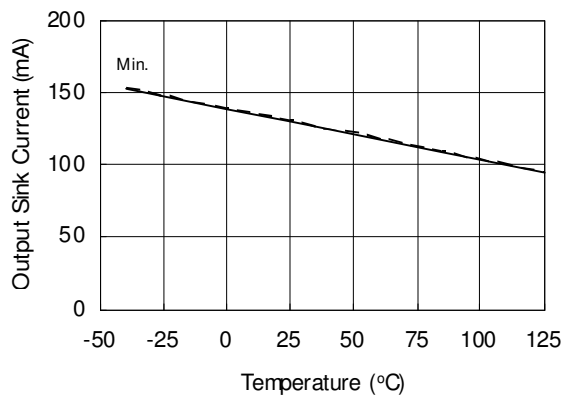


Figure 16A. Output Sink Current vs. Temperature

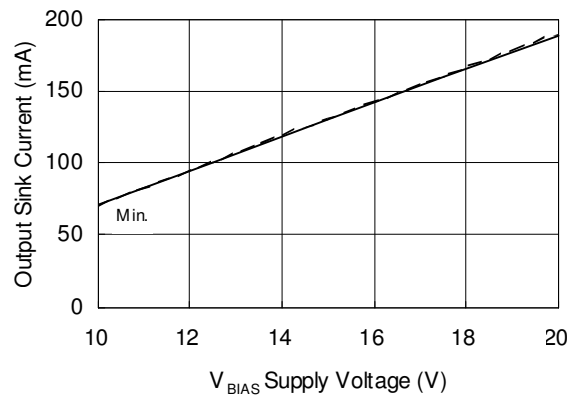


Figure 16B. Output Sink Current vs. Supply Voltage

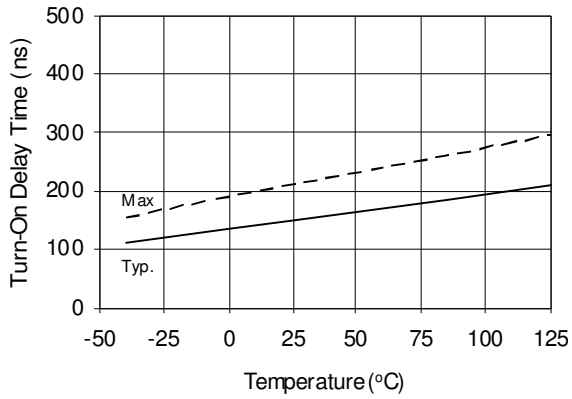


Figure 17A. Turn-On Propagation Delay vs. Temperature

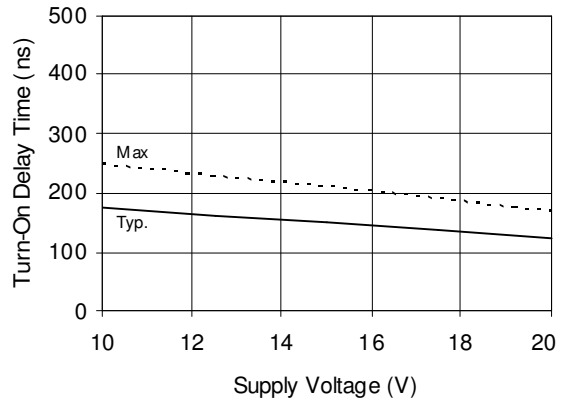


Figure 17B. Turn-On Propagation Delay vs. Supply Voltage

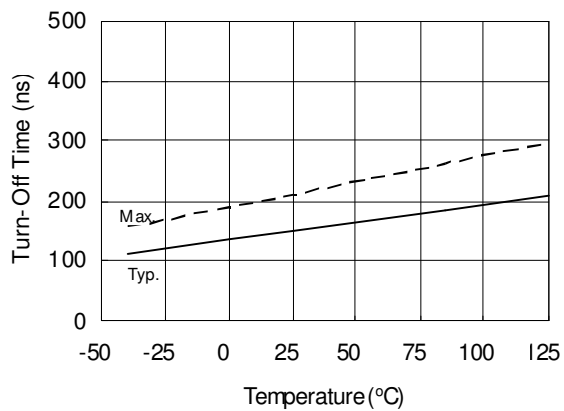


Figure 18A. Turn-Off Propagation Delay vs. Temperature

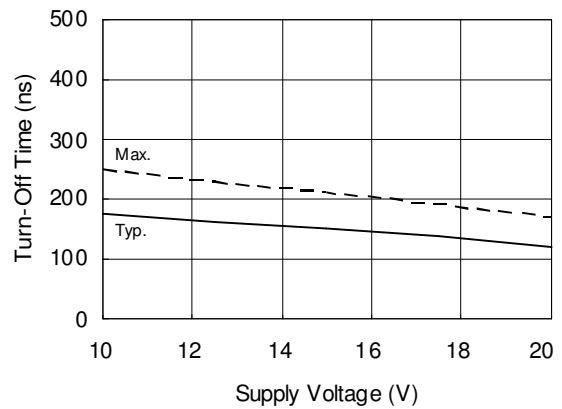


Figure 18B. Turn-Off Propagation Delay vs. Supply Voltage

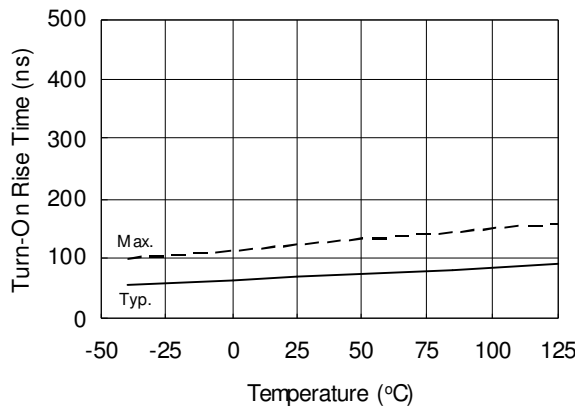


Figure 19A. Turn-On Rise Time vs. Temperature

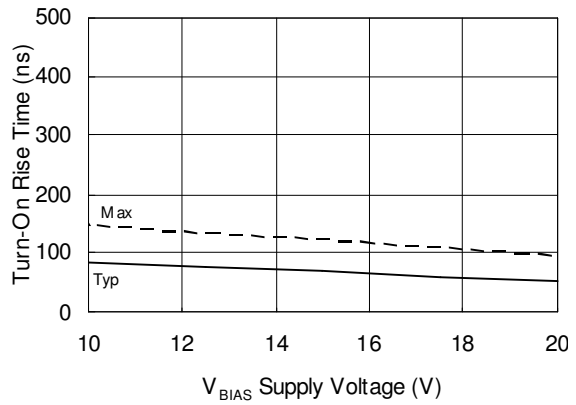


Figure 19B. Turn-On Rise Time vs. Supply Voltage

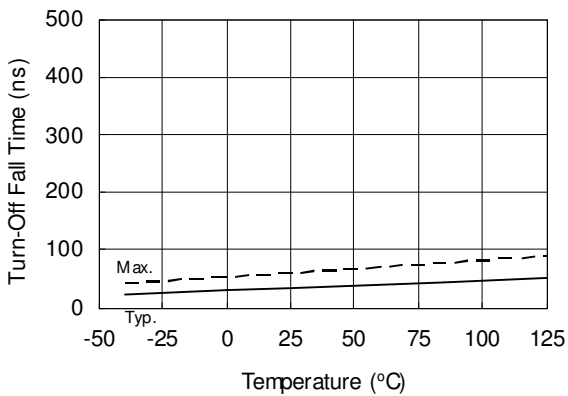


Figure 20A. Turn-Off Fall Time vs. Temperature

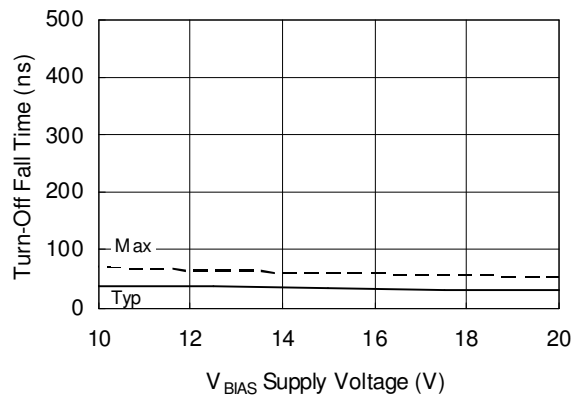


Figure 20B. Turn-Off Fall Time vs. Supply voltage

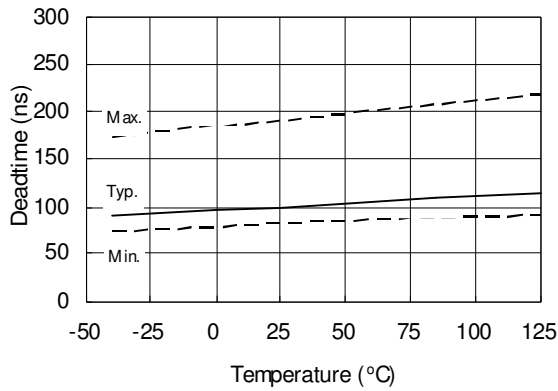


Figure 21A. Deadtime vs. Temperature

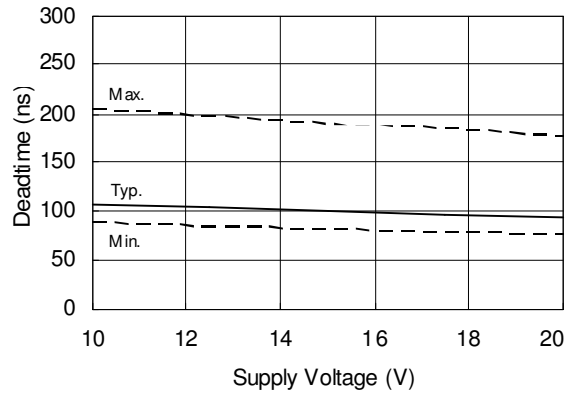


Figure 21B. Deadtime vs. Supply Voltage

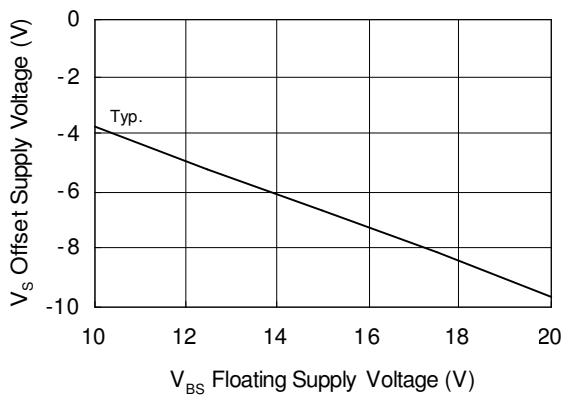


Figure 22. Maximum V_s Negative Offset vs. Supply Voltage

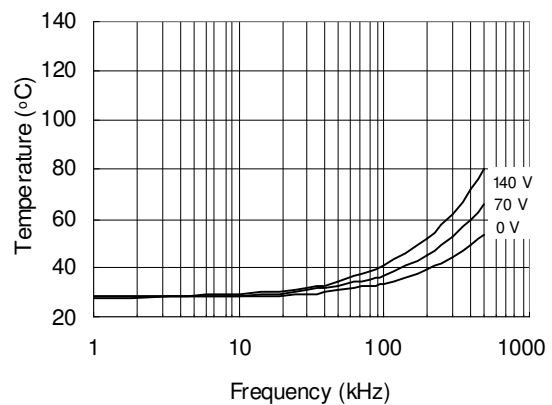


Figure 23. IRS2304 vs. Frequency (IRFBC20),
R_{gate}=33 Ω, V_{CC}=15 V

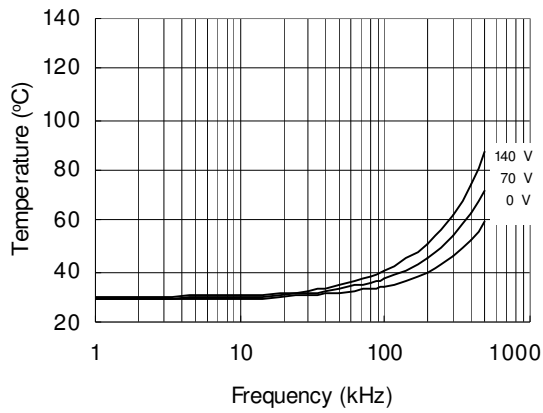


Figure 24. IRS2304 vs. Frequency (IRFBC30)
R_{gate} = 22 Ω, V_{CC} = 15 V

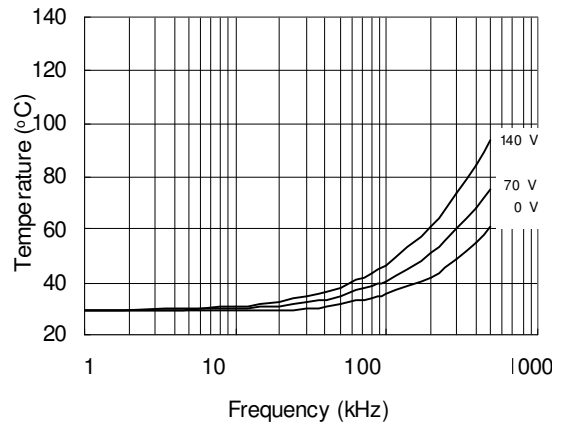


Figure 25. IRS2304 vs. Frequency (IRFBC40),
R_{gate} = 15 Ω, V_{CC} = 15 V

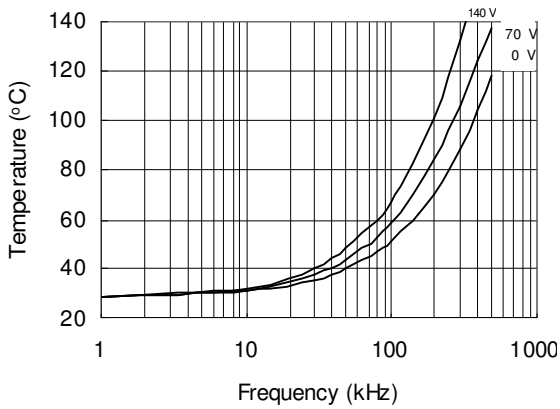


Figure 26. IRS2304 vs. Frequency (IRFPE50),
R_{gate} = 10 Ω, V_{CC} = 15 V

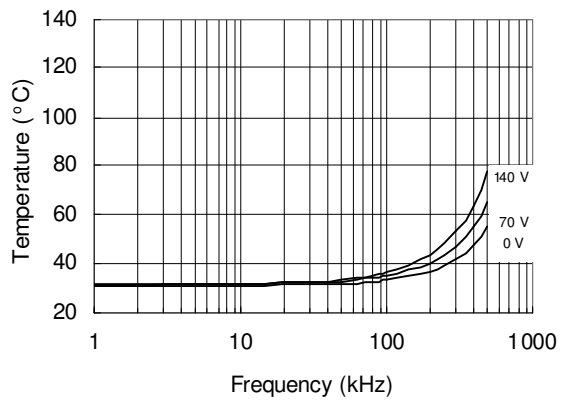
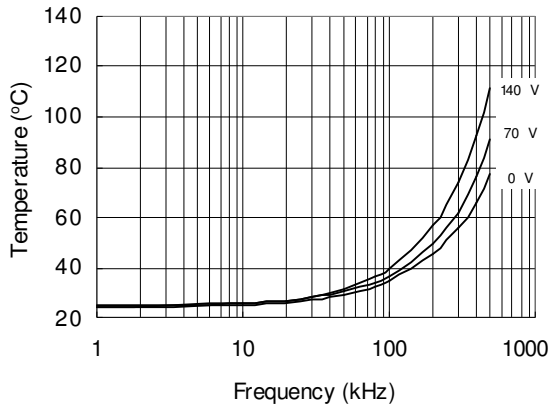
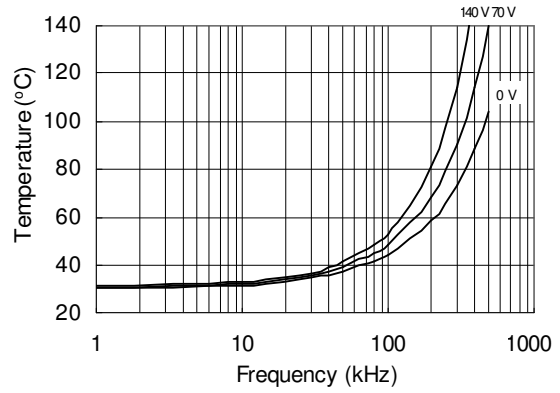


Figure 27. IRS2304S vs. Frequency (IRFBC20)
R_{gate} = 33 Ω, V_{CC} = 15 V

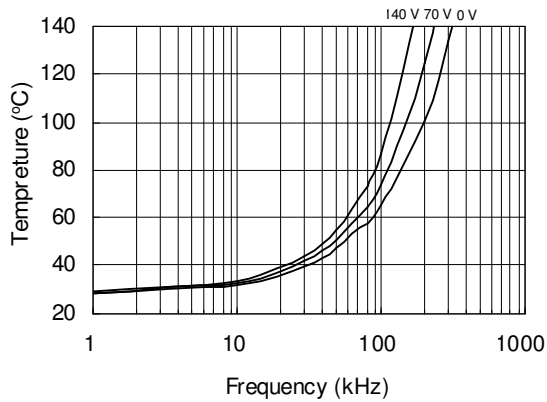
IRS2304(S)PbF



**Figure 28. IRS2304S vs. Frequency (IRFBC30),
 $R_{gate} = 22 \Omega$, $V_{CC} = 15 V$**

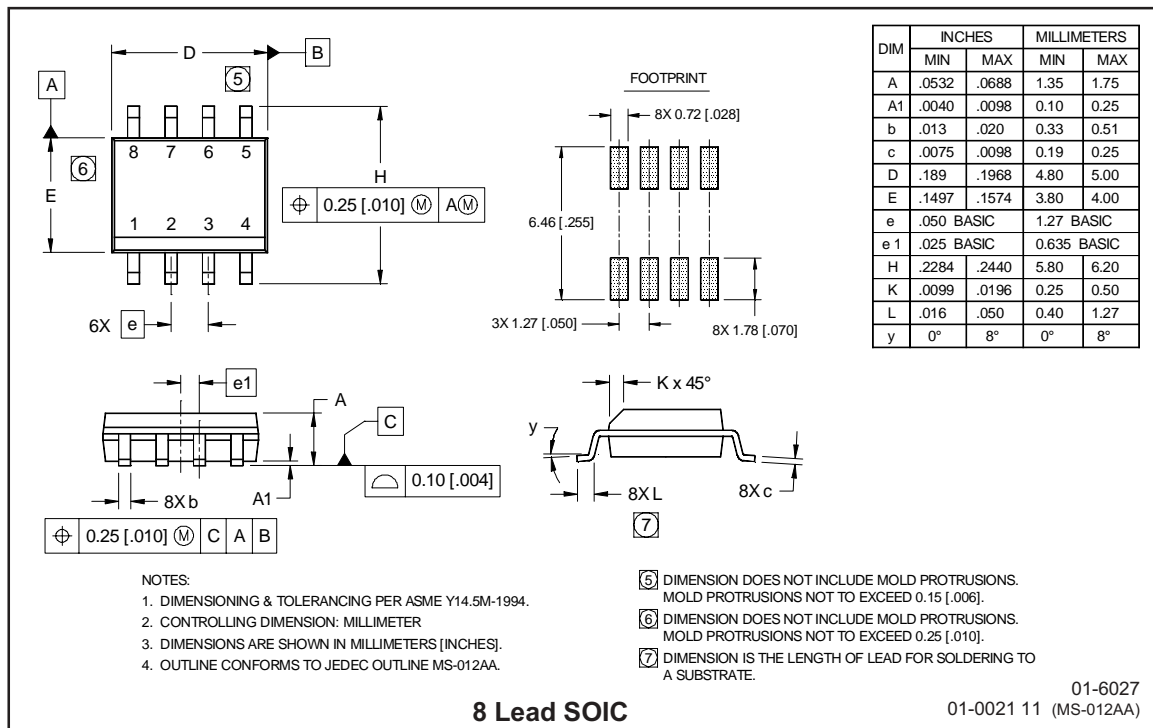
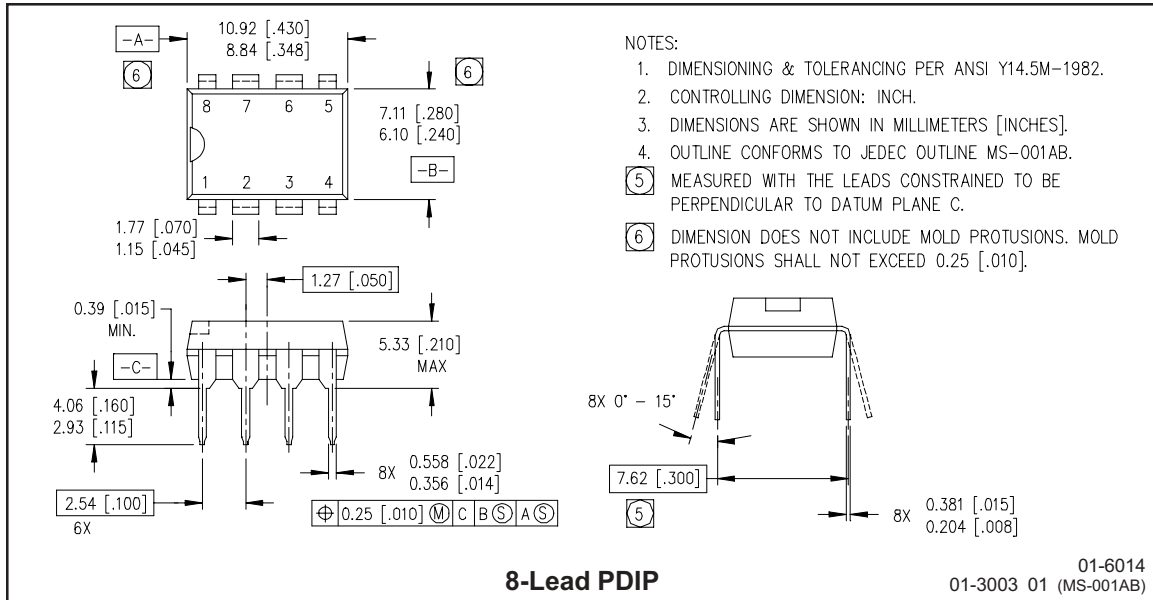


**Figure 29. IRS2304S vs. Frequency (IRFBC40),
 $R_{gate} = 15 \Omega$, $V_{CC} = 15 V$**

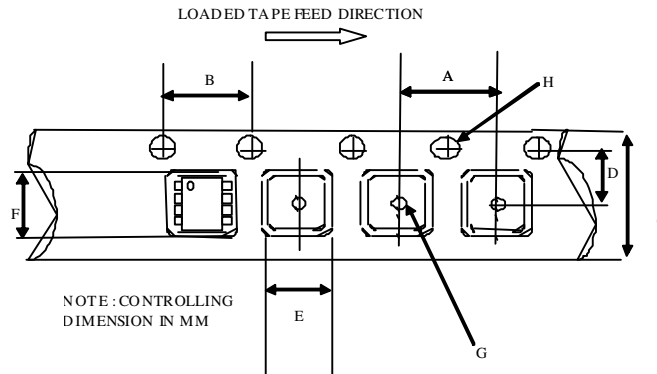


**Figure 30. IR2304s vs. Frequency (IRFPB50),
 $R_{gate} = 10 \Omega$, $V_{CC} = 15 V$**

Case outlines

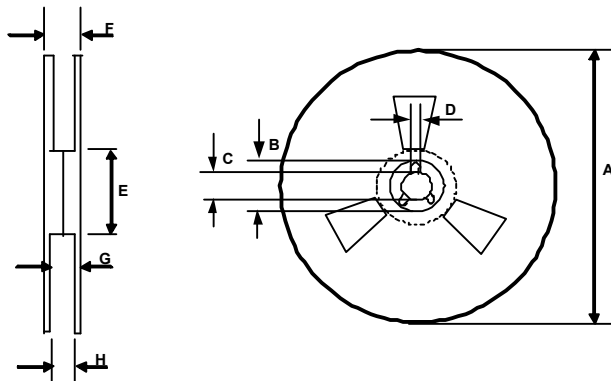


Tape & Reel 8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

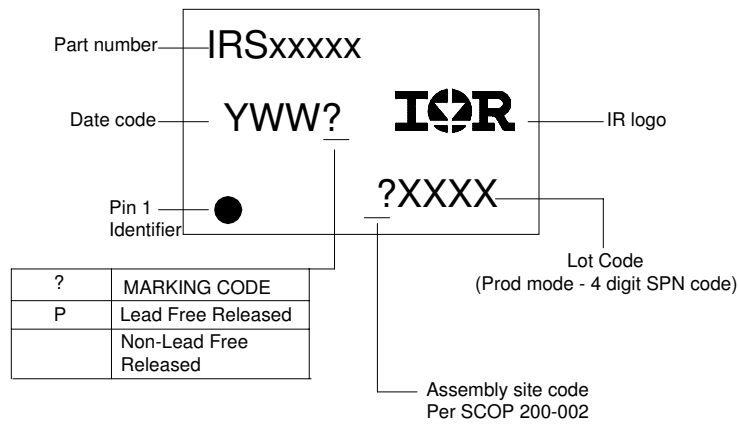
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

- 8-Lead PDIP IRS2304PbF
- 8-Lead SOIC IRS2304SPbF
- 8-Lead SOIC Tape & Reel IRS2304STRPbF