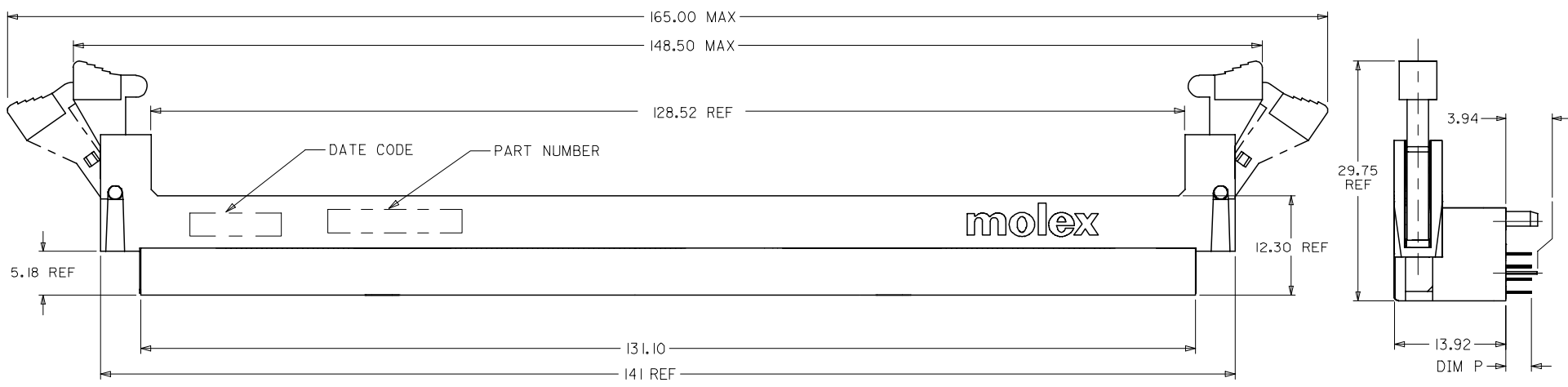
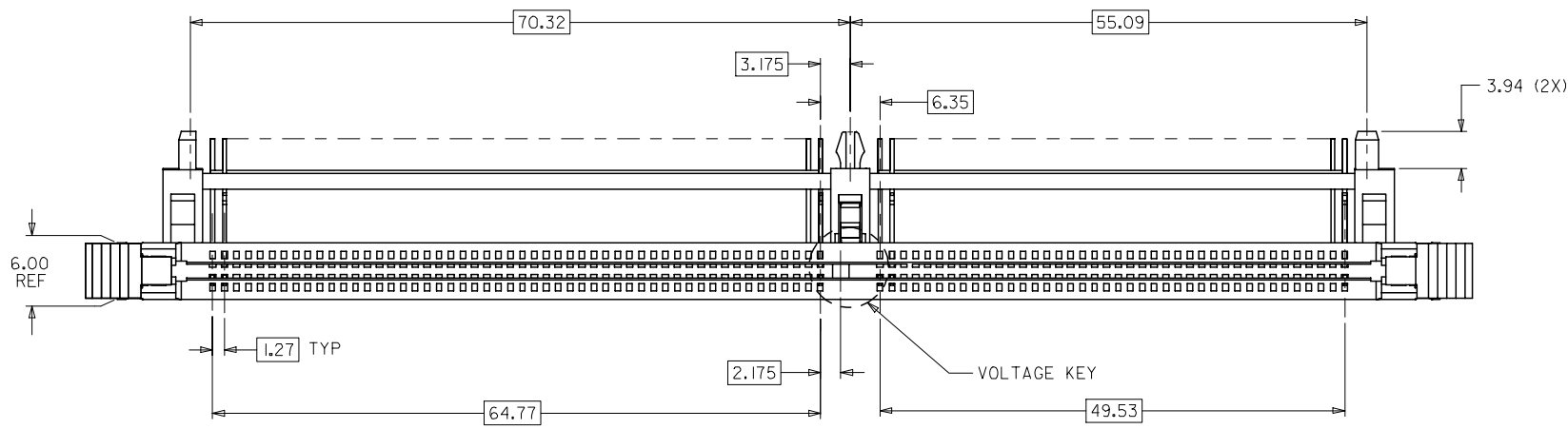


10 9 8 7 6 5 4 3 2 1



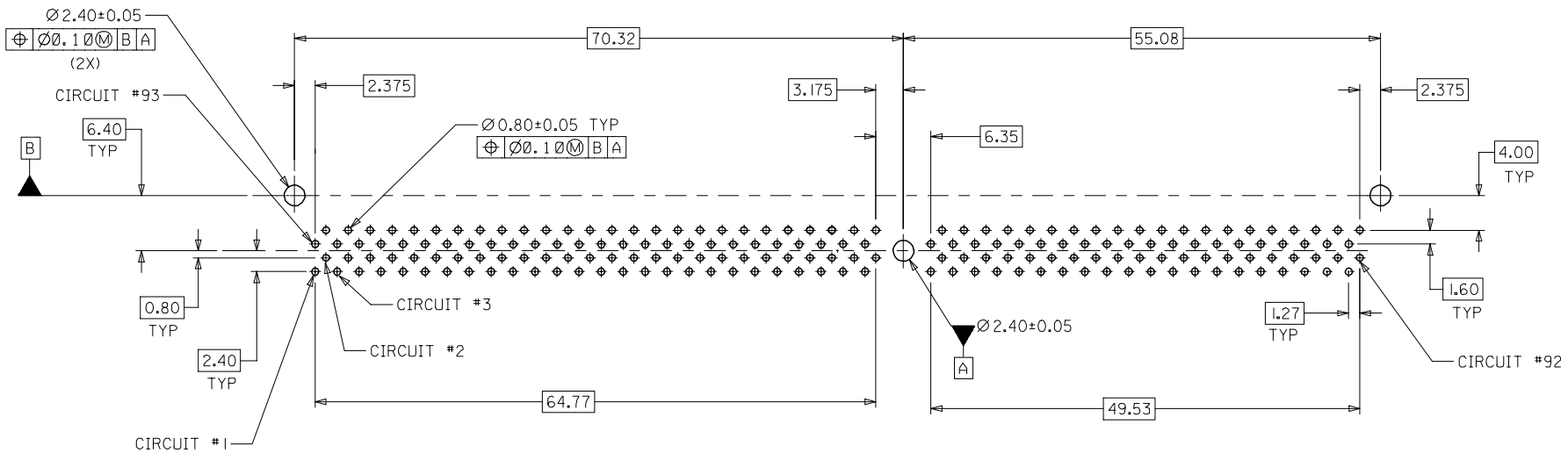
- NOTES:
- MATERIALS: HOUSING, BASEPLATE AND LATCH - HIGH TEMPERATURE THERMOPLASTIC, UL 94-V0 TERMINAL AND FORKLOCK - COPPER ALLOY
 - FINISHES: CONTACT AREA: 0.38um/15u" MIN. GOLD
SOLDER TAIL: 2.54um/100u" MIN. TIN/LEAD OR TIN
UNDERPLATE: 1.27um/50u" MIN. NICKEL

- PRODUCT SPECIFICATIONS: PS-87609-002 FOR PERFORMANCE SPECIFICATIONS.
- DATE CODE SHALL BE MARKED LEGIBLY AS SHOWN: XX XX YEAR WEEK
- PART NUMBER SHALL BE MARKED LEGIBLY AS SHOWN: 87655-OXXX REFER TO TABLE

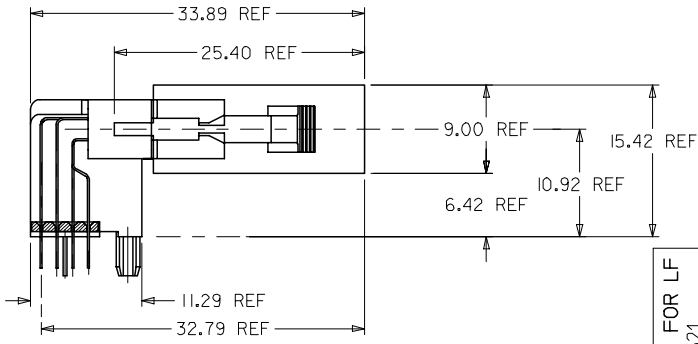
ADD ASSY P/N FOR LF EC NO: S2004-0521 DRAWN:MLONG 2004/09/08 CHKD:ATSEE 2004/09/08 APPR:SKTOH 2004/09/09	QUALITY SYMBOLS ▽=0 ▽=0	GENERAL TOLERANCES (UNLESS SPECIFIED)		DIMENSION STYLE MM ONLY	SCALE NTS	DESIGN UNITS METRIC	THIRD ANGLE PROJECTION	
		4 PLACES ± --- ± ---	3 PLACES ± --- ± ---	2 PLACES ± 0.25 ± ---	1 PLACE ± --- ± ---	ANGULAR ± 5 °	DRAWN BY MLONG	DATE 2000/12/21
REV	DESCRIPTION	DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		SEE TABLE	APPROVED BY SKTOH	DATE 2000/12/29	MOLEX INCORPORATED	
				SIZE A3	MATERIAL NO.	DOCUMENT NO. SD-87655-001	SHEET NO. 1 OF 3	

9 8 7 6 5 4 3 2 1

PLATING OPTION	MATERIAL NO.	VOLTAGE KEY	TAIL LENGTH P±0.25	RECOMMENDED PCB THICKNESS
TIN/LEAD	87655-0001	LEFT (2.5V)	2.79	1.57
	87655-0002		3.18	
TIN	87655-0004	LEFT (2.5V)	2.79	1.57
	87655-0005		3.18	



RECOMMENDED
P.C. BOARD HOLE PATTERN
(CONNECTOR SIDE)



ACTUAL MODULE HEIGHT AND CLEARANCE
WHEN USING A 9.00MM THICK BY 25.40MM HEIGHT
MODULE (TYPICAL SOJ PACKAGING).

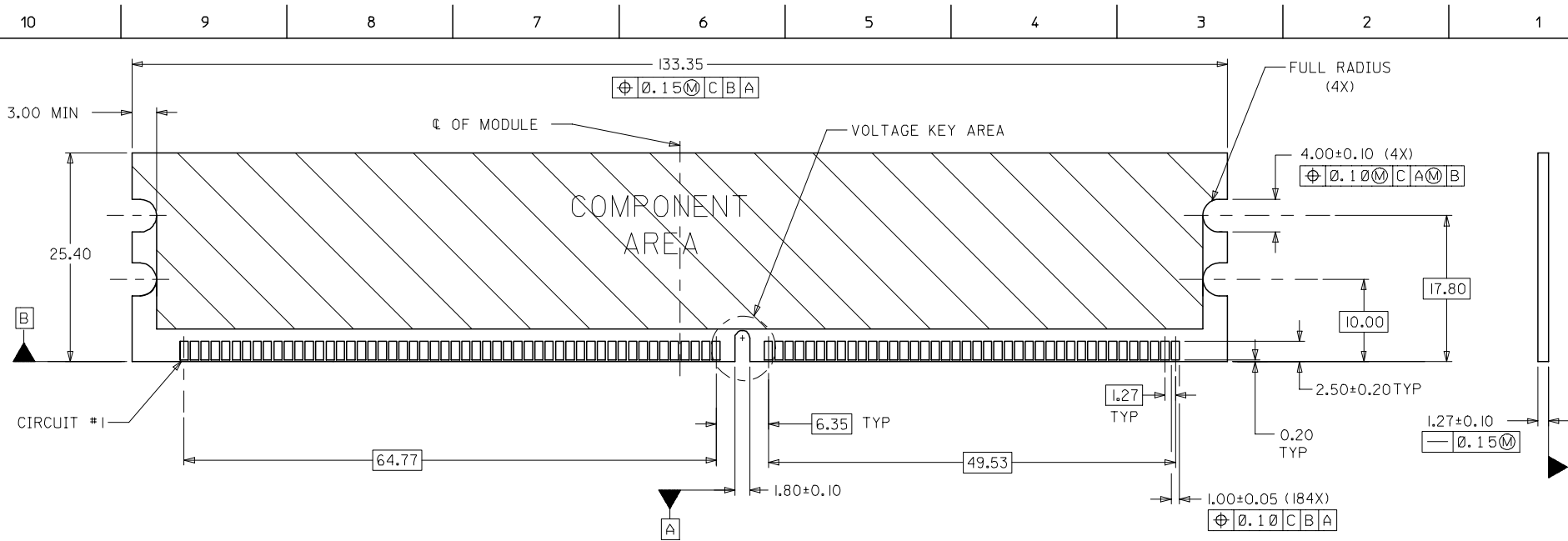
REV	DESCRIPTION
1	ADD ASSY P/N FOR LF
2	EC NO: S2004-0521
3	DRWN:MLONG 2004/09/08
4	CHKD:ATSEE 2004/09/08
5	APPR:SKTOH 2004/09/09

QUALITY SYMBOLS	▽=0
	∇=0

GENERAL TOLERANCES (UNLESS SPECIFIED)	
	ANGULAR ± 5 °
4 PLACES	± ---
3 PLACES	± ---
2 PLACES	± 0.25
1 PLACE	± ---

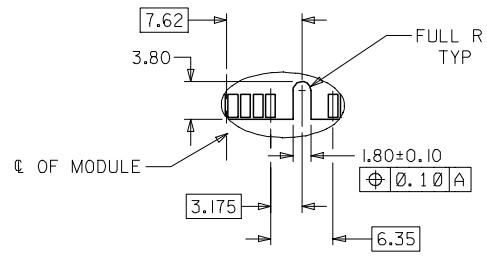
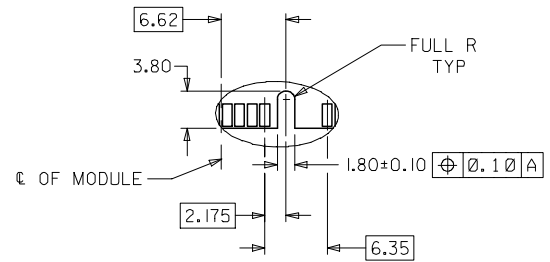
DIMENSION STYLE	
MM ONLY	
DRAWN BY	DATE
MLONG	2000/12/15
CHECKED BY	DATE
SQUEK	2000/12/29
APPROVED BY	DATE
SKTOH	2000/12/29
MATERIAL NO.	
SIZE	A3

SCALE	DESIGN UNITS	THIRD ANGLE PROJECTION
NTS	METRIC	☉ □
TITLE		
SALES DRAWING		
DDR DIMM, 1.27MM PITCH		
184 CKTS, R/A		
MOLEX INCORPORATED		
DOCUMENT NO.	SHEET NO.	
SD-87655-001	2 OF 3	



RECOMMENDED MODULE LAYOUT
 (PER JEDEC STANDARD MO-206, 184 CKT.)
 UNLESS OTHERWISE SPECIFIED, GENERAL TOLERANCE FOR MODULE = ±0.13

VOLTAGE KEY AREA OPTIONS



OFFSET LEFT KEY
 (2.5 VOLTS)

CENTERED KEY
 (1.8 VOLTS)

ADD ASSY P/N FOR LF EC NO: S2004-0521 DRAWN: MLONG 2004/09/08 CHKD: ATSEE 2004/09/08 APPR: SKTOH 2004/09/09	QUALITY SYMBOLS ▽=0 ▽=0	GENERAL TOLERANCES (UNLESS SPECIFIED)		DIMENSION STYLE MM ONLY	SCALE NTS	DESIGN UNITS METRIC	THIRD ANGLE PROJECTION	
		4 PLACES ± --- ± ---	mm INCH	DRAWN BY MLONG	DATE 2000/12/21	TITLE SALES DRAWING DDR DIMM, 1.27MM PITCH 184 CKTS, R/A		
		3 PLACES ± --- ± ---	± 0.25 ± ---	CHECKED BY SQUEK	DATE 2000/12/29	MOLEX INCORPORATED		
		2 PLACES ± --- ± ---	± --- ± ---	APPROVED BY SKTOH	DATE 2000/12/29	DOCUMENT NO. SD-87655-001	SHEET NO. 3 OF 3	
1 PLACE ± --- ± ---	ANGULAR ± 5 °	DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		MATERIAL NO. SEE TABLE	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION			