Ordering number : EN*A2275

LC87F2K08A

Advance Information

ON Semiconductor®

http://onsemi.com

CMOS LSI

8-bit Microcontroller

8K-Byte Flash ROM / 256-Byte RAM / 24-pin

Overview

The LC87F2K08A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 8K-byte flash ROM (onboard programmable), 256-byte RAM, an on-chip debugger function, two sophisticated 16-bit timers/counters (may be divided into 8-bit timers), an asynchronous/synchronous SIO interface, a 5-channel AD converter with 12/8-bit resolution selector, eight analog comparators, two AMP circuits, an IGBT control circuit (PPG), a watchdog timer, an internal reset circuit, a system clock frequency divider, and a 18-source 10-vector interrupt feature.
It is optimal for controlling the IH cooking heaters and other appliances.

Features

■ Flash ROM
- 8192 × 8 bits
- Capable of on-board programming with a power voltage range of 4.5 to 5.5V
- Block-erasable in 128 byte units
- Writing in 2-byte units

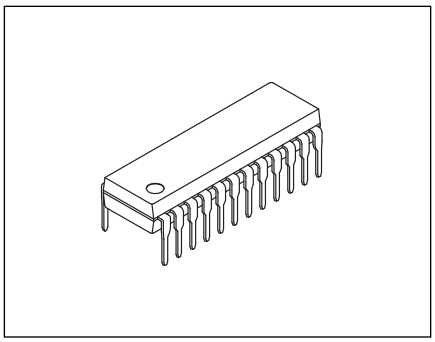
■ ROM
- 256 × 9 bits

■ Package : DIP24S(300mil), Lead-free type

■ Minimum bus cycle time
- 83.3ns (12MHz)

Note : The bus cycle time here refers to the ROM read speed.

■ Minimum instruction cycle time
- 250ns (12MHz)



DIP24S(300mil)

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

■ Ports

- I/O ports
  Ports I/O direction can be designated in 1 bit units: 9 (P00 to P07, P30)
- Dedicated PPG ports 10 (PPGO, AMP1I, AMP2O, CMP1IA, CMP1IB, CMP2I, CMP4I, CMP45I, CMP5I, CMP6I)
- Reset pin 1 (RES#)
- Dedicated on-chip debugger pin 1 (OWP0)
- Power pins 3 (VSS1, VSS2, VDD1)

■ Timers

- Timer 0: 16-bit timer/counter with a capture register
  - Mode 0 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) ×2 channels
  - Mode 1 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  - Mode 2 : 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3 : 16-bit counter (with a 16-bit capture register)
- Timer 1 : 16-bit timer/counter
  - Mode 0 : 8-bit timer with an 8-bit prescaler + 8-bit timer/counter with an 8-bit prescaler
  - Mode 2 : 16-bit timer/counter with an 8-bit prescaler
  - Mode 3 : 16-bit timer with an 8-bit prescaler
- Timer 6 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1) The clock is selectable from the system clock and timer 0 prescaler output.
  2) Interrupts are programmable in 5 different time schemes.

■ Serial interface

- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0 : Synchronous 8-bit serial I/O (2-wire configuration, 2 to 512 Tcyc transfer clocks)
  - Mode 2 : Bus mode 1 (start bit, 8 data bits, 2 to 512 Tcyc transfer clocks)
  - Mode 3 : Bus mode 2 (start detect, 8 data bits, stop detect)

■ UART

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

■ AD converter : 12 bits ×5 channels

- 12/8 bits AD converter resolution selectable

■ Clock output function

- Can generate clock outputs with a frequency of $\frac{1}{1}$, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$, or $\frac{1}{64}$ of the source clock selected as the system clock.

■ Analog comparator : 8 channels

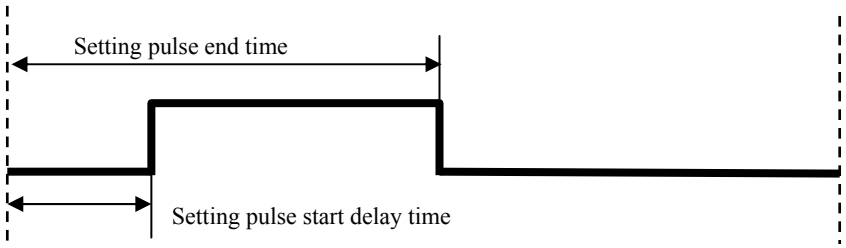
- CMP1: "+" and "–" input pins
  Output: For PPG output timing generation and capture timer input (INT2)
- CMP2: "+" input pin, "–" input is the internal Vref set to 2/3 V_{DD}
  Output for interrupt flag setting (INT0)
- CMP3: "+" input is the output of AMP1.
  "–" input is the internal Vref (user selectable options: 1/6, 2/6, 3/6, or 4/6 V_{DD}).
  Output for the PPG output control (only the existing cycle set to OFF) and interrupt flag set (INT1)
- CMP4: "+" and "–" input pins
  Output for the PPG output control (forced OFF)
- CMP5: "–" input pin, "+" input is multiplexed with the "–" input pin of CMP4
  Output for the PPG output control (forced OFF)
- CMP6: "+" input pin, "–" input is the internal Vref (register setting: 1/6, 2/6, 3/6, or 4/6 V_{DD})
  Output for the PPG output control (forced OFF) and interrupt flag set (CMP6)
- CMP7: "+" input is multiplexed with the "+" input pin of CMP1
  "–" input is the internal Vref (user selectable options: 1/20 or 2/20 V_{DD})
  Output for the PPG output control and sets the interrupt flag (INT3).
- CMP8: "+" input is multiplexed with the "+" input pin of CMP4
  "–" input is the internal Vref (user selectable options: 12/20, 13/20, or 14/20 V_{DD})
  Output for the PPG output control (forced OFF).

■ AMP circuit: 2 channels

- AMP1: The gain is set by user selectable options (6×/8×/10×).
  Input pin (AMP1I)
  Output is CMP3 input and AMP2 input.
- AMP2: The gain (1×/2×/4×) is set by using a register.
  Input is AMP1 output.
  Output pin (AMP2O)

■ Pulse output control circuit (PPG output): 1 channel

- Output sync signal switching: Set by a register (1-pulse output / continuous pulse output synchronized with the CMP1 output)
- Duty control: Pulse start delay time and pulse end time with respect to a sync signal are set by using a register.
- PPG output control using CMP3 to CMP8 outputs
- Surge detection using CMP4/5/6/8 outputs
- CMP1 output: Pulse signal timing detection
- Output polarity selectable: User selectable options



■ Watchdog timer

- Can generate an internal reset signal on an overflow of timer that runs on the WDT-dedicated low-speed RC oscillation clock (30kHz).
- Allows selection of continue, stop, or hold mode operation of the counter on entry into the HALT/HOLD mode.

■ Interrupts

- 18 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, an interrupt into the smallest vector address is given priority.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	UART receive
8	0003BH	H or L	SIO1/UART transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	CMP6/Surge detection

- Priority levels X > H > L
- For interrupts of the same level, an interrupt with a smaller vector address is given priority.

■ Subroutine stack levels: Up to 128 levels (the stack is allocated in RAM)

■ Internal high-speed multiplication/division instructions

- 16 bits × 8 bits (5 Tcyc execution time)
- 24 bits × 16 bits (12 Tcyc execution time)
- 16 bits ÷ 8 bits (8 Tcyc execution time)
- 24 bits ÷ 16 bits (12 Tcyc execution time)

■ Oscillation circuits

- Internal oscillation circuits
  1) Low-speed RC oscillation circuit 1 : For system clock (100kHz)
  2) Medium-speed RC oscillation circuit : For system clock (1MHz)
  3) Multi-frequency RC oscillation circuit : For system clock (12MHz)
  4) Low-speed RC oscillation circuit 2 : For watchdog timer (30kHz)

■ System clock divider function

- Can run on low current.
- The minimum instruction cycle selectable from 250 ns, 500 ns, 1 µs, 2 µs, 4 µs, 8 µs, 16 µs, 32 µs, and 64 µs (at a main clock rate of 12 MHz).

■ Internal reset circuit

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) by configuring options.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level (7 levels : 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V) selectable by configuring options.

■ Standby function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are three ways of releasing the HALT mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Occurrence of an interrupt

- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, and crystal oscillators automatically stop operation.
  2) There are four ways of releasing the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Having an interrupt source established at either INT0, INT1, INT2, or INT4
         * INT0 and INT1 HOLD mode release is available only when level detection is set.

■ On-chip debugger

- Supports software debugging with the IC mounted on the target board.

■ Data security function

- Protects the program data stored in flash memory from unauthorized read or copy.
  Note: This data security function does not necessarily provide absolute data security.

■ Development tools

- On-chip debugger: TCB87 Type C + LC87F2K08A

■ Programming board

Package	Programming board
DIP24S	W87F2KD

■ Flash ROM programmer

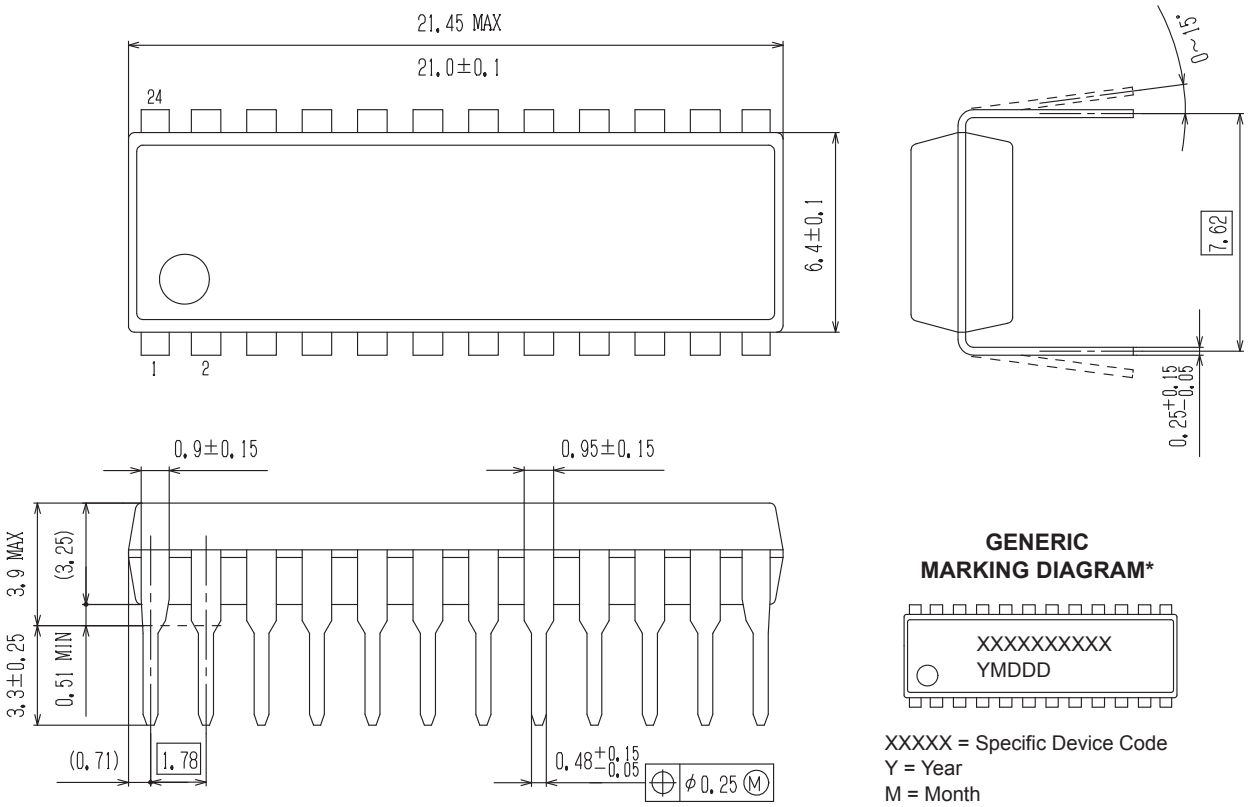
Maker		Model	Supported version	Device
ON Semiconductor	Single/Gang Programmer	SKK/SKK Type B (SanyoFWS)	Application version: 1.05 or later Chip data version: 2.24 or later	LC87F2K08
	Gang Programmer	SKK-4G (SanyoFWS)		

Note : Be sure to check for the latest version.

Package Dimensions

unit : mm

PDIP24 / DIP24S (300 mil)
CASE 646AW
ISSUE A

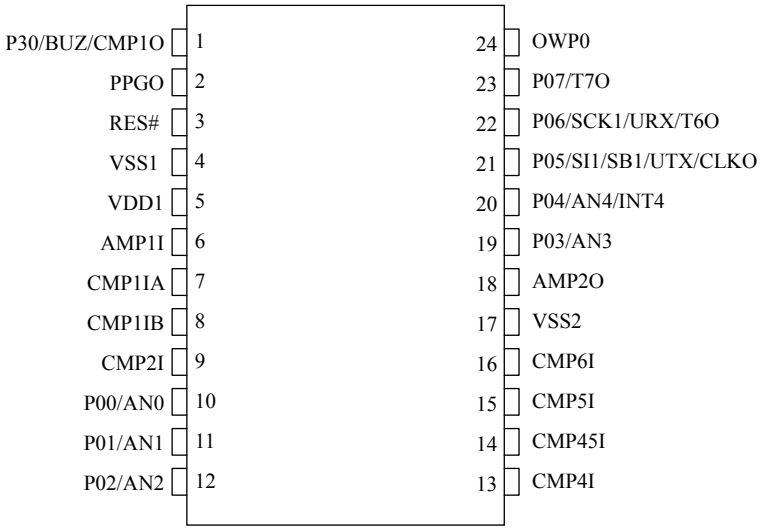


GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

Pin Assignment

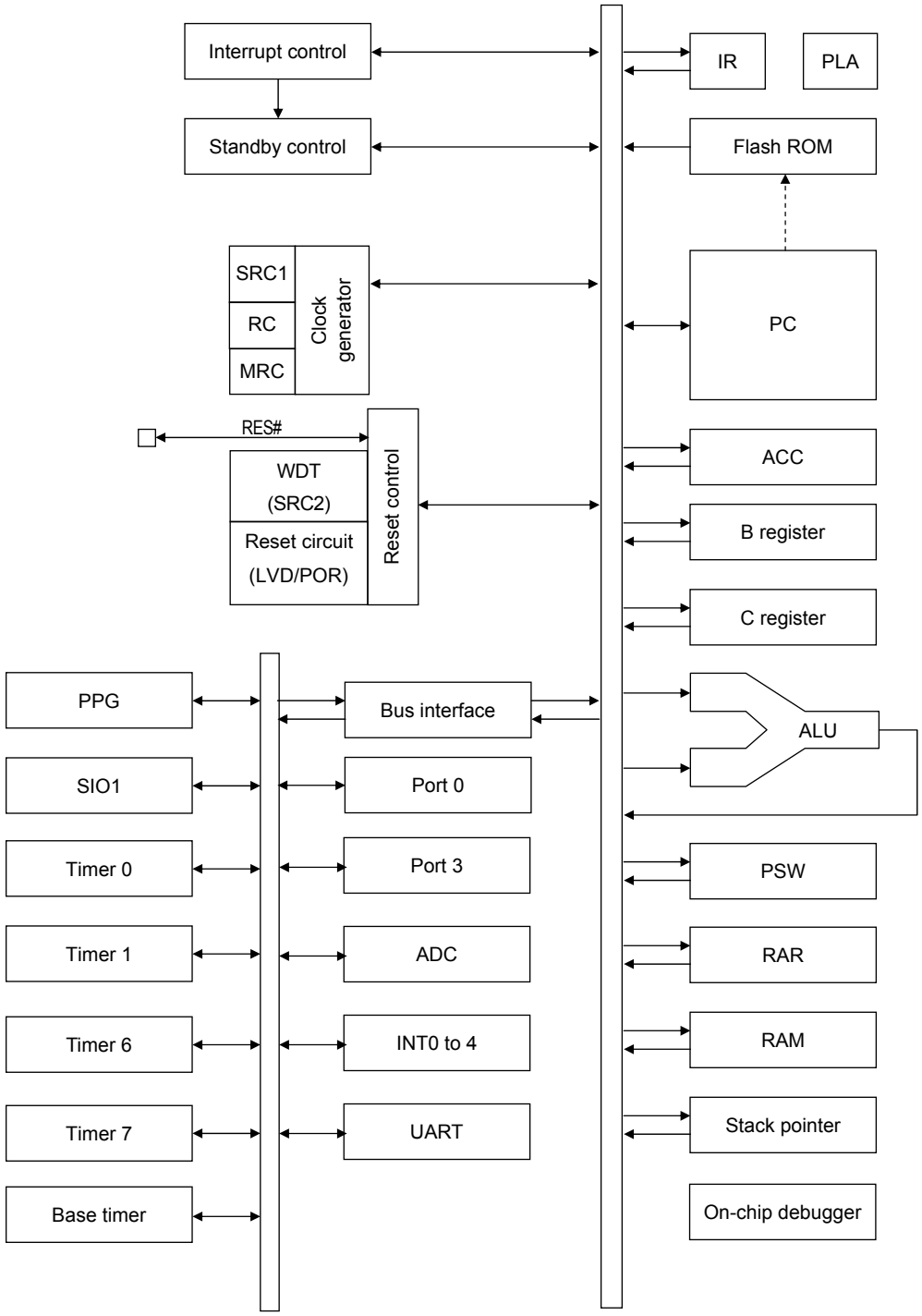


DIP24S “Lead-free Type”

DIP24S	NAME
1	P30/BUZ/CMP1O
2	PPGO
3	RES#
4	VSS1
5	VDD1
6	AMP1I
7	CMP1IA
8	CMP1IB
9	CMP2I
10	P00/AN0
11	P01/AN1
12	P02/AN2

DIP24S	NAME
13	CMP4I
14	CMP45I
15	CMP5I
16	CMP6I
17	VSS2
18	AMP2O
19	P03/AN3
20	P04/AN4/INT4
21	P05/SI1/SB1/UTX/CLKO
22	P06/SCK1/URX/T6O
23	P07/T7O
24	OWP0

System Block Diagram



Pin Function Chart

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>VSS1, VSS2</td><td>–</td><td>– power supply pins</td><td>No</td></tr>
<tr><td>VDD1</td><td>–</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>Port 0</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units. (No pull-up resistor on P07)
• Pin functions
P04 : INT4 input / HOLD release input / Timer 1 event input / Timer 0L capture input / Timer 0H capture input
P05 : SIO1 data I-O / UART transmit / System clock output
P06 : SIO1 clock I-O / UART receive / Timer 6 toggle output
P07 : Timer 7 toggle output
P00 (AN0) to P04 (AN4) : AD convertor input ports
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>P00 to P06 : Yes
P07 : No</td></tr>
<tr><td>Port 3
P30</td><td>I/O</td><td>• 1-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P30 : BUZ output / CMP1O output</td><td>Yes</td></tr>
<tr><td>AMP1I</td><td>I</td><td>AMP1 input</td><td>No</td></tr>
<tr><td>AMP2O</td><td>O</td><td>AMP2 output</td><td>No</td></tr>
<tr><td>CMP1IA</td><td>I</td><td>CMP1 input(–)</td><td>No</td></tr>
<tr><td>CMP1IB</td><td>I</td><td>CMP1 input(+) , CMP7 input (+)</td><td>No</td></tr>
<tr><td>CMP2I</td><td>I</td><td>CMP2 input(+)</td><td>No</td></tr>
<tr><td>CMP4I</td><td>I</td><td>CMP4 input(+), CMP8 input (+)</td><td>No</td></tr>
<tr><td>CMP45I</td><td>I</td><td>CMP4 input (–), CMP5 input (+)</td><td>No</td></tr>
<tr><td>CMP5I</td><td>I</td><td>CMP5 input (–)</td><td>No</td></tr>
<tr><td>CMP6I</td><td>I</td><td>CMP6 input (+)</td><td>No</td></tr>
<tr><td>PPGO</td><td>I/O</td><td>PPG I/O port</td><td>Yes</td></tr>
<tr><td>RES#</td><td>I/O</td><td>External reset Input / internal reset output</td><td>No</td></tr>
<tr><td>OWP0</td><td>I/O</td><td>Debugger-dedicated pin</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P06	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P07	–	No	N-channel open drain	No
P30	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PPGO	–	1	CMOS	No
		2	N-channel open drain	No

User Option Table

Option name	Option to be applied on	Flash-ROM version	Option selected in units of	Option selection
Port output type	P00 to P06	○	1 bit	CMOS
				N-channel open drain
	P30	○	1 bit	CMOS
				N-channel open drain
	PPGO	○	-	CMOS
				N-channel open drain
PPGO output polarity	PPGO	○	-	Not inverted
				Inverted
AMP1 gain	-	○	-	6 x
				8 x
				10 x
CMP3Vref		○		1 / 6VDD
				2 / 6VDD
				3 / 6VDD
				4 / 6VDD
CMP7Vref		○		1 / 20VDD
				2 / 20VDD
CMP8Vref		○		12 / 20VDD
				13 / 20VDD
				14 / 20VDD
				Disabled
PPG Pulse End	PPG-Pulse-End upper limit	○		080h
				100h
				180h
				200h
				280h
				300h
				380h
				3FFh
Program start address	-	○	-	00000h
				01E00h
Low-voltage detection reset function	Detection function	○	-	Enabled: Use
				Disabled: Disuse
	Detection level	○	-	7-level
Power-on reset function	Power-on reset level	○	-	8-level

Recommended Unused Pin Connections

Pin Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P30	Open	Output low

On-chip Debugger pin connection requirements

The on-chip debugger pin (OWPO) must be pulled down (with 100 KΩ) on the user's board.
It is also recommended that a connector be installed to cable with the debugger tool (TCB87 Type C).
The connector must have three connections, i.e., GND, OWPO, and V_{DD}.

Note : Be sure to electrically short-circuit between the VSS1 and VSS2 pins.

1. Absolute Maximum Ratings at Ta=25°C, $V_{SS}1$= $V_{SS}2$= 0V

Parameter		Symbol	Pin / Remarks	Conditions	VDD[V]	Specification min.	typ.	max.	unit
Maximum supply voltage		VDDMAX	VDD1			−0.3	-	+6.5	V
Input voltage		VI	RES#, AMP1I, CMP1IA,CMP1IB, CMP2I, CMP4I CMP45I, CMP5I CMP6I			−0.3	-	VDD+0.3	
Output voltage		VO	AMP2O			−0.3	-	VDD+0.3	
Input/output voltage		VIO	P00 to P07, P30, OWP0, PPGO			−0.3	-	VDD+0.3	
High level output current	Peak output current	IOPH	P00 to P06, P30, PPGO, OWP0	CMOS output select Per 1 applicable pin		−10			mA
	Mean output current (Note 1-1)	IOMH	P00 to P06, P30, PPGO, OWP0	CMOS output select Per 1 applicable pin		−7.5			
	Total output current	ΣIOAH	P00 to P06, P30, PPGO, OWP0	Total of all applicable pins		−25			
Low level output current	Peak output current	IOPL(1)	P02 to P07, P30, PPGO, OWP0	Per 1 applicable pin				20	
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
	Mean output current (Note 1-1)	IOML(1)	P02 to P07, P30, PPGO, OWP0	Per 1 applicable pin				15	
		IOML(2)	P00, P01	Per 1 applicable pin				20	
	Total output current	ΣIOAL(1)	P00 to P03	Total of all applicable pins				40	
		ΣIOAL(2)	P04 to P07, P30, PPGO, OWP0	Total of all applicable pins				40	
		ΣIOAL(3)	P00 to P07, P30, PPGO, OWP0	Total of all applicable pins				70	
Allowable power dissipation		Pdmax(1)	DIP24S	Ta=−40 to +85°C Package only				300	mW
		Pdmax(2)		Ta=−40 to +85°C Mounted on thermal resistance test board (Note 1-2)				470	
Operating ambient temperature		Topr				−40	-	+85	°C
Storage ambient temperature		Tstg				−55	-	+125	

Note 1-1 : The mean output current is a mean value measured over 100ms.

Note 1-2 : SEMI standards thermal resistance board (size : 76.1×114.3×1.6t mm, glass epoxy) is used.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Allowable Operating Conditions at Ta=–40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin / Remarks	Conditions		Specification			
				VDD[V]	min.	typ.	max.	unit
Operating supply voltage	VDD	VDD1	0.238µs ≤ tCYC ≤ 200µs		4.5		5.5	V
Memory sustaining supply voltage	VHD	VDD1	RAM and register contents sustained in HOLD mode.		2.0			
High level input voltage	VIH(1)	P30, OWP0, PPGO		4.5 to 5.5	0.3VDD +0.7		VDD	
	VIH(2)	P00 to P07		4.5 to 5.5	0.3VDD +0.7		VDD	
	VIH(3)	RES#		4.5 to 5.5	0.75VDD		VDD	
Low level input voltage	VIL(1)	P30, OWP0, PPGO		4.5 to 5.5	VSS		0.1VDD +0.4	
	VIL(2)	P00 to P07		4.5 to 5.5	VSS		0.15VDD +0.4	
	VIL(3)	RES#		4.5 to 5.5	VSS		0.25VDD	
Instruction cycle time (Note 2-1)	tCYC (Note 2-1)			4.5 to 5.5	0.238		120	µs
Oscillation frequency range	FmMRC		Multi-frequency RC oscillation. 1/2 frequency division ratio. (RCCTD=0) (Note 2-2)	4.5 to 5.5	11.4	12.0	12.6	MHz
	FmRC		Internal medium-speed RC oscillation	4.5 to 5.5	0.5	1.0	2.0	
	FmSRC1		Internal low-speed RC1 oscillation	4.5 to 5.5	50	100	200	kHz
	FmSRC2		Internal low-speed RC2 oscillation	4.5 to 5.5	15	30	60	

Note 2-1 : Relationship between tCYC and oscillation frequency is 3/FmMRC at a division ratio of 1/1 and 6/FmMRC at a division ratio of 1/2.

Note 2-2 : When switching the system clock, allow an oscillation stabilization time of 100 µs or longer after the multi-frequency RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

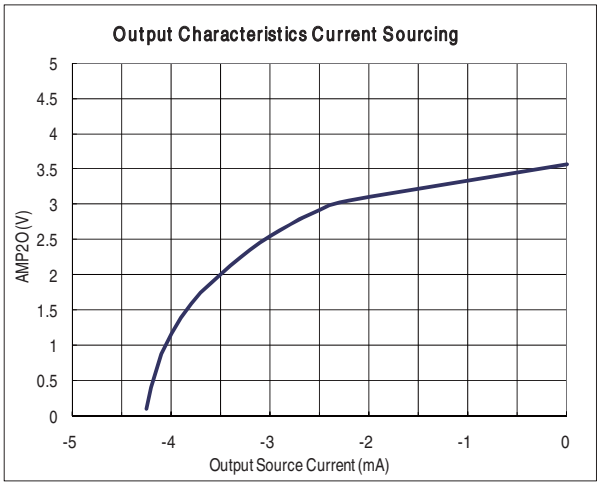
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

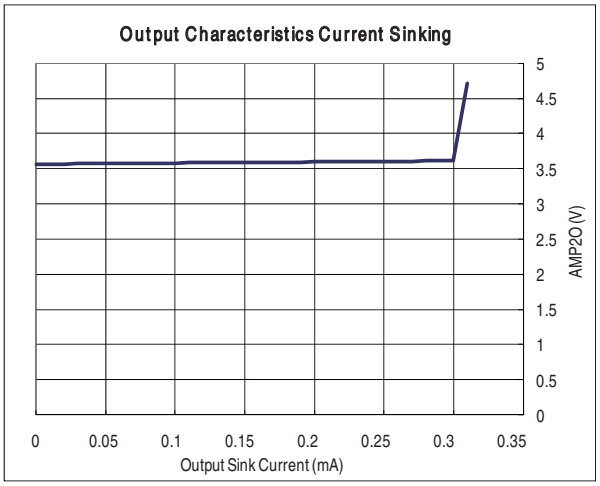
3. Electrical Characteristics at Ta=–40 to +85°C, $V_{SS}1$= $V_{SS}2$=0V

Parameter	Symbol	Pin / Remarks	Conditions	Specification				
				VDD[V]	min.	typ.	max.	unit
High level input current	IIH	P00 to P07, P30, CMP1IA, CMP1IB, CMP2I, CMP4I, CPM45I, CMP5I, CMP6I, AMP1I, OWP0, RES#	Output disabled Pull-up resistor off VIN=VDD (Including output Tr's off leakage current)	4.5 to 5.5			1	μA
Low level input current	IIL	P00 to P07, P30, CMP1IA, CMP1IB, CMP2I, CMP4I, CPM45I, CMP5I, CMP6I, AMP1I, OWP0, RES#	Output disabled Pull-up resistor off VIN=VSS (Including output Tr's off leakage current)	4.5 to 5.5	–1			
AMP allowable output current (Note 3-1)	IAMPO	AMP2O	AMP1 gain is 8 x and AMP2 gain is 1 x selected AMP1I=0.445V	5.0	–2.0		0.30	mA
High level output voltage	VOH(1)	P00 to P06	IOH=-1mA	4.5 to 5.5	VDD–1			V
	VOH(2)	P30, PPGO, OWP0	IOH=-6mA	4.5 to 5.5	VDD–1			
Low level output voltage	VOL(1)	P00 to P07, P30, PPGO, OWP0	IOL=10mA	4.5 to 5.5			1.5	
	VOL(2)		IOL=1.4mA	4.5 to 5.5			0.4	
	VOL(3)	P00, P01	IOL=25mA	4.5 to 5.5			1.5	
	VOL(4)		IOL=4mA	4.5 to 5.5			0.4	
Pull-up resistance	Rpu	P00 to P06, P30	VOH=0.9VDD	4.5 to 5.5	15	35	80	kΩ
Hysteresis voltage	VHYS	P04 to P07, P30, RES#, OWP0, PPGO	P04 only when detecting INT4 interrupt	4.5 to 5.5		0.1VDD		V
Pin capacitance	CP	All pins	For pins other than that under test: VIN=VSS f=1MHz Ta=25°C	4.5 to 5.5		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Note 3-1 :





4. Serial I/O Characteristics at Ta=–40 to +85°C, $V_{SS}1$= $V_{SS}2$=0V

(Note 4-1)

Parameter			Symbol	Pin / Remarks	Conditions	Specification				
						VDD[V]	min.	typ.	max.	unit
Serial clock	Input clock	Period	tSCK(3)	SCK1 (P06)	• See Fig. 5.	4.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Period	tSCK(4)	SCK1 (P06)	• CMOS output selected • See Fig. 5.	4.5 to 5.5	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1 (P05)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 2.	4.5 to 5.5	0.05			µs
	Data hold time		thDI(2)				0.05			
Serial output	Output delay time		tdD0(4)	SB1 (P05)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 2.	4.5 to 5.5			(1/3)tCYC +0.08	

Note 4-1 : These specifications are theoretical values. Be sure to add a margin depending on its use.

5. Pulse Input Conditions at Ta=–40 to +85°C, $V_{SS}1$= $V_{SS}2$=0V

Parameter	Symbol	Pin / Remarks	Conditions	Specification				
				VDD[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT4 (P04)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	4.5 to 5.5	1			tCYC
	tPIL(2)	RES#	• Resetting is enabled.	4.5 to 5.5	200			µs

6. AD Converter Characteristics at $V_{SS}1= V_{SS}2=0V$

< 12 bits AD Converter Mode / Ta=–40 to +85°C >

Parameter	Symbol	Pin / Remarks	Conditions		Specification			
				VDD[V]	min.	typ.	max.	unit
Resolution	N	AN0 (P00) to AN4 (P04)		4.5 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	4.5 to 5.5			±16	LSB
Conversion time	TCAD		• See conversion time calculation formulas. (Note 6-2)	4.5 to 5.5	32		115	µs
Analog input voltage range	VAIN			4.5 to 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 5.5			1	µA
	IAINL		VAIN=VSS	4.5 to 5.5	–1			

< 8 bits AD Converter Mode / Ta=–40 to +85°C >

Parameter	Symbol	Pin / Remarks	Conditions		Specification			
				VDD[V]	min.	typ.	max.	unit
Resolution	N	AN0 (P00) to AN4 (P04)		4.5 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	4.5 to 5.5			±1.5	LSB
Conversion time	TCAD		• See conversion time calculation formulas. (Note 6-2)	4.5 to 5.5	20		90	µs
Analog input voltage range	VAIN			4.5 to 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 5.5			1	µA
	IAINL		VAIN=VSS	4.5 to 5.5	–1			

Conversion time calculation formulas :

12bits AD Converter Mode: TCAD (Conversion time) = ((52 / (AD division ratio)) + 2) × (1/3) × tCYC

8bits AD Converter Mode: TCAD (Conversion time) = ((32 / (AD division ratio)) + 2) × (1/3) × tCYC

<Recommended Operating Conditions>

Internal oscillation (FmMRC)	Operating supply voltage range (VDD)	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD)	
					12-bit AD	8-bit AD
12MHz	4.5V to 5.5V	1/1	250ns	1/8	34.8µs	21.5µs

Note 6-1 : The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no change in I/O status occurs at the pins adjacent to the analog input channel.

Note 6-2 : The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.
The conversion time is 2 times the normal-time conversion time when :

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

7. Power-on Reset (POR) Characteristics at Ta=–40 to +85°C, $V_{SS}1$= $V_{SS}2$=0V

Parameter	Symbol	Pin / Remarks	Conditions	Option selected voltage	Specification min.	typ.	max.	unit
POR release voltage	PORRL		• Select from options. (Note 7-1)	1.67V	1.55	1.67	1.79	V
				1.97V	1.85	1.97	2.09	
				2.07V	1.95	2.07	2.19	
				2.37V	2.25	2.37	2.49	
				2.57V	2.45	2.57	2.69	
				2.87V	2.75	2.87	2.99	
				3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	
Detection voltage unknown state	POUKS		• See Fig. 4. (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS		• Power supply rise time from VDD=0V to 1.6V.				100	ms

Note7-1 : The POR release level can be selected out of 8 levels when the LVD reset function is disabled.

Note7-2 : POR is in an unknown state before transistors start operation.

8. Low Voltage Detection Reset (LVD) Characteristics at Ta=–40 to +85°C, $V_{SS}1$= $V_{SS}2$=0V

Parameter	Symbol	Pin / Remarks	Conditions	Option selected voltage	Specification min.	typ.	max.	unit
LVD reset voltage (Note 8-2)	LVDET		Select from options. See Fig. 5. (Note 8-1) (Note 8-3)	1.91V	1.81	1.91	2.01	V
				2.01V	1.91	2.01	2.11	
				2.31V	2.21	2.31	2.41	
				2.51V	2.41	2.51	2.61	
				2.81V	2.71	2.81	2.91	
				3.79V	3.69	3.79	3.89	
				4.28V	4.18	4.28	4.38	
LVD detection voltage hysteresis	LVHYS			1.91V		55		mV
				2.01V		55		
				2.31V		55		
				2.51V		55		
				2.81V		60		
				3.79V		65		
				4.28V		65		
Detection voltage unknown state	LVUKS		See Fig. 5. (Note 8-4)			0.7	0.95	V
Low voltage detection minimum width (Reply sensitivity)	TLVDW		LVDET-0.5V See Fig. 6.		0.2			ms

Note8-1 : The LVD reset level can be selected out of 7 levels when the LVD reset function is enabled.

Note8-2 : LVD reset voltage specification values do not include hysteresis voltage.

Note8-3 : LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4 : LVD is in an unknown state before transistors start operation.

9. Amplifier and Comparator Characteristics at Ta=–40 to +85°C, $V_{SS}1= V_{SS}2=0V$

Parameter	Symbol	Pin / Remarks	Conditions	VDD[V]	Specification min.	typ.	max.	unit
Common mode input voltage range (Note 9-1)	VCMIN	CMP1IA, CMP1IB, CMP2I,CMP4I CMP45I, CMP5I, CMP6I		4.5 to 5.5	VSS		VDD –1.5V	V
Internal reference voltage	VREF(1)	CMP2,		4.5 to 5.5	2/3VDD –0.02		2/3VDD +0.02	
	VREF(2)	CMP3, CMP6		4.5 to 5.5	1/6VDD –0.02		4/6VDD +0.02	
	VREF(3)	CMP7		4.5 to 5.5	1/20VDD –0.02		2/20VDD +0.02	
	VREF(4)	CMP8		4.5 to 5.5	12/20VDD –0.02		14/20VDD +0.02	
AMP input voltage range (Note 9-2)	VAMIN	AMP1I		4.5 to 5.5	VSS		(VDD –1.5V) /AMP gain	
Offset voltage	VOFF(1)	CMP1IA, CMP1IB, (CMP1) CMP4I, CMP45I, (CMP4) CMP45I, CMP5I, (CMP5)	• Within common mode input voltage range	4.5 to 5.5			±20	mV
	VOFF(2)	CMP2I (CMP2), CMP6I (CMP6), CMP1IB (CMP7), CMP4I,(CMP8)	• Within common mode input voltage range • Including VREF error	4.5 to 5.5			±40	
	VOFF(3)	AMP1I (CMP3)	• Within AMP Input voltage range • AMP1 gain set at 8x • Including VREF error	4.5 to 5.5			±28	
AMP output error	VAER	AMP2O	• Within AMP Input voltage range • AMP1 gain set at 8x • AMP2 gain set at 1x	4.5 to 5.5		±155	±200	mV
CMP1 response time (Note 9-3)	tC1RT	CMP1O(P30)	• Within common mode input voltage range • Input amplitude=100mV • Over drive=50mV	4.5 to 5.5		200		ns
CMP3 response time	tC3RT	PPGO	• AMP1 gain set at 8x • AMP1I rising time • MP1I=(VREF±100mV)/8 • See Fig. 7.	4.5 to 5.5		600		
CMP4 /CMP5 response time	tC45RT	PPGO	• Within common mode input voltage range • Input amplitude=100mV • Over drive=50mV	4.5 to 5.5		200		
CMP6 /CMP8 response time	tC68RT	PPGO	• CMP input pin rising time CMP input=VREF±50mV • See Fig. 7.	4.5 to 5.5		200		
CMP7 response time	tC7RT	PPGO	• CMP input pin falling time • CMP input=VREF±50mV • See Fig. 8.	4.5 to 5.5		200		

Note 9-1 : When V_{DD}=5V, the comparator input voltage is effective from 0 to 3.5V.

Note 9-2 : AMP gain = AMP1 gain × AMP2 gain
When V_{DD} =5V, AMP1 gain 8×, AMP2 gain 1×, the AMP input voltage is effective from 0 to 0.4375V.

Note 9-3 : PPG output has a delay of 1/6tCYC to 1/2tCYC from CMP1O falling timing for synchronization with system clock, when the pulse start delay setup register is set to 000H.

10. Consumption Current Characteristics at Ta=–40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin / Remarks	Conditions	VDD[V]	Specification			
					min.	typ.	Max.	unit
Normal mode consumption current (Note 10-1) (Note 10-2)	IDDOP(1)	VDD1	• System clock set to 12MHz of multi-frequency RC oscillator. • Internal low speed/medium speed RC oscillator stopped. • 1/1 frequency division ratio	4.5 to 5.5		8	12	mA
	IDDOP(2)		• System clock: Internal medium-speed RC oscillator • Internal low speed RC oscillator/multi-frequency RC oscillator stopped. • 1/2 frequency division ratio	4.5 to 5.5		2.5	4	
	IDDOP(3)		• System clock: Internal low-speed RC oscillator • Internal medium speed RC oscillator/multi-frequency RC oscillator stopped. • 1/1 frequency division ratio	4.5 to 5.5		2.1	3.1	
Halt mode consumption current (Note 10-1) (Note 10-2)	IDDHALT (1)		• HALT mode • System clock set to 12MHz of multi-frequency RC oscillator • Internal low speed/medium speed RC oscillator stopped. • 1/1 frequency division ratio	4.5 to 5.5		4.2	7	
	IDDHALT (2)		• HALT mode • System clock set to internal medium- speed RC oscillator • Internal low speed RC oscillator/multi-frequency RC oscillator stopped. • 1/2 frequency division ratio	4.5 to 5.5		2.3	3.5	
	IDDHALT (3)		• HALT mode • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillator/multi-frequency RC oscillator stopped. • 1/1 frequency division ratio	4.5 to 5.5		2	3	
HOLD mode consumption current (Note 10-1) (Note 10-2) (Note 10-3)	IDDHOLD		• HOLD mode. • When LVD option selected	4.5 to 5.5		2	3	

Note10-1 : Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note10-2 : The consumption current values do not include operational current of LVD function if not specified.

Note10-3 : AMP/CMP circuits are operating in HOLD mode.

11. F-ROM Programming Characteristics at Ta=+10 to +55°C, $V_{SS}1= V_{SS}2=0V$

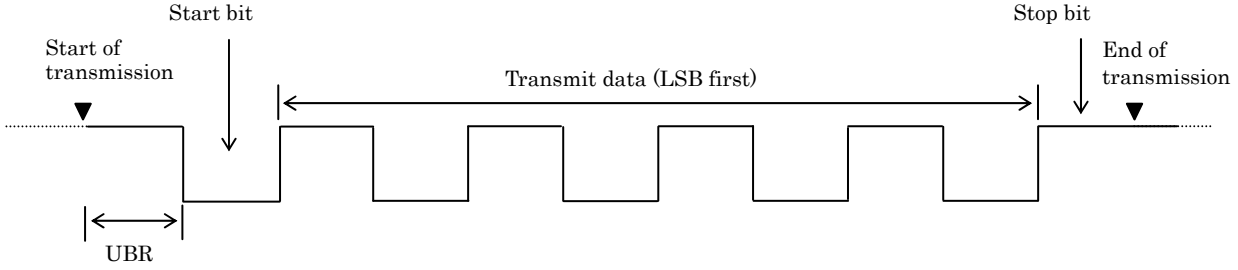
Parameter	Symbol	Pin / Remarks	Conditions	Specification				
				VDD[V]	min.	typ.	max.	unit
Onboard programming current	IDDFW	VDD1	• Excluding current consumption of the microcontroller block	4.5 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing operation	4.5 to 5.5		20	30	ms
	tFW(2)		• Programming operation			40	60	µs

12. UART (Full Duplex) Operating Conditions at Ta=–40 to +85°C, $V_{SS}1= V_{SS}2=0V$

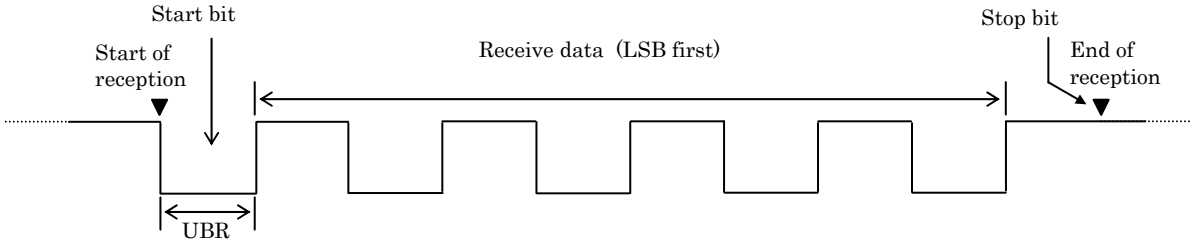
Parameter	Symbol	Pin / Remarks	Conditions	Specification				
				VDD[V]	min.	typ.	max.	unit
Transfer rate	UBR	UTX(P05) URX(P06)		4.5 to 5.5	16/3		8192/3	tCYC

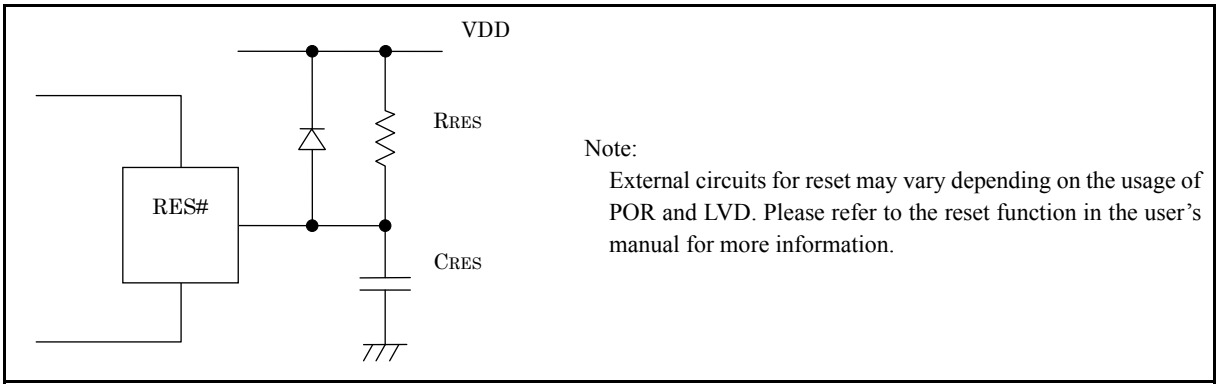
Data length : 7/8/9 bits (LSB first)
Stop bits : 1 bit(2-bit in continuous data transmission)
Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)





Note:
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the reset function in the user's manual for more information.

Figure 1. Sample Reset Circuit

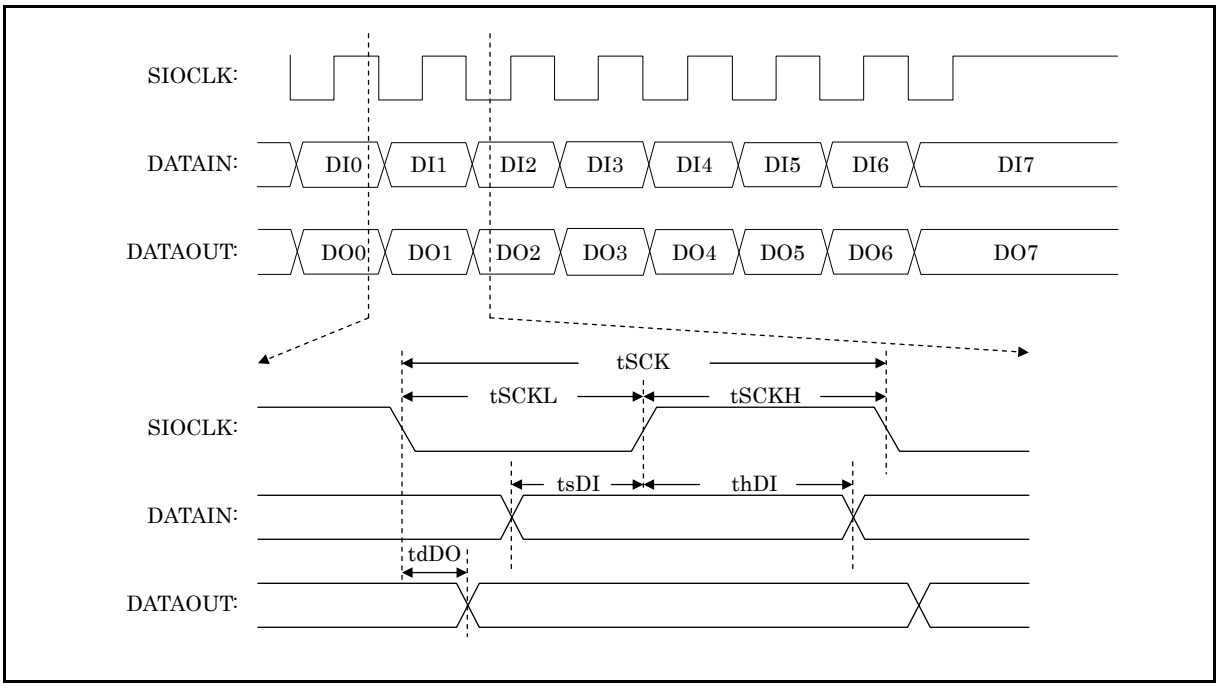


Figure 2. Serial I/O Waveforms

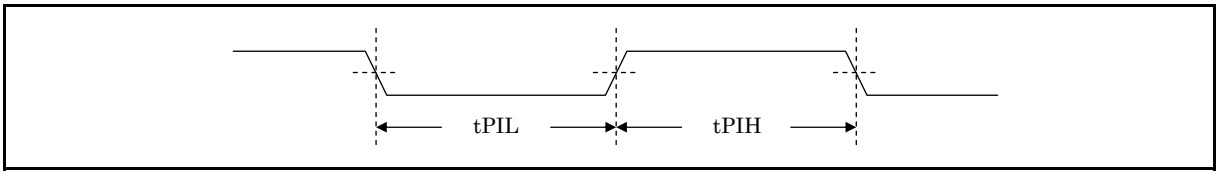


Figure 3. Pulse Input Timing Signal Waveform

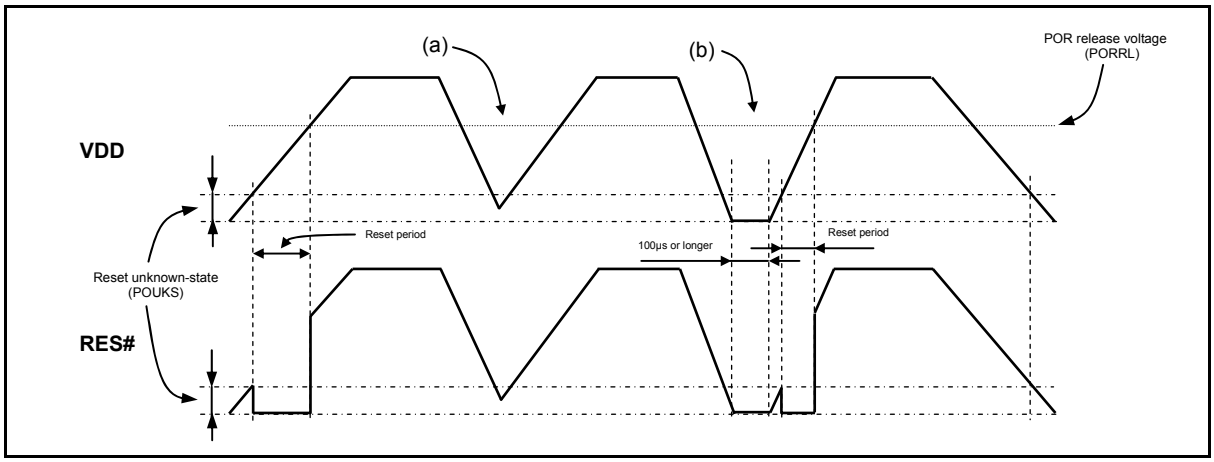


Figure 4. Example of waveforms observed when only POR is used (LVD not used)
(RESET pin : Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the VSS level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the VSS level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

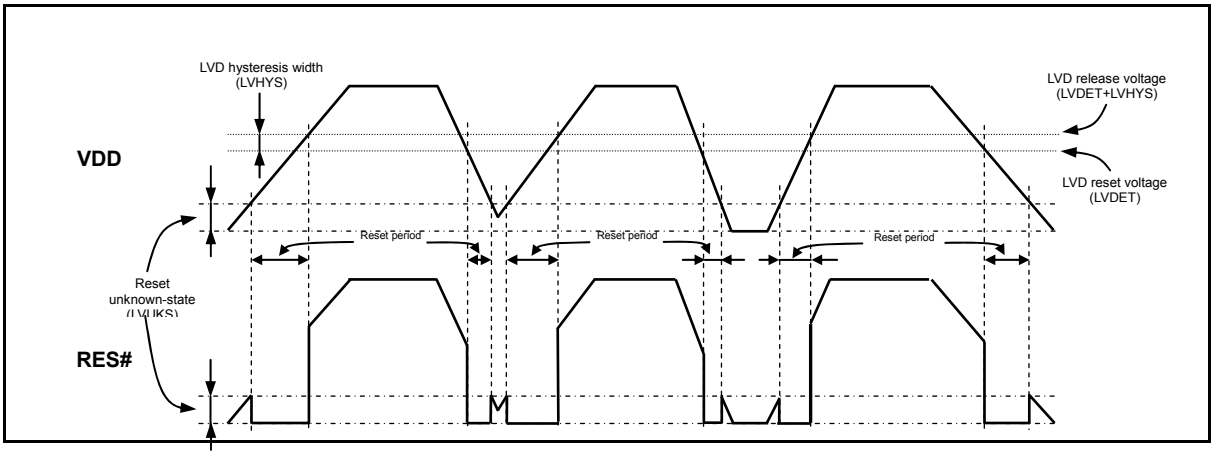


Figure 5. Example of waveforms observed when both POR and LVD functions are used
(RESET pin : Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

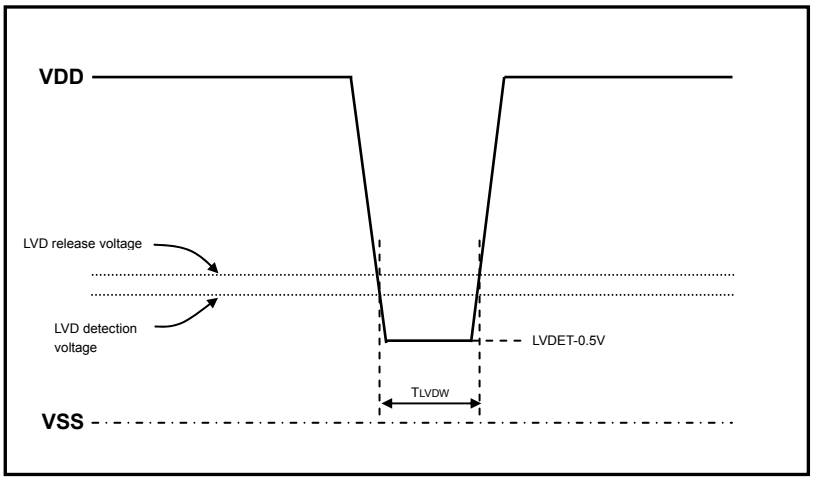


Figure 6. Low voltage detection minimum width
(Example of momentary power loss / Voltage variation waveform)

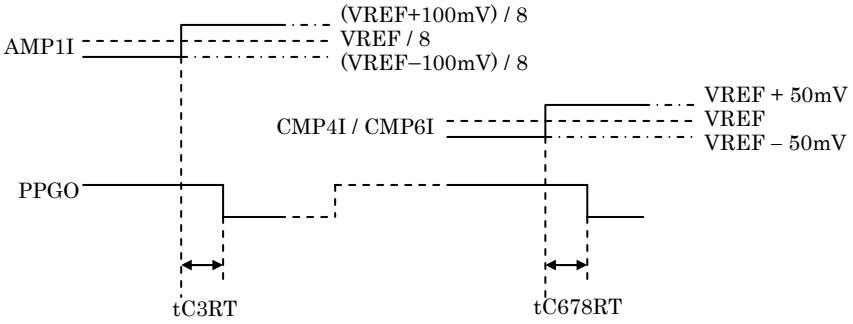


Figure 7. CMP response time 1

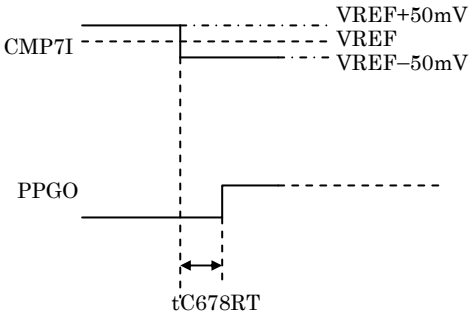


Figure 8. CMP response time 2

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F2K08AU-DIP-E	DIP24S(300mil) (Pb-Free)	1100 / Fan-Fold