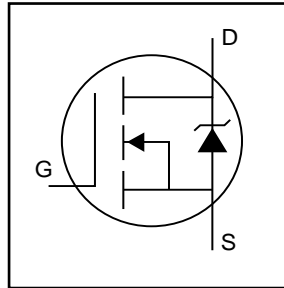


# IRFR/U3303

HEXFET<sup>®</sup> Power MOSFET

- Ultra Low On-Resistance
- Surface Mount (IRFR3303)
- Straight Lead (IRFU3033)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

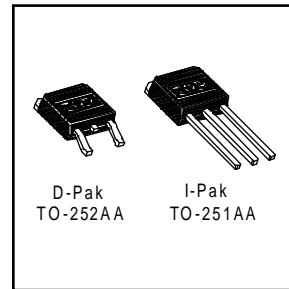


$V_{DSS} = 30V$
$R_{DS(on)} = 0.031\Omega$
$I_D = 33A^{\textcircled{5}}$

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



## Absolute Maximum Ratings

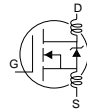
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	33 <sup>⑤</sup>	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	21 <sup>⑥</sup>	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	120	
$P_D @ T_C = 25^\circ C$	Power Dissipation	57	W
	Linear Derating Factor	0.45	W/ <sup>o</sup> C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy <sup>②</sup>	95	mJ
$I_{AR}$	Avalanche Current <sup>①</sup>	18	A
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	5.7	mJ
dv/dt	Peak Diode Recovery dv/dt <sup>③</sup>	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 150	<sup>o</sup> C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.2	<sup>o</sup> C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

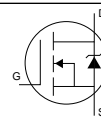
## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.032	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.031	$\Omega$	$V_{GS} = 10V, I_D = 18A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	9.3	—	—	S	$V_{DS} = 25V, I_D = 18A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	—	29	nC	$I_D = 18A$
$Q_{gs}$	Gate-to-Source Charge	—	—	7.3		$V_{DS} = 24V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	13		$V_{GS} = 10V$ , See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 15V$
$t_r$	Rise Time	—	99	—		$I_D = 18A$
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		$R_G = 13\Omega$
$t_f$	Fall Time	—	28	—		$R_D = 0.8\Omega$ , See Fig. 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑥
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	750	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	400	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	140	—		$f = 1.0\text{MHz}$ , See Fig. 5



## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	120		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	53	80	ns	$T_J = 25^\circ\text{C}, I_F = 18A$
$Q_{rr}$	Reverse Recovery Charge	—	94	140	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting  $T_J = 25^\circ\text{C}, L = 590\mu H$   
 $R_G = 25\Omega, I_{AS} = 18A$ . (See Figure 12)
- ③  $I_{SD} \leq 18A, di/dt \leq 140A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤ Calculated continuous current based on maximum allowable junction temperature; Package limitation current = 20A.
- ⑥ This is applied for I-PAK,  $L_S$  of D-PAK is measured between lead and center of die contact

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material ) .  
For recommended footprint and soldering techniques refer to application note #AN-994

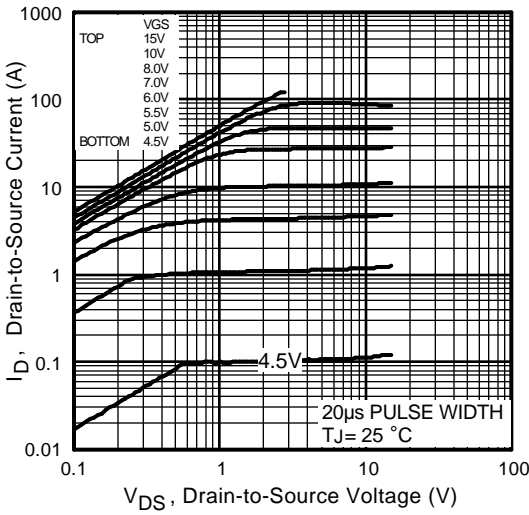


Fig 1. Typical Output Characteristics

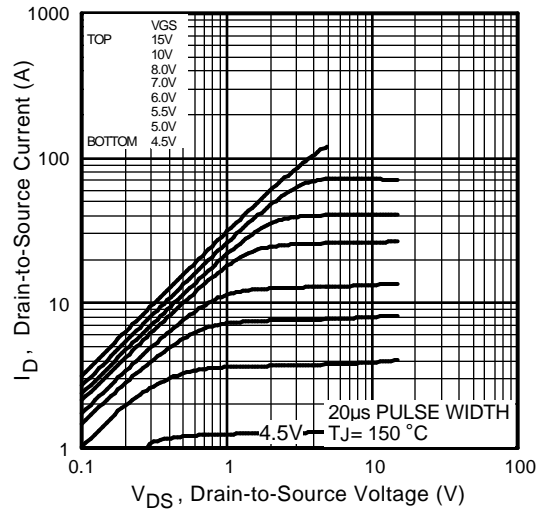


Fig 2. Typical Output Characteristics

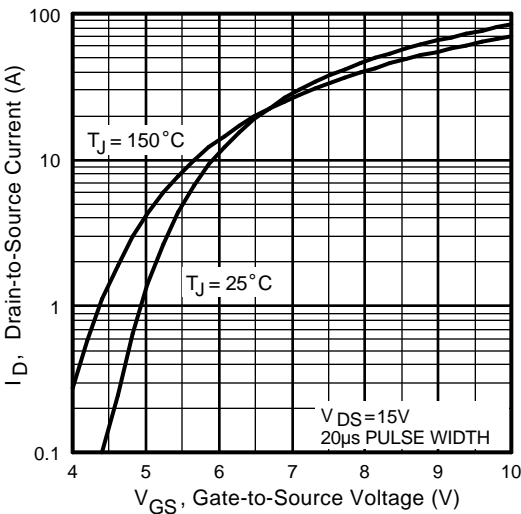


Fig 3. Typical Transfer Characteristics

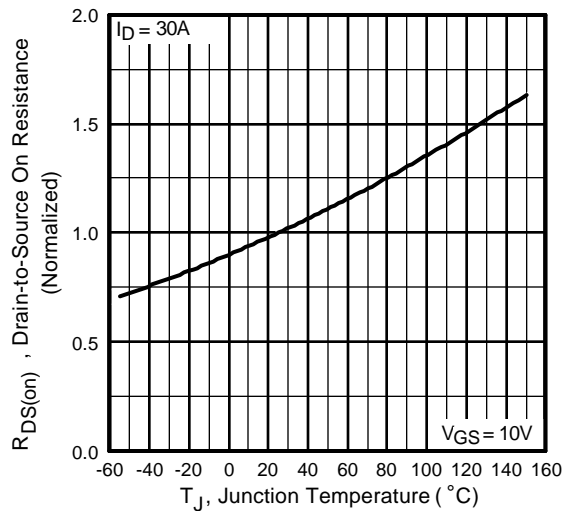
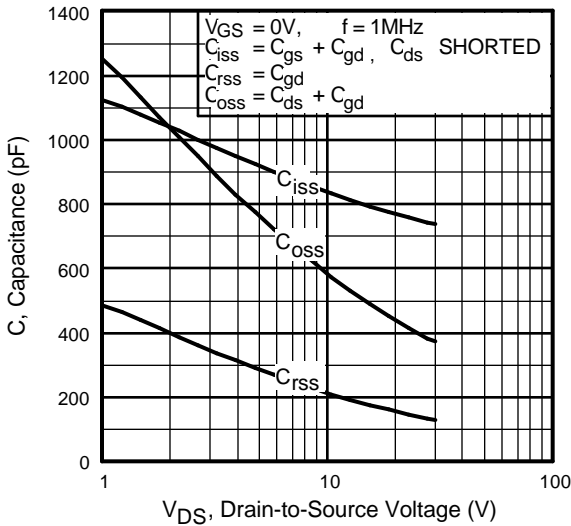
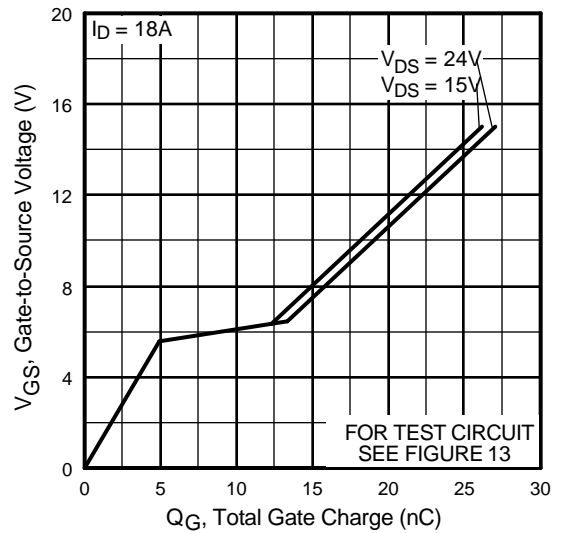


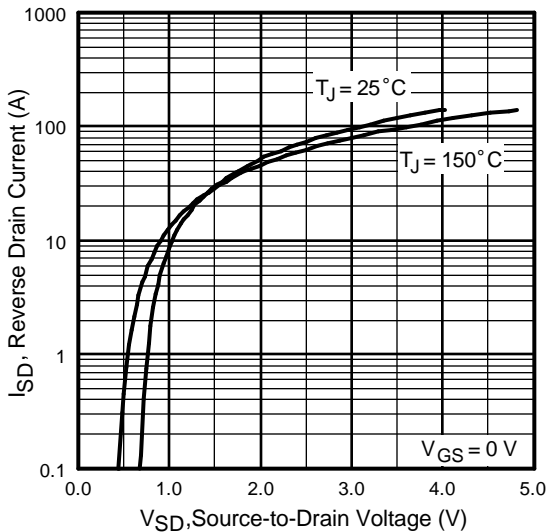
Fig 4. Normalized On-Resistance Vs. Temperature



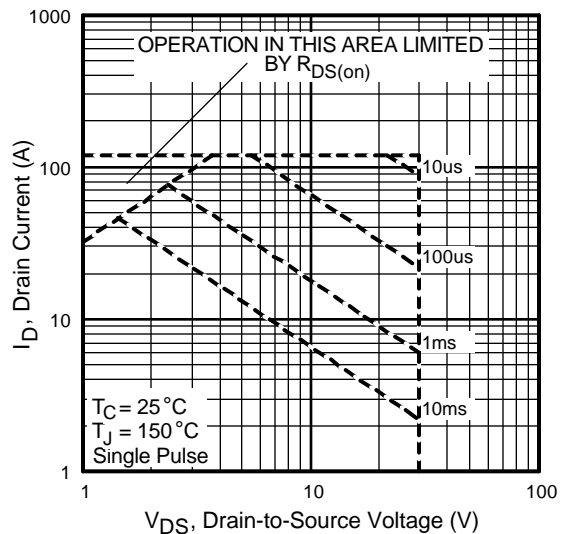
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



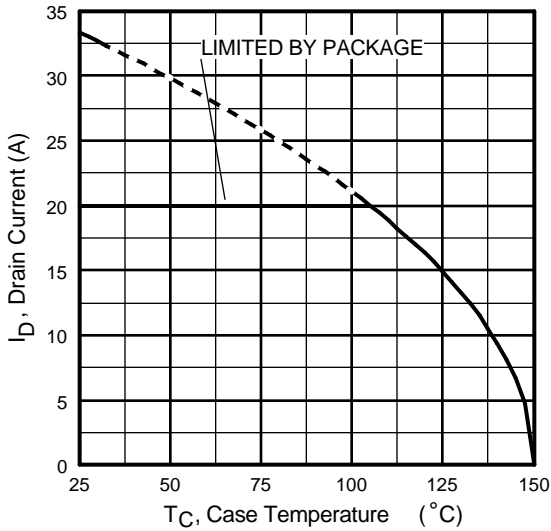
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



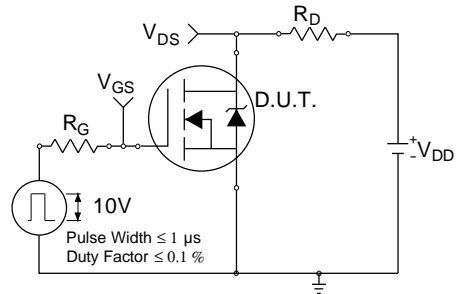
**Fig 7.** Typical Source-Drain Diode Forward Voltage



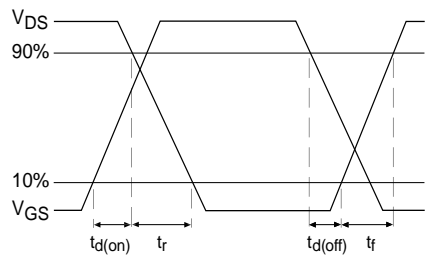
**Fig 8.** Maximum Safe Operating Area



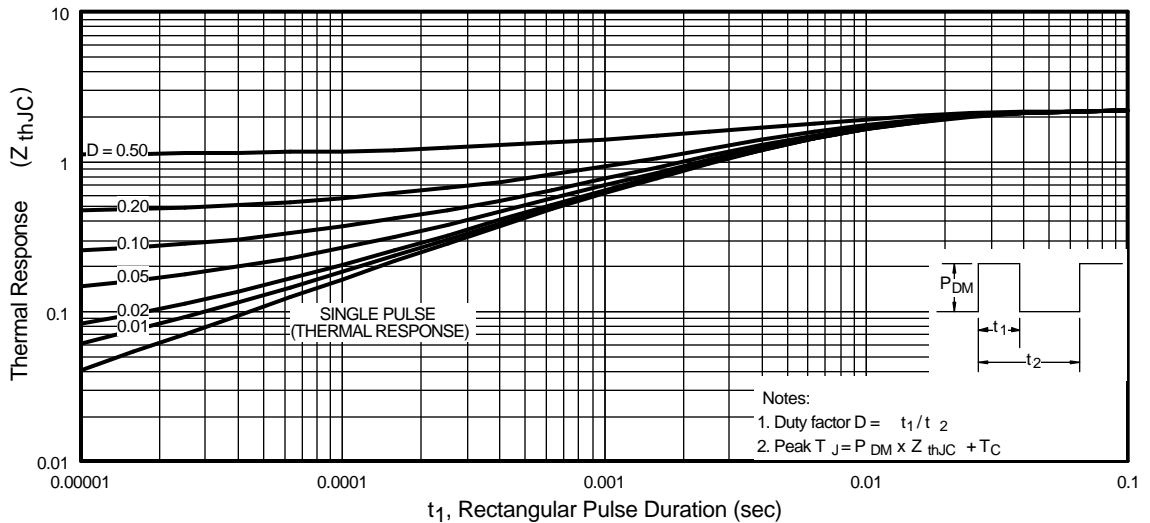
**Fig 9.** Maximum Drain Current Vs. Case Temperature



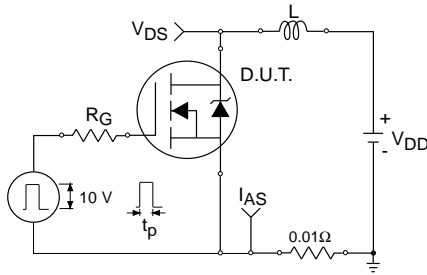
**Fig 10a.** Switching Time Test Circuit



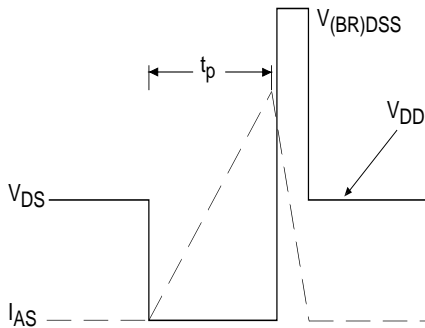
**Fig 10b.** Switching Time Waveforms



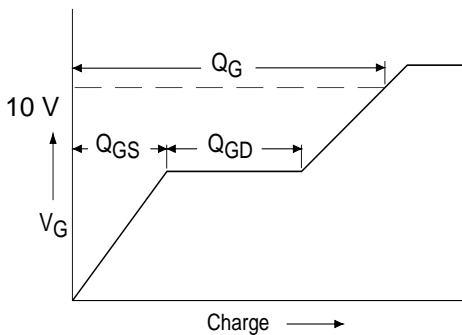
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



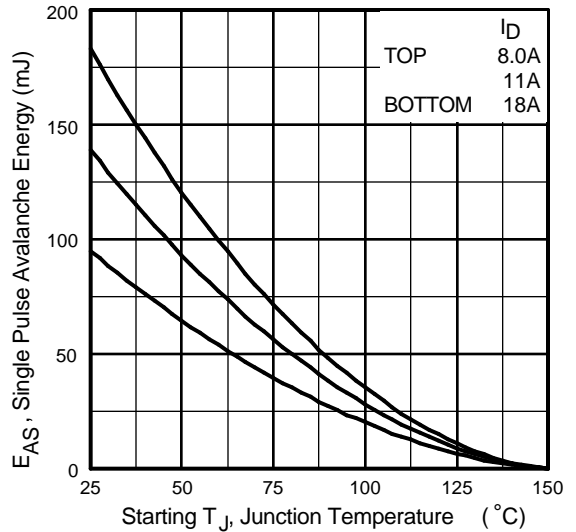
**Fig 12a.** Unclamped Inductive Test Circuit



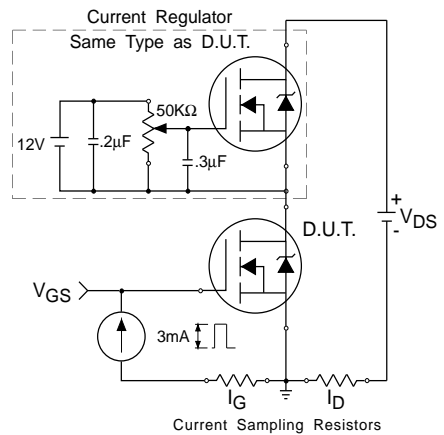
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

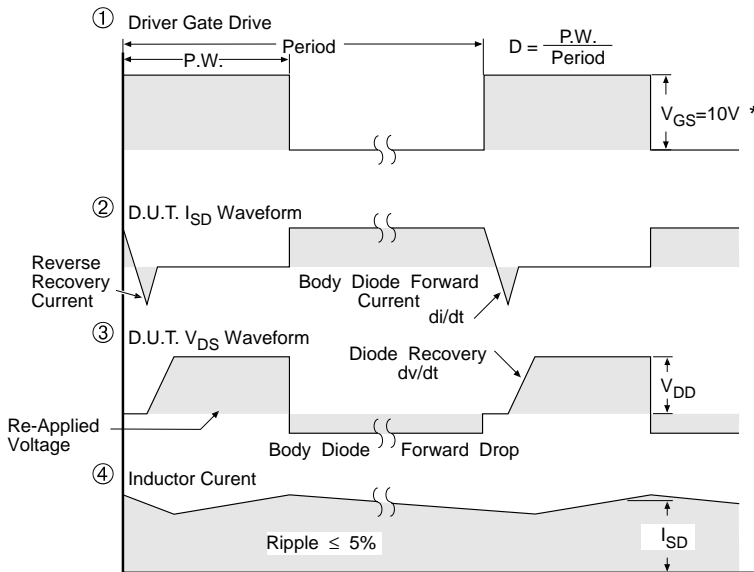
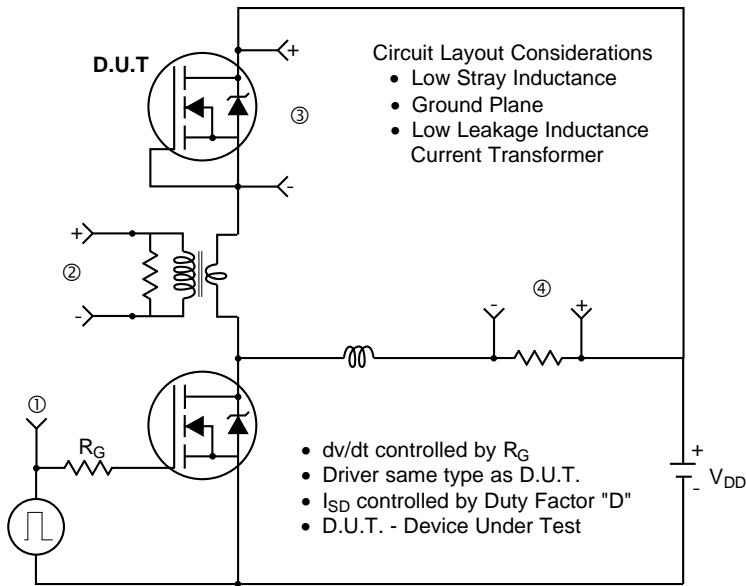


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



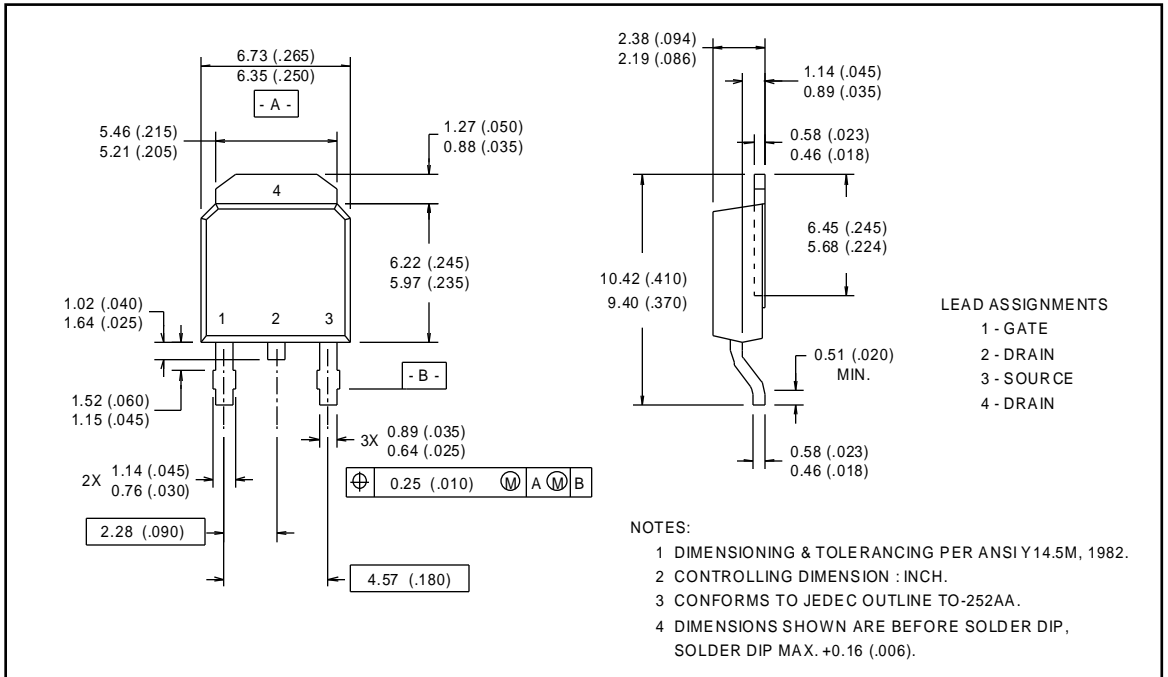
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

## Package Outline

### TO-252AA Outline

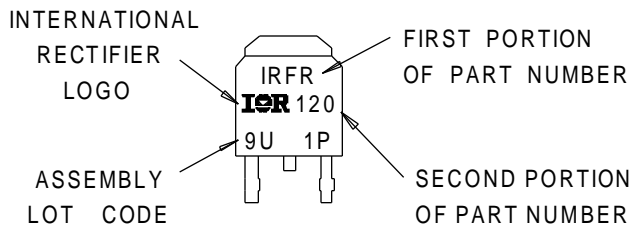
Dimensions are shown in millimeters (inches)



## Part Marking Information

### TO-252AA (D-Pak)

EXAMPLE : THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 9U1P

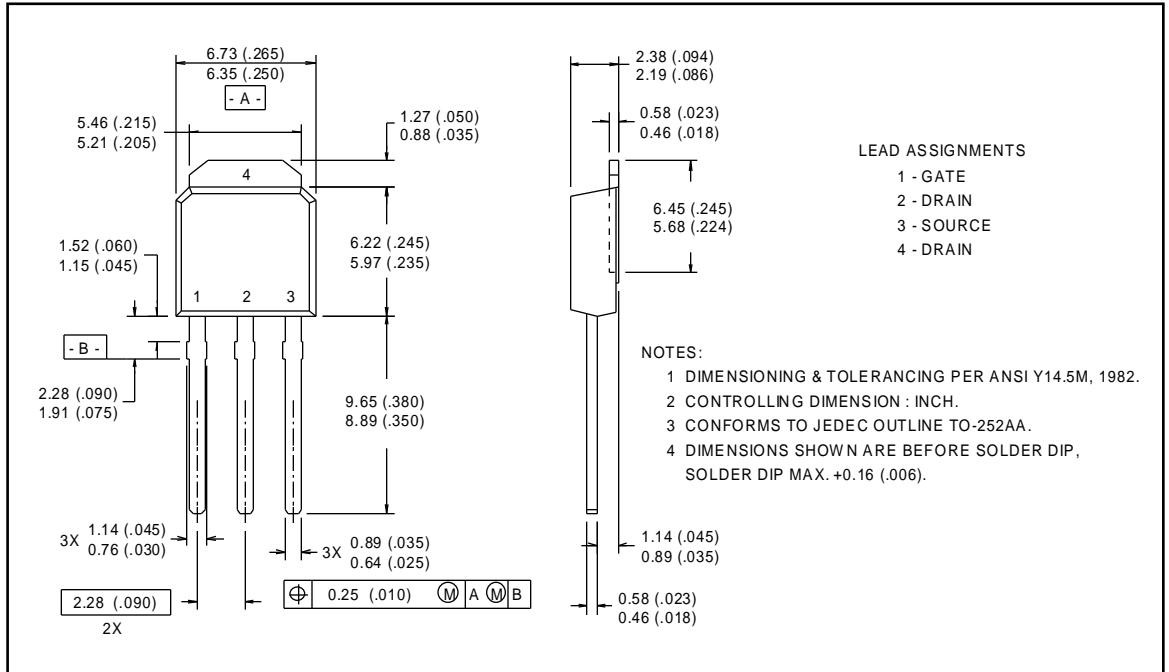




## Package Outline

### TO-251AA Outline

Dimensions are shown in millimeters (inches)



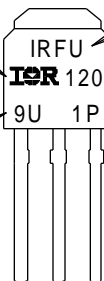
## Part Marking Information

### TO-251AA (I-Pak)

EXAMPLE : THIS IS AN IRFU120  
 WITH ASSEMBLY  
 LOT CODE 9U1P

INTERNATIONAL  
 RECTIFIER  
 LOGO

ASSEMBLY  
 LOT CODE

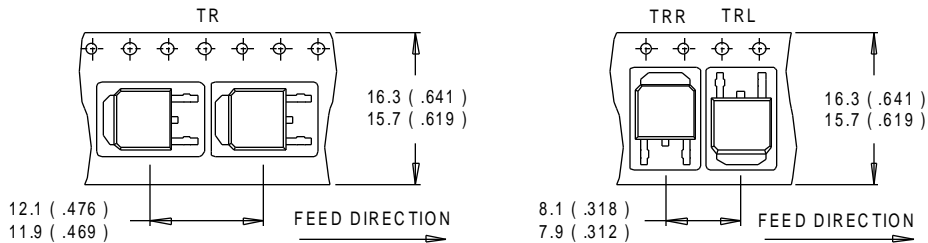


FIRST PORTION  
 OF PART NUMBER

SECOND PORTION  
 OF PART NUMBER

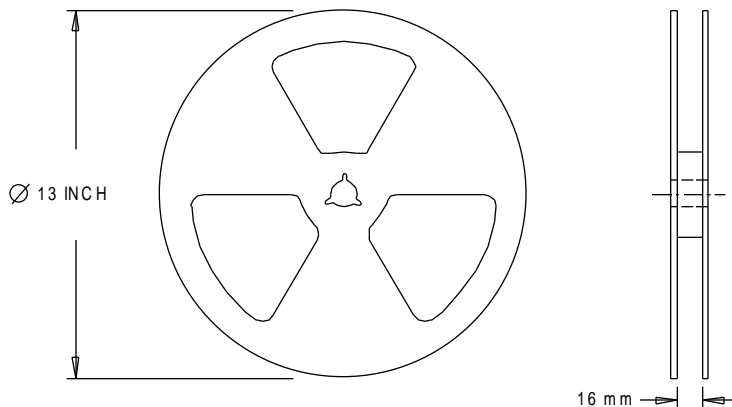
## Tape & Reel Information

TO-252AA



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>