

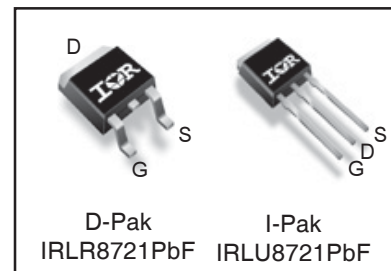
**Applications**

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- Lead-Free

**Benefits**

- Very Low RDS(on) at 4.5V V<sub>GS</sub>
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>Q<sub>g</sub></b>
<b>30V</b>	<b>8.4mΩ</b>	<b>8.5nC</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Absolute Maximum Ratings**

	<b>Parameter</b>	<b>Max.</b>	<b>Units</b>
V <sub>DS</sub>	Drain-to-Source Voltage	30	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	65 <sup>①</sup>	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	46 <sup>②</sup>	
I <sub>DM</sub>	Pulsed Drain Current <sup>①</sup>	260	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	65	W
P <sub>D</sub> @ T <sub>C</sub> = 100°C	Maximum Power Dissipation	33	
	Linear Derating Factor	0.43	W/°C
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		

**Thermal Resistance**

	<b>Parameter</b>	<b>Typ.</b>	<b>Max.</b>	<b>Units</b>
R <sub>θJC</sub>	Junction-to-Case	—	2.3	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) <sup>③</sup>	—	50	
R <sub>θJA</sub>	Junction-to-Ambient	—	110	

Notes <sup>①</sup> through <sup>③</sup> are on page 11

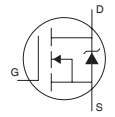
## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

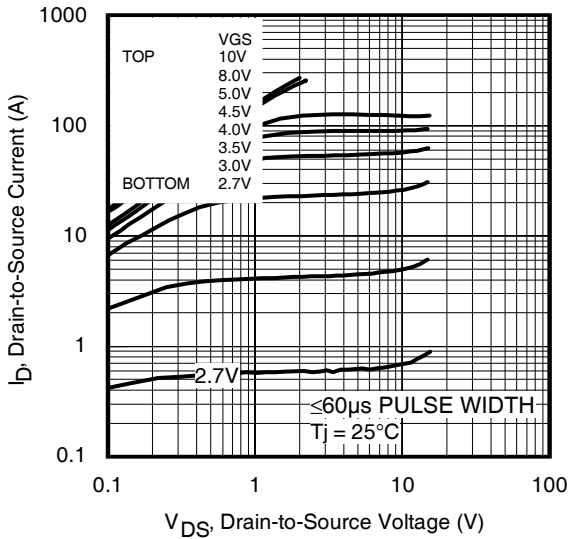
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	21	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	6.3	8.4	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A ④
		—	10.1	11.8		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 20A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.9	2.35	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 25μA
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-6.8	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	46	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 20A
Q <sub>g</sub>	Total Gate Charge	—	8.5	13	nC	V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 20A See Fig. 16
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	1.9	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	1.2	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	3.4	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	2.0	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	4.6	—		
Q <sub>oss</sub>	Output Charge	—	7.9	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	2.3	3.8	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.8	—	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V ④ I <sub>D</sub> = 20A R <sub>G</sub> = 1.8Ω See Fig. 14
t <sub>r</sub>	Rise Time	—	30	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	9.4	—		
t <sub>f</sub>	Fall Time	—	6.5	—		
C <sub>iss</sub>	Input Capacitance	—	1030	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 15V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	350	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	110	—		

## Avalanche Characteristics

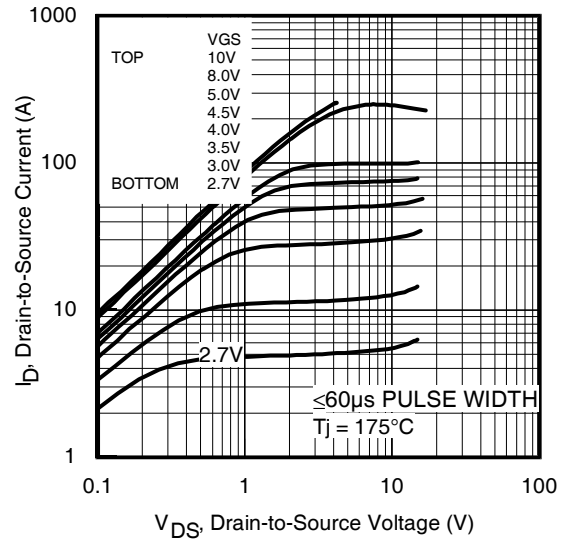
	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②⑥	—	93	mJ
I <sub>AR</sub>	Avalanche Current ①	—	20	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	—	6.5	mJ

## Diode Characteristics

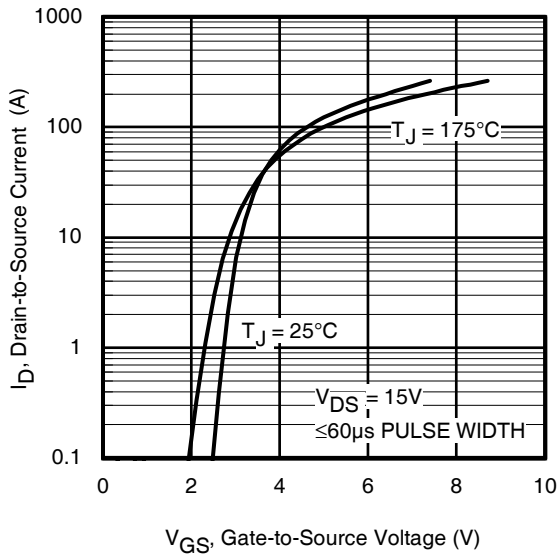
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	65④	A	 <p>MOSFET symbol showing the integral reverse p-n junction diode.</p>
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①⑥	—	—	260		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	
t <sub>rr</sub>	Reverse Recovery Time	—	17	26	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	24	36	nC	di/dt = 300A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



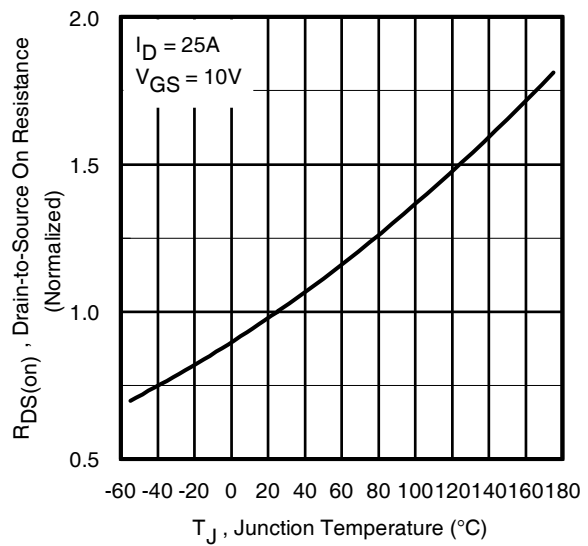
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

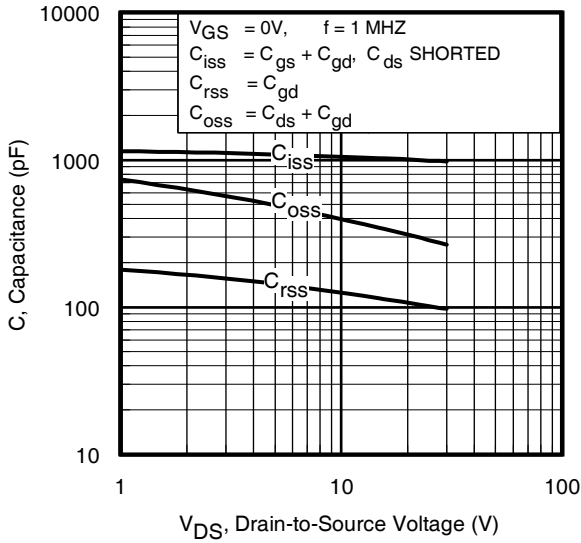


**Fig 3.** Typical Transfer Characteristics

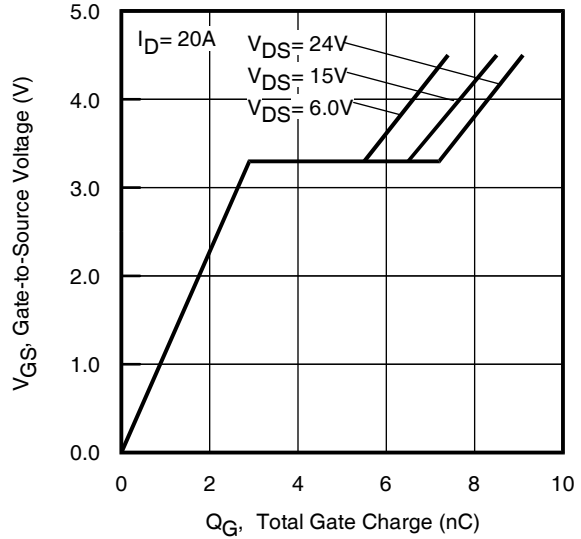


**Fig 4.** Normalized On-Resistance vs. Temperature

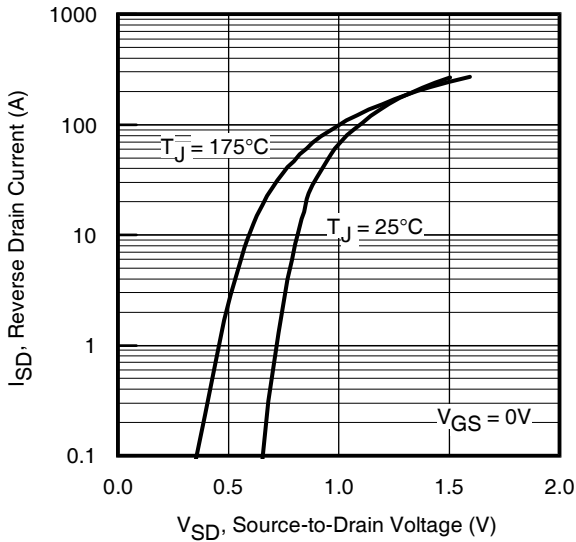
# IRLR/U8721PbF



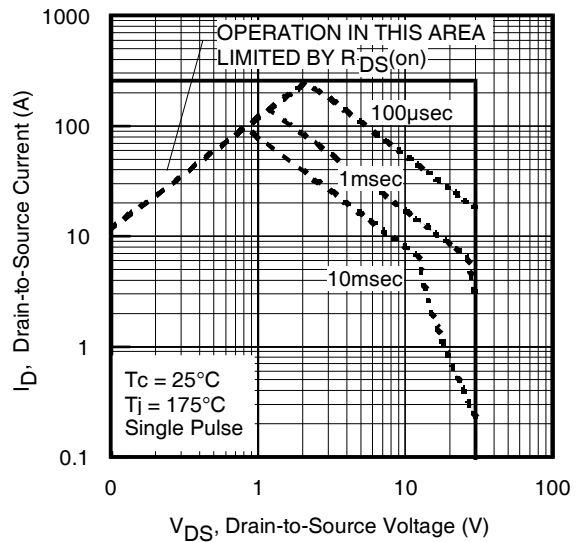
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



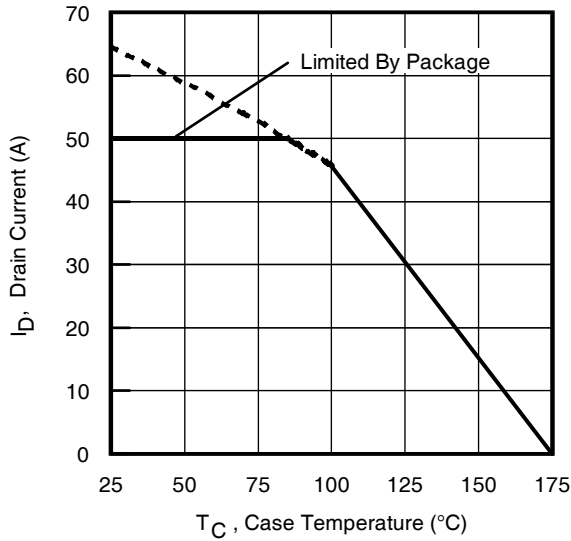
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



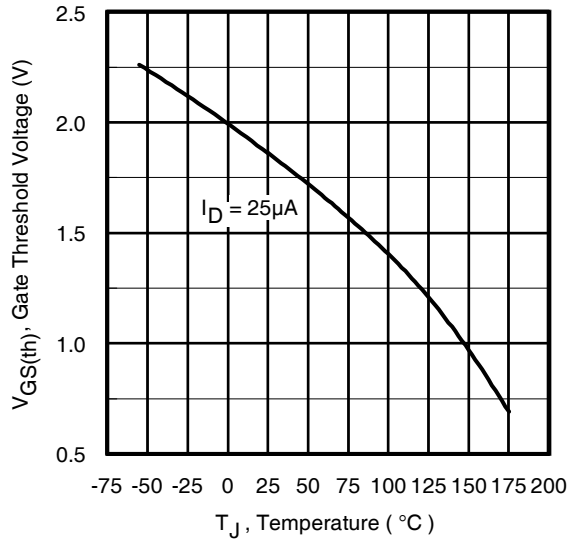
**Fig 7.** Typical Source-Drain Diode Forward Voltage



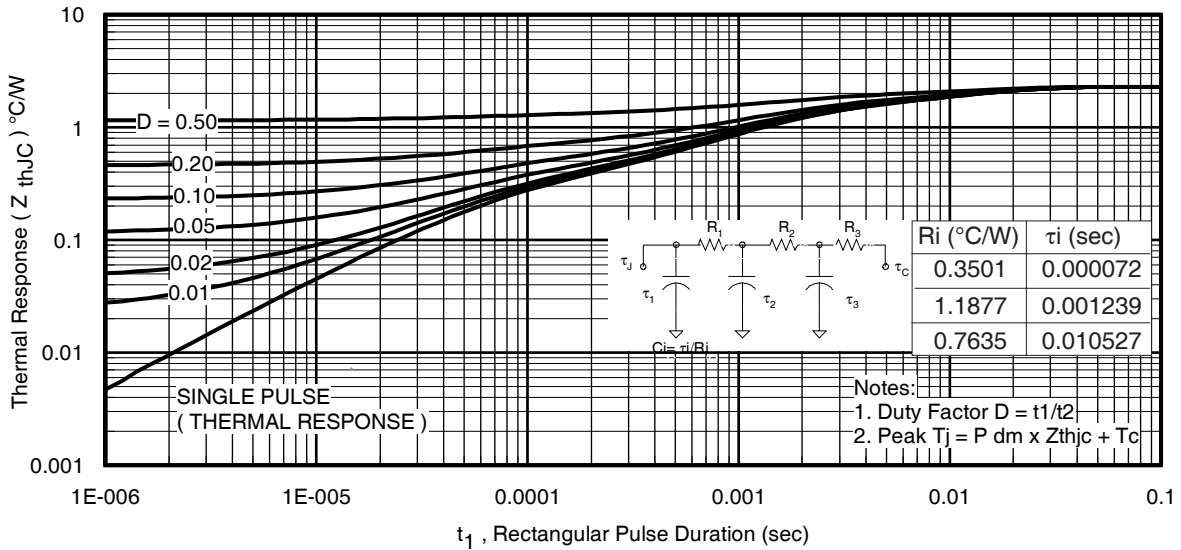
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs. Case Temperature



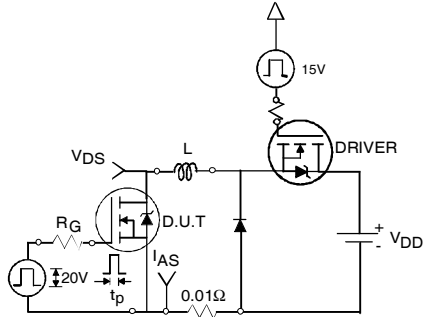
**Fig 10.** Threshold Voltage vs. Temperature



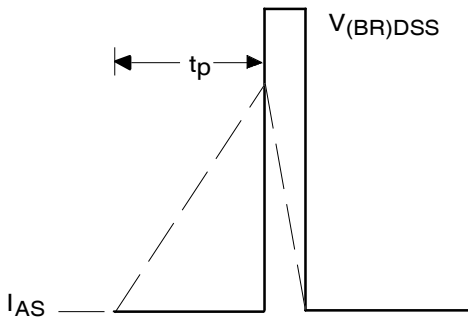
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRLR/U8721PbF

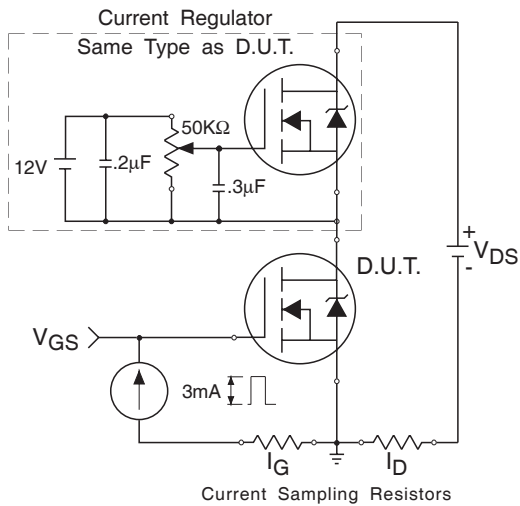
International  
**IR** Rectifier



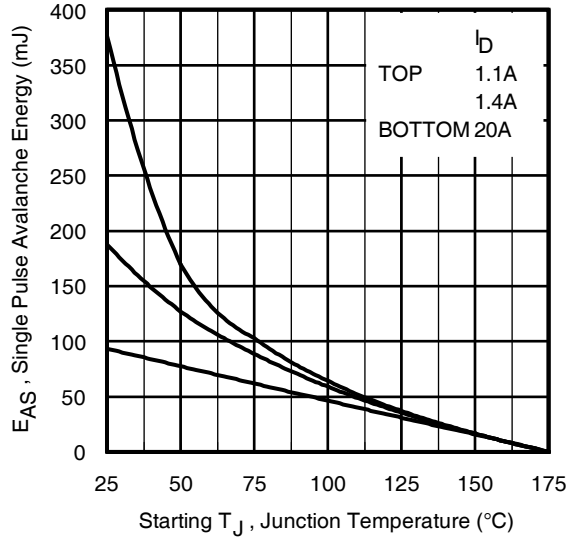
**Fig 12a.** Unclamped Inductive Test Circuit



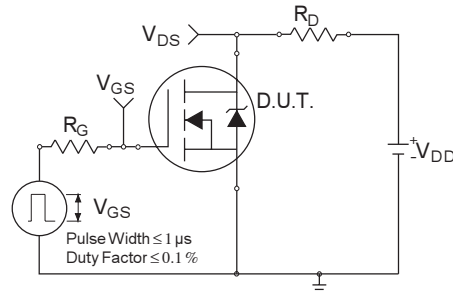
**Fig 12b.** Unclamped Inductive Waveforms



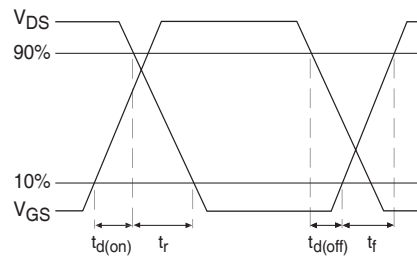
**Fig 13.** Gate Charge Test Circuit



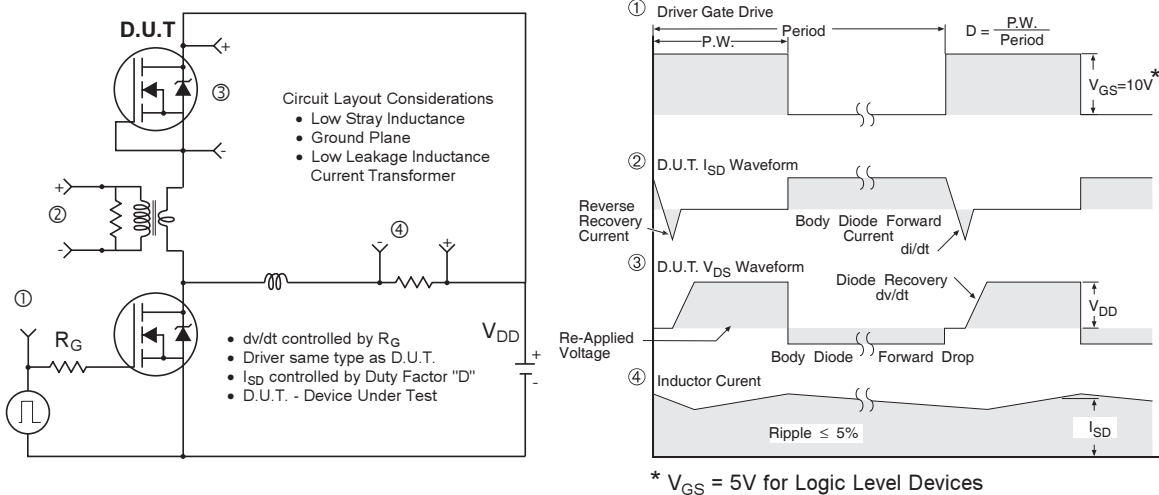
**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



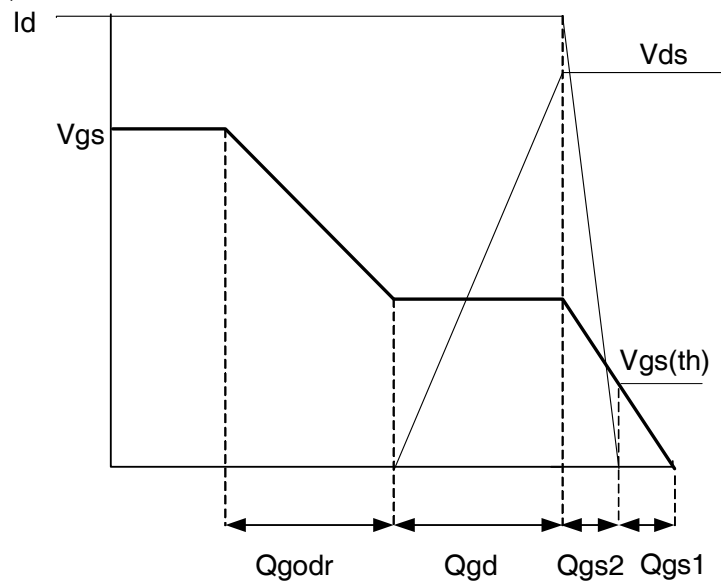
**Fig 14a.** Switching Time Test Circuit



**Fig 14b.** Switching Time Waveforms



**Fig 15. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**



**Fig 16. Gate Charge Waveform**

## Power MOSFET Selection for Non-Isolated DC/DC Converters

### Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the  $R_{ds(on)}$  of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left( I_{rms}^2 \times R_{ds(on)} \right) + \left( I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left( I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) + \left( Q_g \times V_g \times f \right) + \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms  $Q_{gs2}$  and  $Q_{oss}$  which are new to Power MOSFET data sheets.

$Q_{gs2}$  is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements,  $Q_{gs1}$  and  $Q_{gs2}$ , can be seen from Fig 16.

$Q_{gs2}$  indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to  $I_{dmax}$  at which time the drain voltage begins to change. Minimizing  $Q_{gs2}$  is a critical factor in reducing switching losses in Q1.

$Q_{oss}$  is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how  $Q_{oss}$  is formed by the parallel combination of the voltage dependant (non-linear) capacitance's  $C_{ds}$  and  $C_{dg}$  when multiplied by the power supply input buss voltage.

### Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$

$$P_{loss} = \left( I_{rms}^2 \times R_{ds(on)} \right) + \left( Q_g \times V_g \times f \right) + \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right) + \left( Q_{rr} \times V_{in} \times f \right)$$

\*dissipated primarily in Q1.

For the synchronous MOSFET Q2,  $R_{ds(on)}$  is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge  $Q_{oss}$  and reverse recovery charge  $Q_{rr}$  both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and  $V_{in}$ . As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of  $Q_{gd}/Q_{gs1}$  must be minimized to reduce the potential for Cdv/dt turn on.

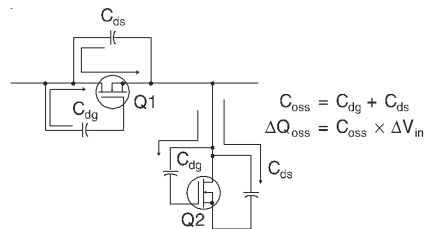
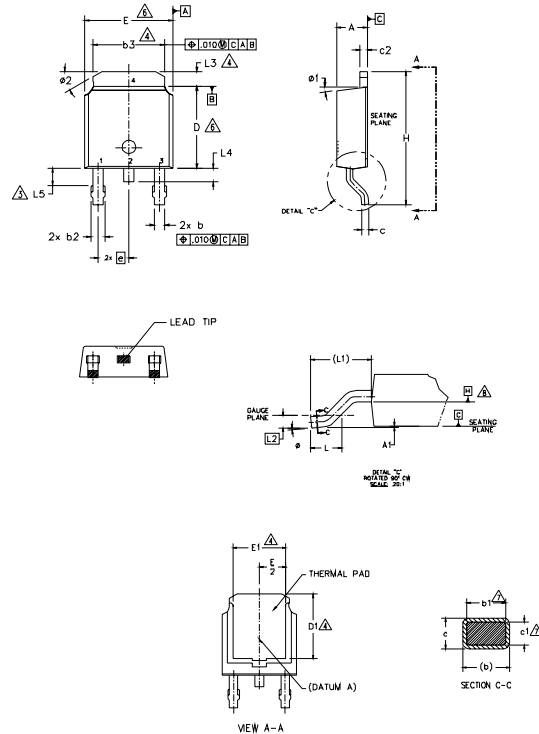


Figure A:  $Q_{oss}$  Characteristic



## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
  - 3.- LEAD DIMENSION UNCONTROLLED IN L5.
  - 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
  - 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
  - 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  - 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
Ø	0"	10"	0"	10"	
Ø1	0"	15"	0"	15"	
Ø2	25"	35"	25"	35"	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBT & CoPAK**

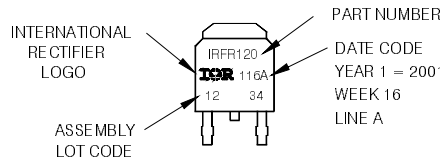
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

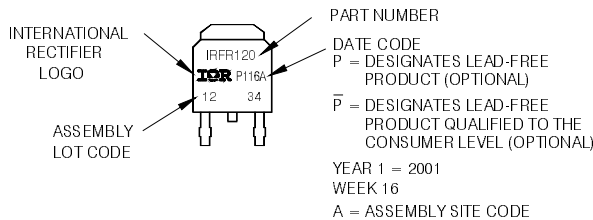
EXAMPLE: THIS IS AN IRRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position  
indicates 'Lead-Free'

'P' in assembly line position indicates  
'Lead-Free' qualification to the consumer-level



OR

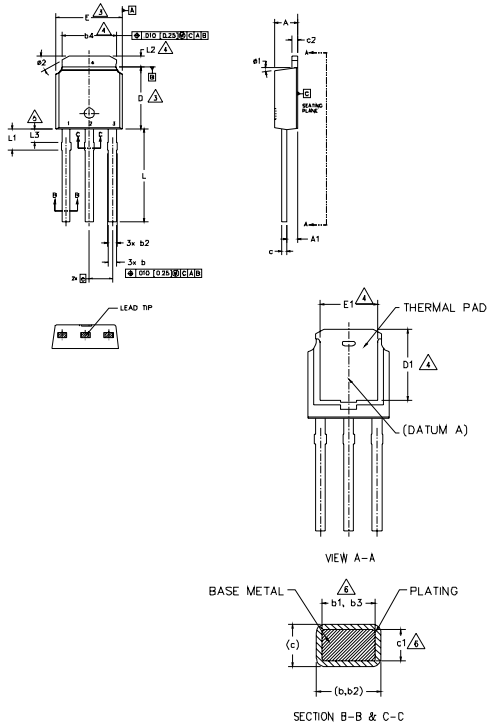


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>  
[www.irf.com](http://www.irf.com)

# IRLR/U8721PbF

## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
  - 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
  - 5.- LEAD DIMENSION UNCONTROLLED IN L3.
  - 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
  - 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
  - 8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29	BSC	.090	BSC	
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	1.14	1.52	.045	.060	5
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFET

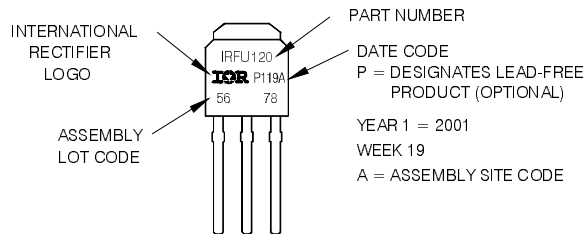
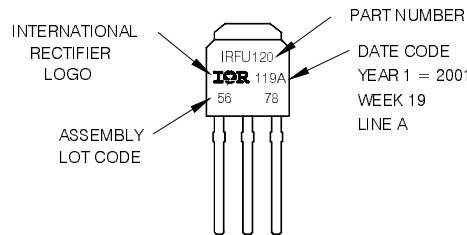
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 2001  
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position  
indicates Lead-Free

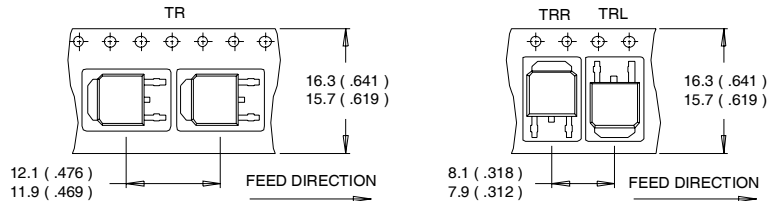
OR



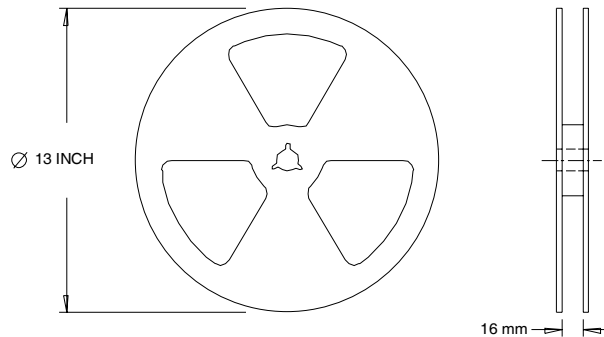
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D-Pak (TO-252AA) Tape & Reel Information**

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.47\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 20\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 50A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.