

VFXO301

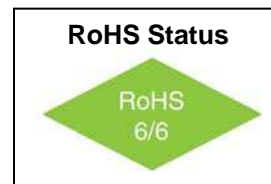
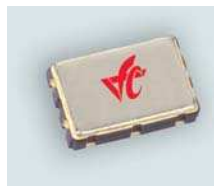
XO Low Jitter 2.5V, 3.3V

5x7mm SMD, LVPECL / LVDS



Features

- 38MHz to 700MHz Frequency Range
- Ultra Low Phase Noise
- <0.5ps jitter over 12KHz ~ 20MHz



Applications

- Optical Networking, SONET / SDH
- 10 Gigabit Ethernet
- Broadband Access

Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Frequency Range	F		38		700	MHz	
Frequency Stability	$\Delta F/F$	Vs. Operating Temperature			± 50 ± 25 ± 20	ppm	Order Code B Order Code C Order Code D
		Vs. Supply Voltage Vs. Aging / Year		± 3 ± 3 ± 1		ppm/V ppm ppm	First Year After first year
Operating Temperature	T		0° -40°		+70° +85°	°C	Order Code B Order Code G
Output		LVPECL LVDS					Order Code L Order Code D
Supply Voltage	Vcc		3.15 2.25	3.3 2.5	3.45 2.75	V	Order Code E Order Code G
Period Jitter RMS		77.76 MHz		2.5	4	ps	
		155.52 MHz		3	4		
		311.08 MHz		3	5		
		622.08 MHz		6	8		
Integrated Jitter RMS 12KHz to 20MHz		155.52MHz		0.4	0.5	ps	
		311.04MHz		0.4	0.5		
		622.08MHz		0.4	0.5		
Period Jitter Peak-to-Peak		77.76MHz		18	30	ps	
		155.52MHz		20	30		
		311.08MHz		25	30		
		622.08MHz		42	55		



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Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Symmetry		($V_{DD}-1.3$) V_{DC} 1.25 V_{DC}	45 45		55 55	%	PECL LVDS
Phase Noise		10Hz		-66		dBc/Hz	@77.76MHz
		100Hz		-96			
		1KHz		-124			
		10KHz		-136			
		100KHz		-132			
		10Hz		-62		dBc/Hz	@155.52MHz
		100Hz		-92			
		1KHz		-120			
		10KHz		-132			
		100KHz		-128			
		10Hz		-59		dBc/Hz	@311.04MHz
		100Hz		-86			
		1KHz		-116			
		10KHz		-129			
		100KHz		-124			
		10Hz		-48		dBc/Hz	@622.08MHz
		100Hz		-80			
		1KHz		-108			
		10KHz		-118			
		100KHz		-114			
Input Current	I _{CC}	38 – 100MHz			65	mA	PECL
		100 – 300MHz			80		
		300 – 700MHz			95		
		38 – 100MHz			45	mA	LVDS
		100 – 320MHz			60		
		320 – 700MHz			75		
Load	50 Ohm to $V_{DD}-2V$ (PECL) 100 Ohm (LVDS)						
Output High Voltage	V_{OH}			$V_{DD}-1.025$ 1.4	1.6	V	PECL LVDS
Output Low Voltage	V_{OL}		0.9	1.1	$V_{DD}-1.620$	V	PECL LVDS
Output Differential Voltage	V_{OD}		247	355	454	mV	LVDS
Offset Voltage	V_{OS}		1.125	1.2	1.375	V	LVDS
Rise / Fall Time	Tr/Tf	20% to 80%		0.6 0.7	1.5 1.0	ns	PECL LVDS
Tristate	"1": Output Enable – Pin 1 may float 2.8V min (3.3V V_{DD}) or 2.25V min (2.5V V_{DD}) "0": Tristate – Pin 1 requires 0.4V max (3.3V or 2.5V V_{DD})						



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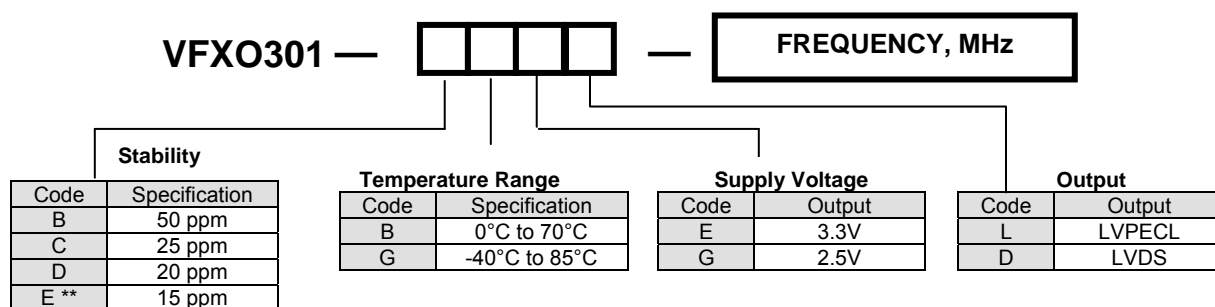
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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Lead Temperature		Soldering, 10s max			260	°C	
Storage Temperature	T _s		-55		+125°	°C	
Junction Temperature	T _j				+125°	°C	
ESD Protection		Human Body Model			2	kV	

How to Order



**not available for all frequencies.
Please consult the factory



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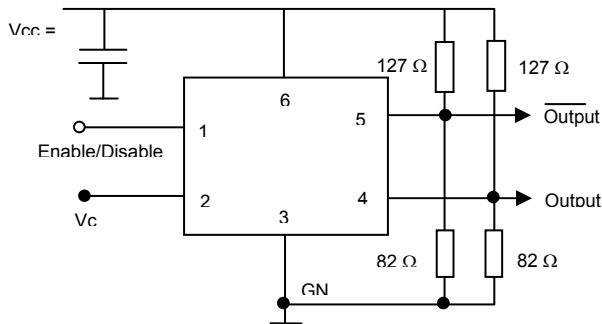
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Environmental and Mechanical Conditions

Parameter	Specification
Shock	1000 Gs, 0.35ms, ½ sine wave, 3 shocks in each plane
Humidity	Resistant to 85 °R.H. at 85 °C
Vibration	10-2000 Hz of 0.06" d.a. or 20 Gs, whichever is less
Leak	MIL STD 883, Method 1014, Condition A1
Case	Ceramic with hermetic resistance-welded metal lid
Pads	Solderable gold over nickel
Marking	Epoxy ink or laser engraved
Resistance to Solvents	MIL STD 202, Method 215



Pin #	Connection
1	Tristate
2	N/C
3	Case, GND
4	Output
5	Output
6	Supply Voltage

