

# VFXO311

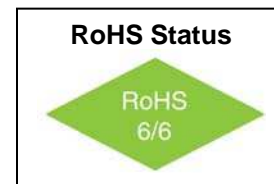
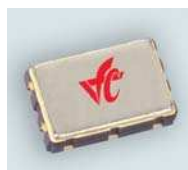
## XO Ultra Low Jitter 2.5V, 3.3V

### 5x7mm SMD, LVPECL / LVDS / LVCMOS



#### Features

- 60MHz to 800MHz Frequency Range
- Differential Output Levels (LVPECL/LVDS)
- Single Ended LVCMOS output available
- <0.2ps jitter RMS over 12KHz ~ 20MHz
- Selectable OE Logic



#### Applications

- Optical Networking, SONET / SDH
- 10 Gigabit Ethernet
- Broadband Access

#### Electrical Specifications

| Parameter                               | Symbol          | Condition                              | Min          | Typ                           | Max                              | Unit                | Note   |
|---|-----------------|--|--------------|-------------------------------|----------------------------------|---------------------|--|
| Frequency Range                         | F               |  | 60<br>60     |                               | 800<br>320                       | MHz                 | PECL / LVDS<br>CMOS                          |
| Frequency Stability                     | $\Delta F/F$    | Vs. Operating Temperature              |              |                               | $\pm 50$<br>$\pm 25$<br>$\pm 20$ | ppm                 | Order Code B<br>Order Code C<br>Order Code D |
|   |                 | Vs. Supply Voltage<br>Vs. Aging / Year |              | $\pm 3$<br>$\pm 3$<br>$\pm 1$ |                                  | ppm/V<br>ppm<br>ppm | First Year<br>After first year               |
| Operating Temperature                   | T               |  | 0°<br>-40°   |                               | +70°<br>+85°                     | °C                  | Order Code B<br>Order Code G                 |
| Output                                  |                 | LVPECL<br>LVDS<br>LVCMOS               |              |                               |                                  |                     | Order Code L<br>Order Code D<br>Order Code C |
| Supply Voltage                          | V <sub>cc</sub> |  | 3.15<br>2.25 | 3.3<br>2.5                    | 3.45<br>2.75                     | V                   | Order Code E<br>Order Code G                 |
| Period Jitter RMS                       |                 | 155.52 MHz<br>311.04 MHz<br>622.08 MHz |              | 2.5<br>2.5<br>4               | 3<br>3<br>6                      | ps                  |  |
| Integrated Jitter RMS<br>12KHz to 20MHz |                 | 155.52MHz<br>311.04MHz<br>622.08MHz    |              | 0.25<br>0.18<br>0.09          |                                  | ps                  |  |
| Period Jitter Peak-to-Peak              |                 | 155.52MHz<br>311.04MHz<br>622.08MHz    |              | 18<br>18<br>25                | 20<br>20<br>30                   | ps                  |  |

\* NOTE: Certain frequencies above 500MHz (3.3V<sub>DD</sub>) and above 300MHz (2.5V<sub>DD</sub>) are not available. Consult factory for availability.



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#### Electrical Specifications

| Parameter                   | Symbol  | Condition   | Min   | Typ                           | Max                           | Unit | Note                 |
|-----------------------------|---|---|-------|-------------------------------|-------------------------------|------|----------------------|
| Supply Current              | I <sub>CC</sub>   | 38 – 100MHz   |       |                               | 65                            | mA   | PECL                 |
|                             |   | 100 – 300MHz  |       |                               | 80                            |      |                      |
|                             |   | 300 – 640MHz  |       |                               | 90                            |      |                      |
|                             |   | 38 – 100MHz   |       |                               | 45                            | mA   | LVDS                 |
|                             |   | 100 – 320MHz  |       |                               | 60                            |      |                      |
|                             |   | 320 – 640MHz  |       |                               | 70                            |      |                      |
|                             |   | At 100MHz,<br>load = 15pF   |       | 16                            | 20                            | mA   | CMOS                 |
| Load                        | 50 Ohm to V <sub>DD</sub> -2V (PECL)<br>100 Ohm (LVDS)  |   |       |                               |                               |      |                      |
| Output High Voltage         | V <sub>OH</sub>   | R <sub>L</sub> = 50 ohm to<br>(V <sub>DD</sub> -2V)<br>I <sub>OH</sub> = -8.5mA | 2.4   | V <sub>DD</sub> -1.025<br>1.4 | 1.6                           | V    | PECL<br>LVDS<br>CMOS |
| Output Low Voltage          | V <sub>OL</sub>   | I <sub>OL</sub> = -8.5mA  | 0.9   | 1.1                           | V <sub>DD</sub> -1.620<br>0.4 | V    | PECL<br>LVDS<br>CMOS |
| Output Differential Voltage | V <sub>OD</sub>   |   | 247   | 355                           | 454                           | mV   | LVDS                 |
| Output Drive Voltage        | I <sub>OSD</sub>  | V <sub>OL</sub> = 0.4V,<br>V <sub>OH</sub> = 2.4V                               |       | 8.5                           |                               | mA   | CMOS                 |
| Offset Voltage              | V <sub>OS</sub>   |   | 1.125 | 1.2                           | 1.375                         | V    | LVDS                 |
| Rise / Fall Time            | Tr/Tf   | 20% to 80%  |       | 0.25                          | 0.45                          | ns   | PECL<br>LVDS<br>CMOS |
|                             |   |   |       | 0.3                           | 0.7                           |      |                      |
|                             |   |   |       | 1.2                           | 1.6                           |      |                      |
| Duty Cycle                  |   | V <sub>DD</sub> – 1.3V<br>@ 1.25V<br>50% V <sub>DD</sub>                        | 45    | 50                            | 55                            | %    | PECL<br>LVDS<br>CMOS |
| Tristate                    | "1": Output Enable – Pin 2 may float 2.8V min (3.3V V <sub>DD</sub> ) or 2.25V min (2.5V V <sub>DD</sub> )<br>"0": Tristate – Pin 2 requires 0.4V max (3.3V or 2.5V V <sub>DD</sub> ) |   |       |                               |                               |      |                      |

#### Phase Noise Performance

| Parameter            | Output Type  | Frequency Range (MHz) | Carrier Freq. (MHz) | 10Hz | 100Hz | 1KHz | 10 KHz | 100 KHz | 1 MHz | 10 MHz |
|----------------------|--------------|-----------------------|---------------------|------|-------|------|--------|---------|-------|--------|
| Phase Noise (dBc/Hz) | PECL<br>LVDS | 300 - 800             | 622.08              | -55  | -85   | -110 | -130   | -137    | -148  | -150   |
|                      | CMOS         | 120 – 320             | 155.52              | -50  | -82   | -110 | -128   | -142    | -148  | -150   |
|                      | PECL<br>LVDS | 120 – 320             | 155.52              | -50  | -82   | -110 | -128   | -142    | -148  | -150   |
|                      | CMOS         | 60 – 160              | 155.52              | -65  | -95   | -122 | -138   | -142    | -148  | -149   |
|                      | PECL<br>LVDS | 60 – 160              | 155.52              | -65  | -95   | -122 | -138   | -142    | -148  | -149   |



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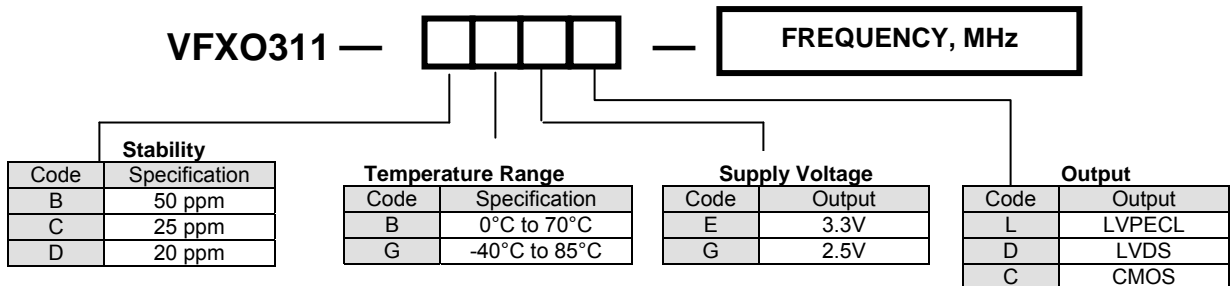
**Absolute Maximum Ratings**

| Parameter            | Symbol          | Condition                                 | Min                  | Typ | Max                  | Unit | Note |
|----------------------|-----------------|---|----------------------|-----|----------------------|------|------|
| Lead Temperature     |                 | Soldering, 10s max                        |                      |     | 260                  | °C   |      |
| Storage Temperature  | T <sub>s</sub>  |   | -55                  |     | +125°                | °C   |      |
| Junction Temperature | T <sub>j</sub>  |   |                      |     | +125°                | °C   |      |
| ESD Protection       |                 | Input static discharge voltage protection |                      |     | 2                    | kV   |      |
| Supply Voltage       | V <sub>DD</sub> |   |                      |     | 4.6                  | V    |      |
| Output Voltage       | V <sub>O</sub>  |   | V <sub>DD</sub> -0.5 |     | V <sub>DD</sub> +0.5 | V    |      |

**Environmental and Mechanical Conditions**

| Parameter              | Specification  |
|------------------------|--|
| Shock                  | 1000 Gs, 0.35ms, ½ sine wave, 3 shocks in each plane |
| Humidity               | Resistant to 85 °R.H. at 85 °C                       |
| Vibration              | 10-2000 Hz of 0.06" d.a. or 20 Gs, whichever is less |
| Leak                   | MIL STD 883, Method 1014, Condition A1               |
| Case                   | Ceramic with hermetic resistance-welded metal lid    |
| Pads                   | Solderable gold over nickel                          |
| Marking                | Epoxy ink or laser engraved                          |
| Resistance to Solvents | MIL STD 202, Method 215                              |

**How to Order**



Note: DG combination not available at all frequencies. Consult factory.



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#### LVPECL, LVDS

| Pin # | Connection     |
|-------|----------------|
| 1     | N/C            |
| 2     | Tristate       |
| 3     | Case, GND      |
| 4     | Output         |
| 5     | Output         |
| 6     | Supply Voltage |

#### LVCMOS

| Pin # | Connection     |
|-------|----------------|
| 1     | N/C            |
| 2     | Tristate       |
| 3     | Case, GND      |
| 4     | Output         |
| 5*    | N/C            |
| 6     | Supply Voltage |

\*For LVCMOS, Dual single ended outputs available – consult factory

