



SD57120

RF power transistor
the LdmoST family

Features

- Excellent thermal stability
- Common source configuration push-pull
- $P_{OUT} = 120W$ with 13dB gain @ 960MHz
- BeO free package
- Internal input matching
- In compliance with the 2002/95/EC european directive

Description

The SD57120 is a common source N-channel enhancement-mode lateral Field-Effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1.0 GHz. The SD57120 is designed for high gain and broadband performance operating in common source mode at 28V. Its internal matching makes it ideal for base station applications requiring high linearity.

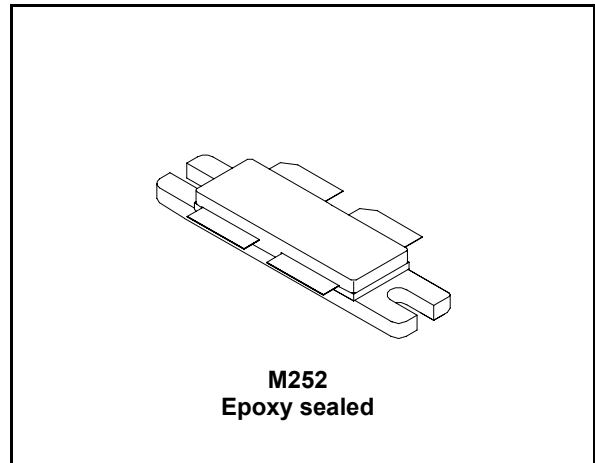


Figure 1. Pin connection

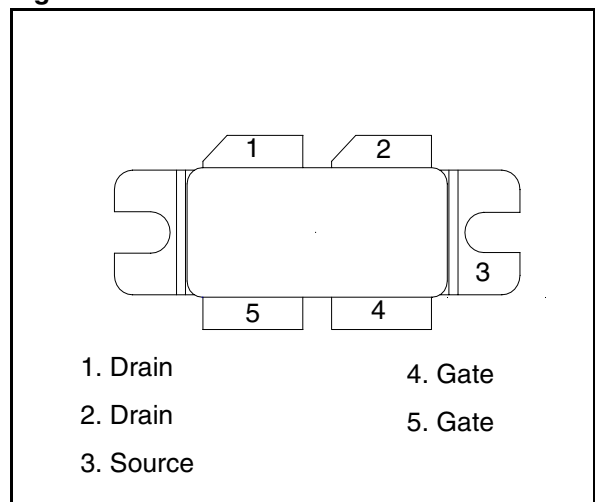


Table 1. Device summary

Order code	Package	Branding
SD57120	M252	SD57120

Contents

1 Electrical data 3

 1.1 Maximum ratings 3

 1.2 Thermal data 3

2 Electrical characteristics 4

 2.1 Static 4

 2.2 Dynamic 4

3 Impedance 5

4 Typical performance 6

5 Test circuit 8

6 Text circuit layout 10

7 Package mechanical data 11

8 Revision history 13

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings ($T_{CASE} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current	14	A
P_{DISS}	Power dissipation (@ $T_c = 70^{\circ}C$)	236	W
T_J	Max. operating junction temperature	200	$^{\circ}C$
T_{STG}	Storage temperature	-65 to + 150	$^{\circ}C$

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.55	$^{\circ}C/W$

2 Electrical characteristics

$$T_{\text{CASE}} = +25\text{ }^{\circ}\text{C}$$

2.1 Static

Table 4. Static

Symbol	Test conditions		Min	Typ	Max	Unit
$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{ V}$	$I_{\text{DS}} = 1\text{ mA}$	65			V
I_{DSS}	$V_{\text{GS}} = 0\text{ V}$	$V_{\text{DS}} = 28\text{ V}$			1	μA
I_{GSS}	$V_{\text{GS}} = 20\text{ V}$	$V_{\text{DS}} = 0\text{ V}$			1	μA
$V_{\text{GS(Q)}}$	$V_{\text{DS}} = 28\text{ V}$	$I_{\text{D}} = 100\text{ mA}$	2.0		5.0	V
$V_{\text{DS(ON)}}$	$V_{\text{GS}} = 10\text{ V}$	$I_{\text{D}} = 3\text{ A}$		0.7	0.9	V
G_{FS}	$V_{\text{DS}} = 10\text{ V}$	$I_{\text{D}} = 3\text{ A}$		3		S
$C_{\text{ISS}}^{(1)}$	$V_{\text{GS}} = 0\text{ V}$	$V_{\text{DS}} = 28\text{ V}$		169		pF
C_{OSS}	$V_{\text{GS}} = 0\text{ V}$	$V_{\text{DS}} = 28\text{ V}$		48		pF
C_{RSS}	$V_{\text{GS}} = 0\text{ V}$	$V_{\text{DS}} = 28\text{ V}$		2.7		pF

1. Includes Internal Input Moscap.

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions		Min	Typ	Max	Unit
P_{OUT}	$V_{\text{DD}} = 28\text{ V}$	$I_{\text{DQ}} = 800\text{ mA}$ $f = 960\text{ MHz}$	120			W
G_{PS}	$V_{\text{DD}} = 28\text{ V}$	$I_{\text{DQ}} = 800\text{ mA}$ $P_{\text{OUT}} = 120\text{ W}$ $f = 960\text{ MHz}$	13	14		dB
h_{D}	$V_{\text{DD}} = 28\text{ V}$	$I_{\text{DQ}} = 800\text{ mA}$ $P_{\text{OUT}} = 120\text{ W}$ $f = 960\text{ MHz}$	50			%
Load mismatch	$V_{\text{DD}} = 28\text{ V}$	$I_{\text{DQ}} = 800\text{ mA}$ $P_{\text{OUT}} = 120\text{ W}$ $f = 960\text{ MHz}$ All phase angles	10:1			VSW R

3 Impedance

Figure 2. Current conventions

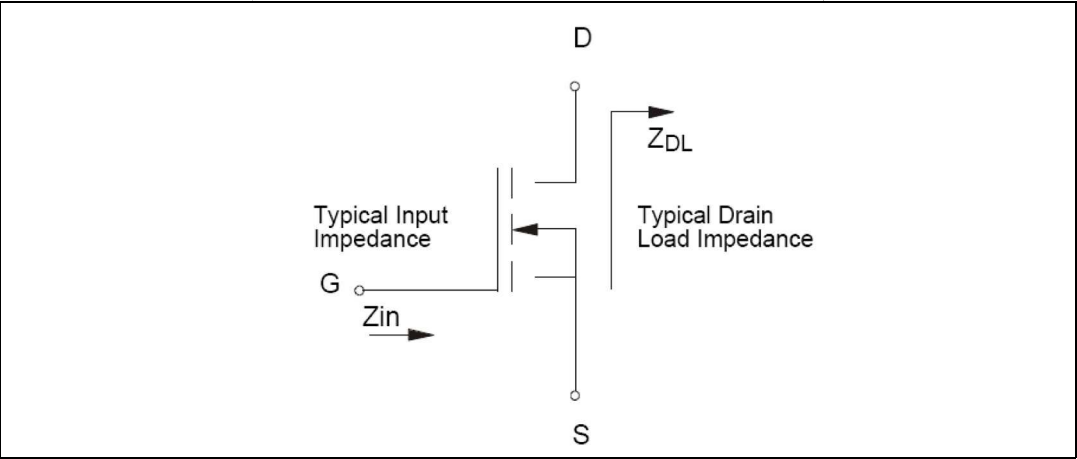


Table 6. Impedance data

Freq. (MHz)	$Z_{IN} (\Omega)$	$Z_{DL}(\Omega)$
945 MHz	$3.9 + j\ 4.9$	$3.26 - j\ 5.1$
960 MHz	$4.1 + j\ 4.6$	$3.24 - j\ 4.74$
980 MHz	$3.9 + j\ 5.2$	$3.27 - j\ 6.9$

Note: Measured gateto gate and drain to drain respectively.

4 Typical performance

Figure 3. Output power and efficiency vs input power

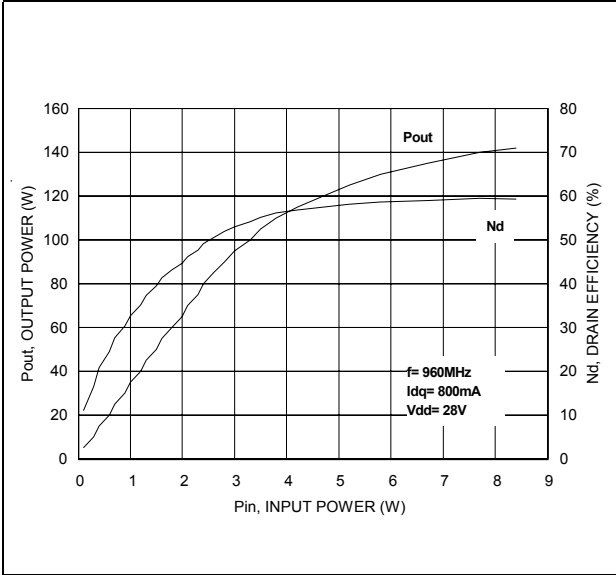


Figure 4. Power gain vs output power

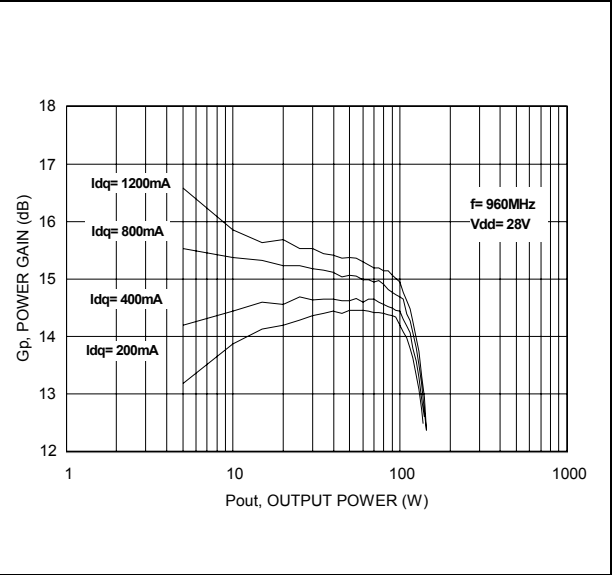


Figure 5. Intermodulation distortion vs output power

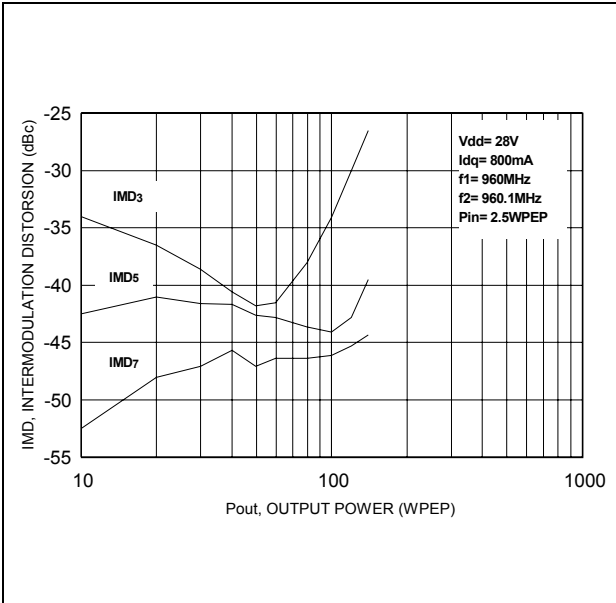


Table 7. Intermodulation distortion vs output power

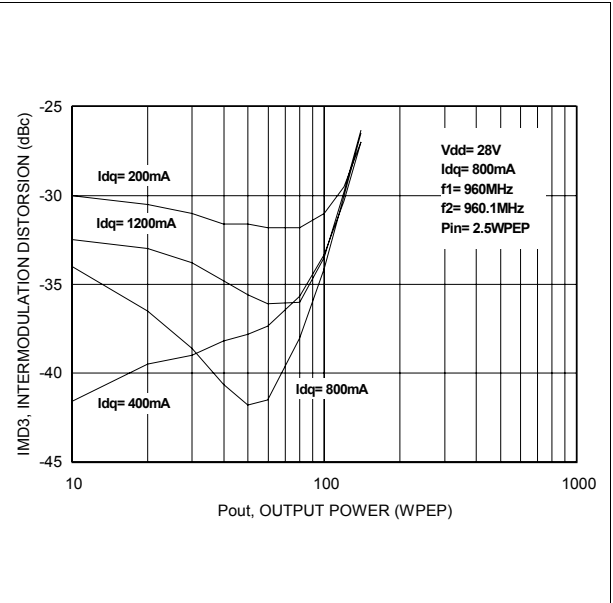


Table 8. Output power vs gate voltage

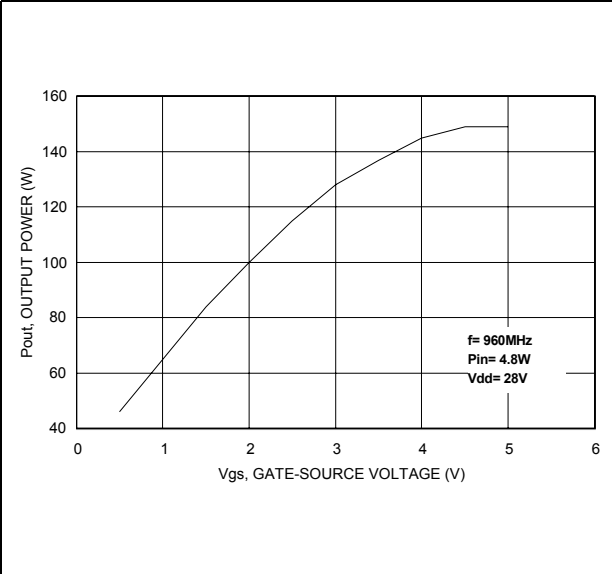


Figure 6. Output power vs drain voltage

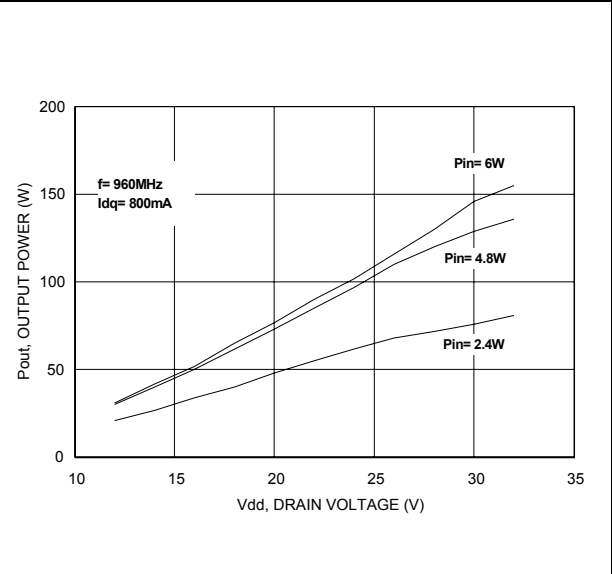


Figure 7. Capacitance vs drain voltage

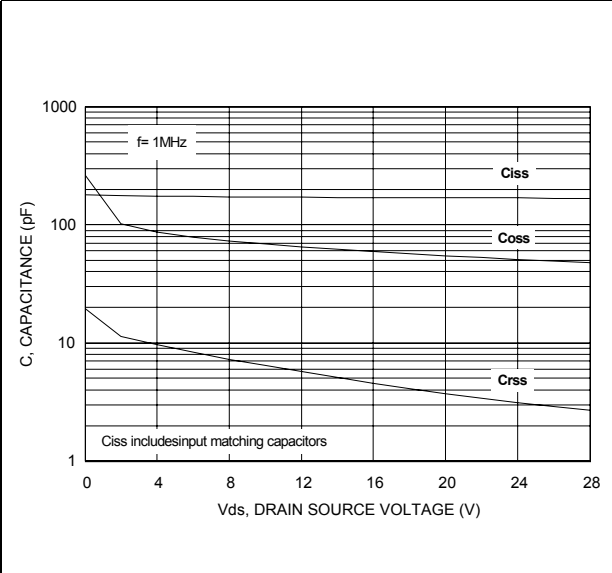
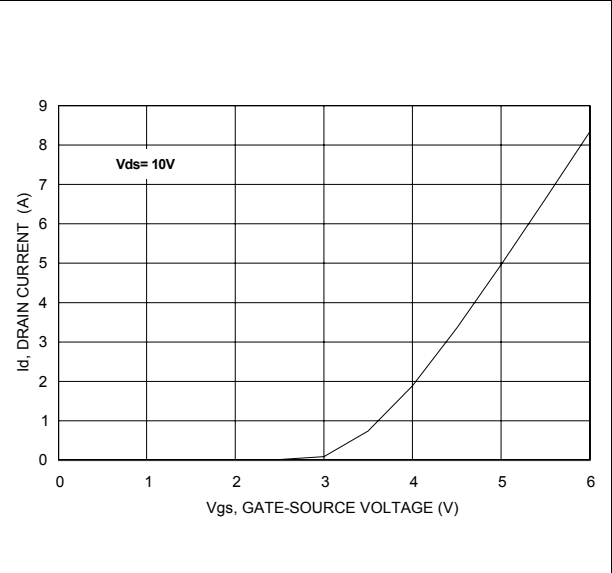
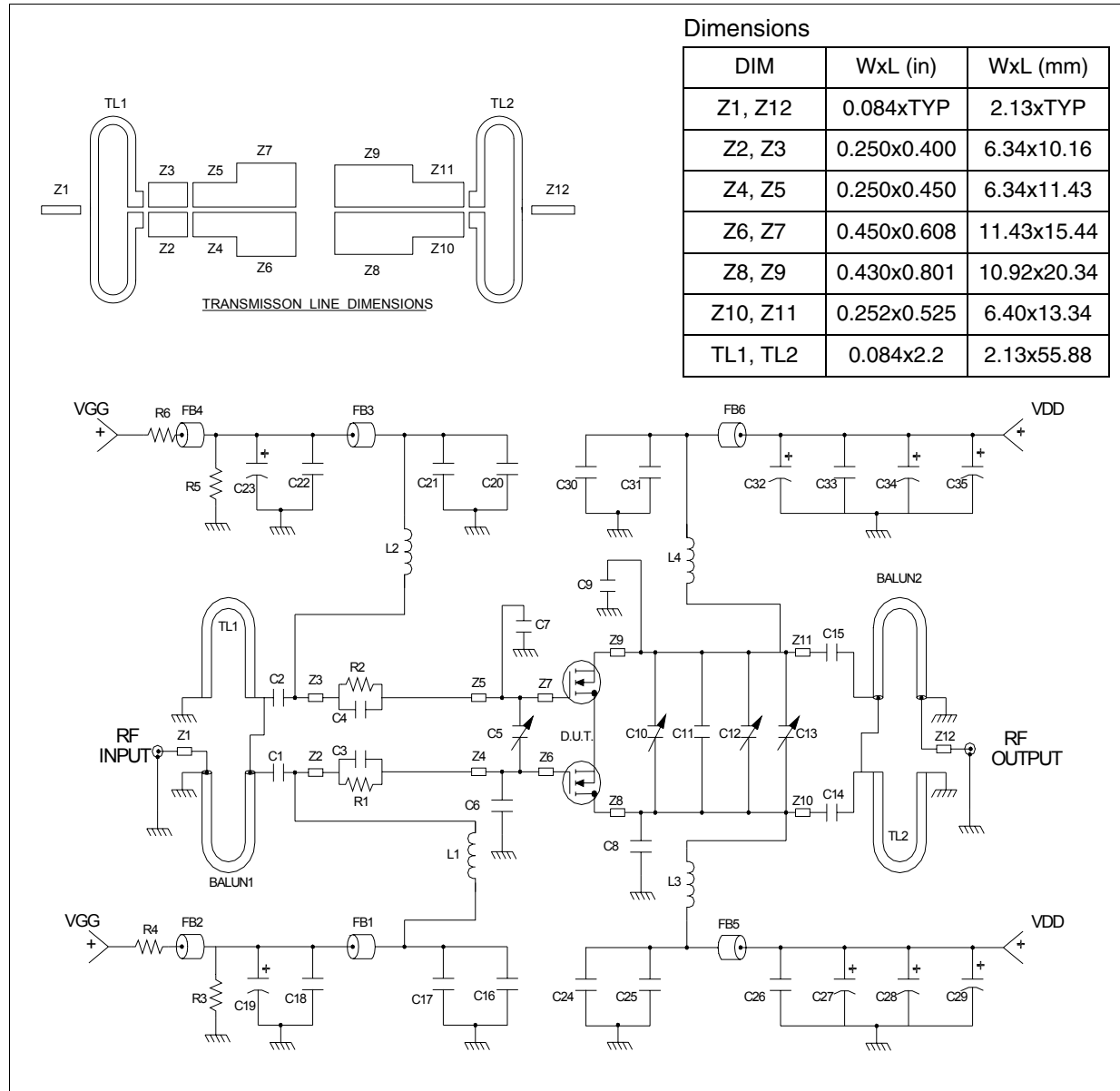


Figure 8. Drain current vs gate voltage



5 Test circuit

Figure 9. 960MHz test circuit schematic



- 1 Dimensions at component symbols are reference for component placement.
- 2 Gap between ground & transmission line = 0.056 [1.42] +0.002 [0.05] -0.000 [0.00] typ.
- 3 Dimension of microstrip = 1/2 printed balun only.

Table 9. Test circuit component part list

Component	Description
BF1-BF4	SURFACE MOUNT EMI SHIELD BEAD
L1,L2,L3,L4	INDUCTOR, 3 TURN AIR-WOUND #20AWG ID=0.126[3.20] 24.7nH MAGNET WIRE
B1, B2	BALUN, 50 OHM SUCOFORM, OD 0.141. 2.20 LG COAXIAL CABLE OR EQUIVALENT
R1,R2	75 OHM 1 W SURFACE MOUNT CHIP RESISTOR
R3,R5	1.2 K OHM 1 W SURFACE MOUNT CHIP RESISTOR
R4,R6	1 K OHM 1 W SURFACE MOUNT CHIP RESISTOR
C1,C2,C14,C15	47 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C3,C4	42 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C5,C12	0.8-8 pF GIGATRIM VARIABLE CAPACITOR
C6,C7,C11	1.7 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C8,C9	5.6 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C10,C13	0.6-4.5 pF GIGATRIM VARIABLE CAPACITOR
C16,C17,C20,C21, C24,C25,C30,C31	300 pF ATC 700B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C18,C22	10000 pF ATC 200B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C19,C23,C27,C28, C32,C34	10 μ F, 50 V ALUMINUM ELECTROLYTICS RADIAL LEAD CAPACITOR
C26,C33	20000 pF ATC 900B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C29,C35	220 μ F, 50 V ALUMINUM ELECTROLYTICS RADIAL LEAD CAPACITOR
BOARD	ULTRA LAM 2000. 0.030" THK, $\epsilon_r = 2.55$, 2 O ₂ ED CU BOTH SIDES

6 Text circuit layout

Figure 10. 960MHz production test fixture

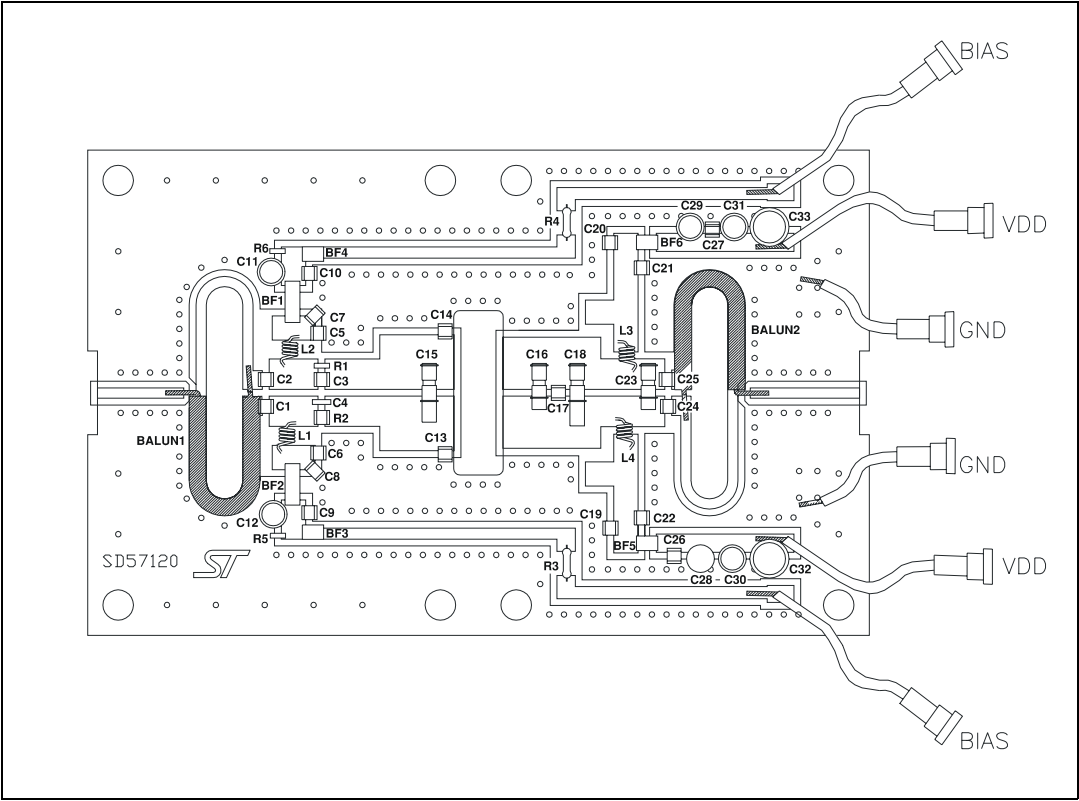
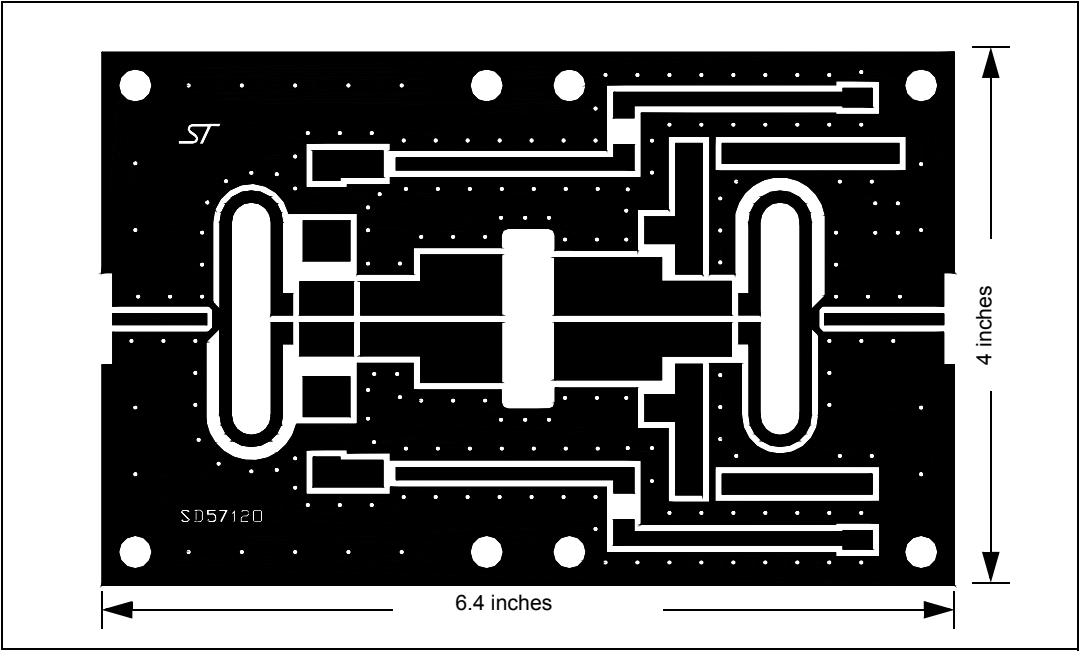


Figure 11. 960MHz test circuit photomaster

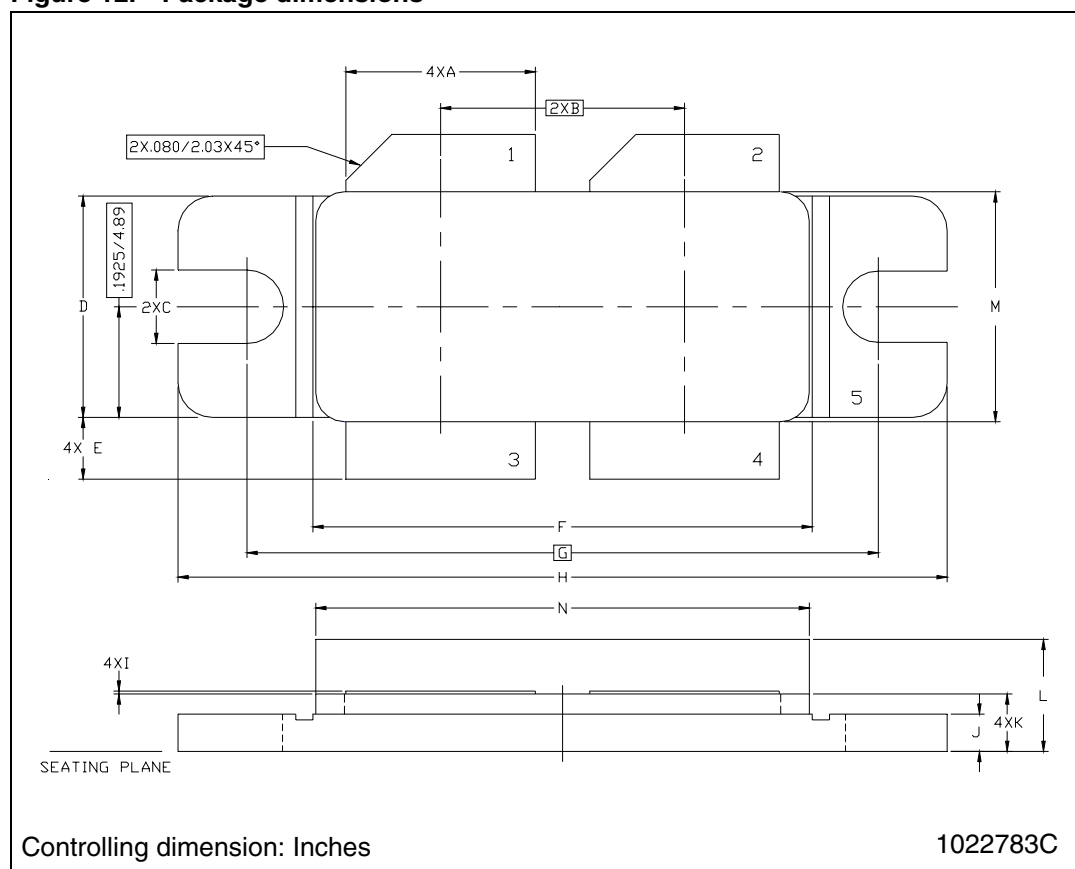


7 Package mechanical data

Table 10. M252 (.400 x .860 4L BAL N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	8.13		8.64	.320		.340
B		10.80			.425	
C	3.00		3.30	.118		.130
D	9.65		9.91	.380		.390
E	2.16		2.92	.085		.115
F	21.97		22.23	.865		.875
G		27.94			1.100	
H	33.91		34.16	1.335		1.345
I	0.10		0.15	.004		.006
J	1.52		1.78	.060		.070
K	2.36		2.74	.093		.108
L	4.57		5.33	.180		.210
M	9.96		10.34	.392		.407
N	21.64		22.05	.852		.868

Figure 12. Package dimensions



8 Revision history

Table 11. Document revision history

Date	Revision	Changes
24-Mar-2003	6	First Issue.
11-Jul-2007	7	Document reformatted, added lead free info
27-Aug-2007	8	Cover page title updated

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