



STP10NK80Z, STP10NK80ZFP, STW10NK80Z

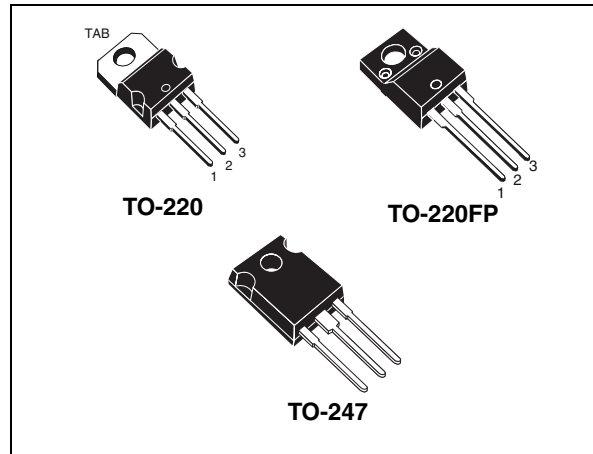
N-channel 800 V, 0.78 Ω , 9 A Zener-protected SuperMESH™ Power MOSFETs in TO-220, TO-220FP and TO-247 packages

Datasheet — production data

Features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STP10NK80Z	800V	<0.90 Ω	9A	160 W
STP10NK80ZFP	800V	<0.90 Ω	9A	40 W
STW10NK80Z	800V	<0.90 Ω	9A	160 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeability



Applications

- Switching application

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram

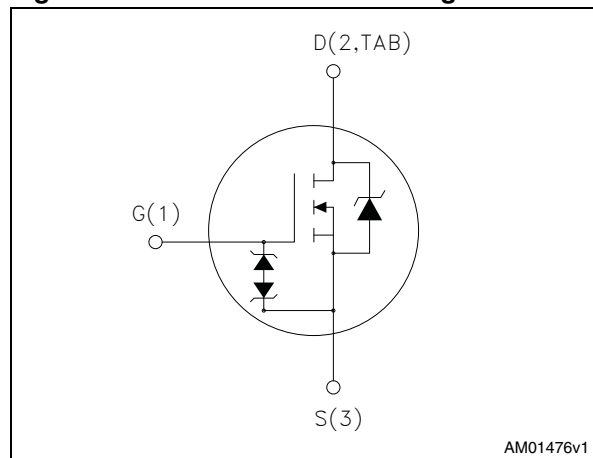


Table 1. Device summary

Part number	Marking	Package	Packaging
STP10NK80Z	P10NK80Z	TO-220	Tube
STP10NK80ZFP	P10NK80ZFP	TO-220FP	Tube
STW10NK80Z	W10NK80Z	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/ TO-247	TO-220FP	
V_{DSS}	Drain-source voltage ($V_{GS} = 0$)	800		V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20k\Omega$)	800		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25^\circ C$	9	$9^{(1)}$	A
I_D	Drain current (continuous) at $T_C = 100^\circ C$	6	$6^{(1)}$	A
$I_{DM}^{(2)}$	Drain current (pulsed)	36	$36^{(1)}$	A
P_{TOT}	Total dissipation at $T_C = 25^\circ C$	160	40	W
	Derating factor	1.28	0.32	W/ $^\circ C$
Vesd(G-S)	G-S ESD (HBM C=100pF, R=1.5k Ω)	4		kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (DC)	--	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150		$^\circ C$

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 9$ A, $di/dt \leq 200$ A/ μs , $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-220FP	TO-247	
$R_{thj-case}$	Thermal resistance junction-case Max	0.78	3.1	0.78	$^\circ C/W$
R_{thj-a}	Thermal resistance junction-ambient Max	62.5		50	$^\circ C/W$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J Max)	9	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ C$, $I_d = I_{AS}$, $V_{DD} = 50V$)	290	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	800			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 800V$ $V_{DS} = 800V, T_C = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 4.5A$		0.78	0.9	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 4.5A$	-	9.6	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 MHz, V_{GS} = 0$	-	2180 205 38	-	pF pF pF
$C_{oss eq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 640V$	-	105	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 640V, I_D = 9A$ $V_{GS} = 10V$ See Figure 20	-	72 12.5 37	-	nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=400\text{ V}$, $I_D=4.5\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ See Figure 21		30 20		ns ns
$t_{d(off)}$ t_f	Turn-off delay Time Fall time	$V_{DD}=400\text{ V}$, $I_D=4.5\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ See Figure 21		65 17		ns ns

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS}=\pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

Table 9. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=9\text{ A}$, $V_{GS}=0$	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=45\text{ V}$, $T_j=150^\circ\text{C}$	-	645 6.4 20		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

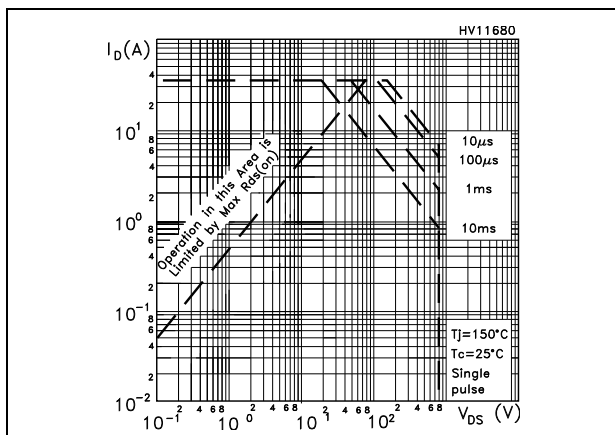


Figure 3. Thermal impedance for TO-220

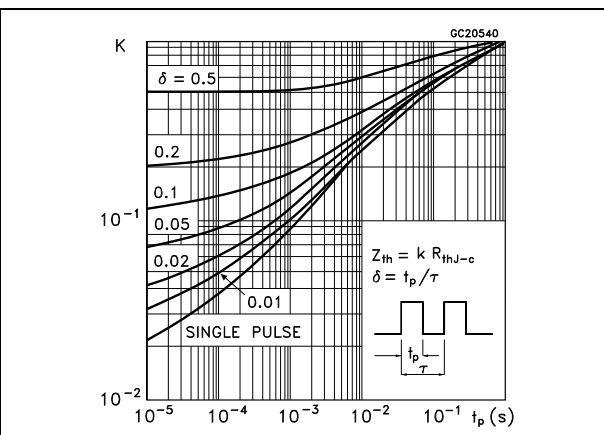


Figure 4. Safe operating area for TO-220FP

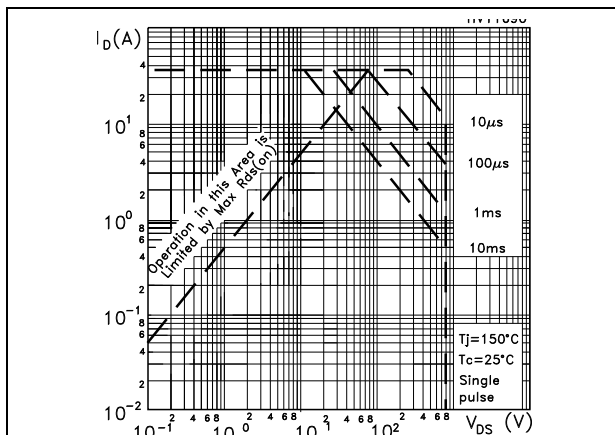


Figure 5. Thermal impedance for TO-220FP

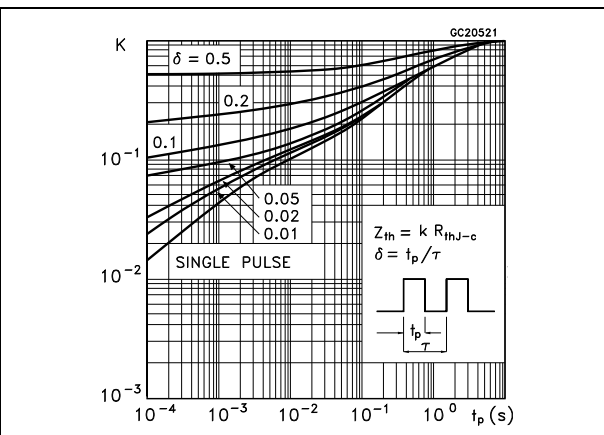


Figure 6. Safe operating area for TO-247

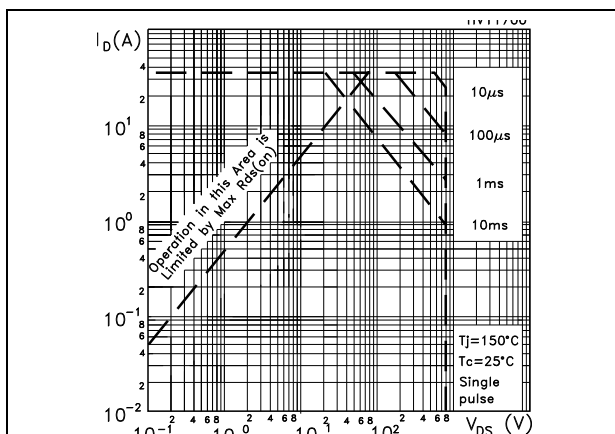


Figure 7. Thermal impedance for TO-247

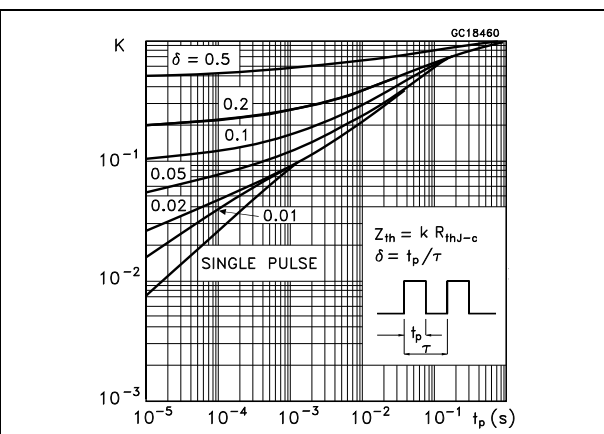


Figure 8. Output characteristics

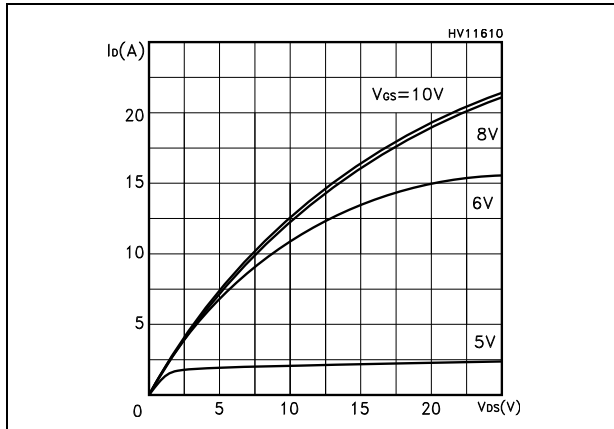


Figure 9. Transfer characteristics

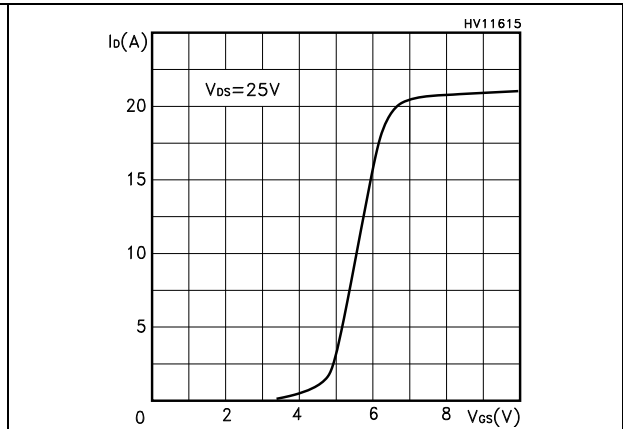


Figure 10. Transconductance

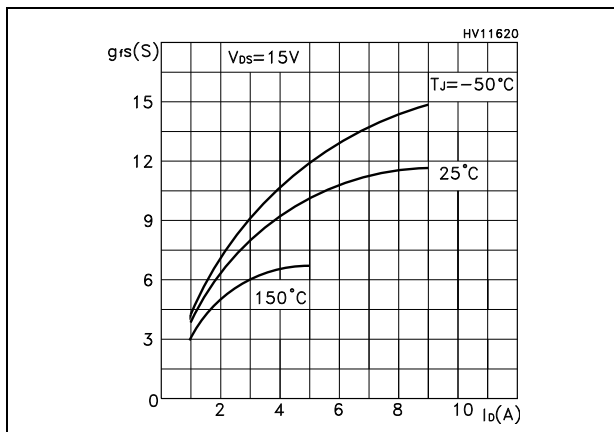


Figure 11. Static drain-source on resistance

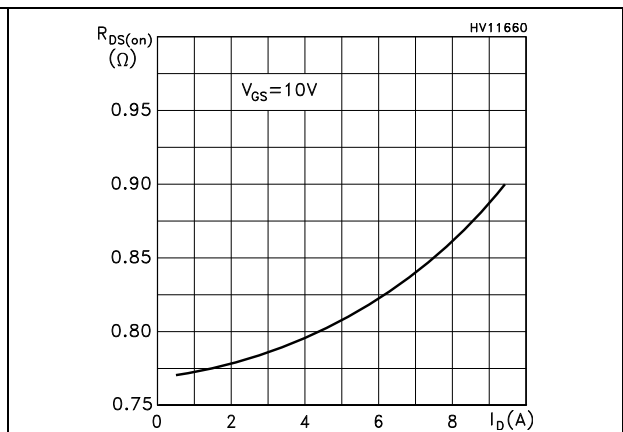


Figure 12. Gate charge vs gate-source voltage Figure 13. Capacitance variations

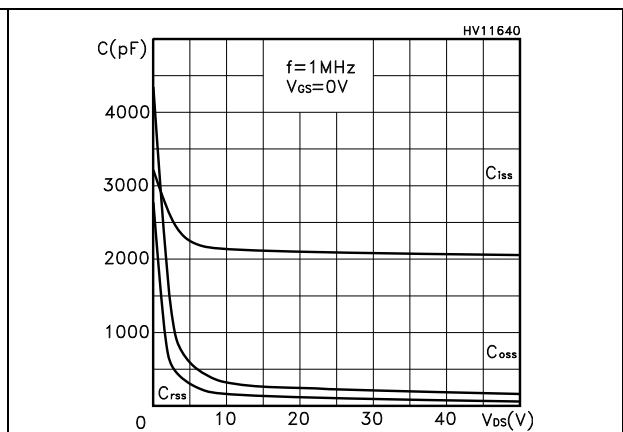
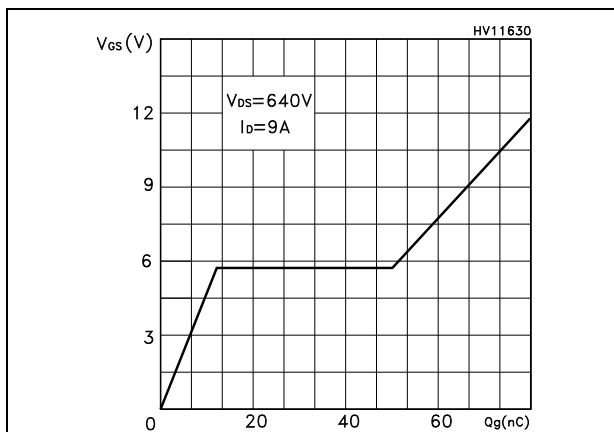


Figure 14. Normalized gate threshold voltage vs temperature

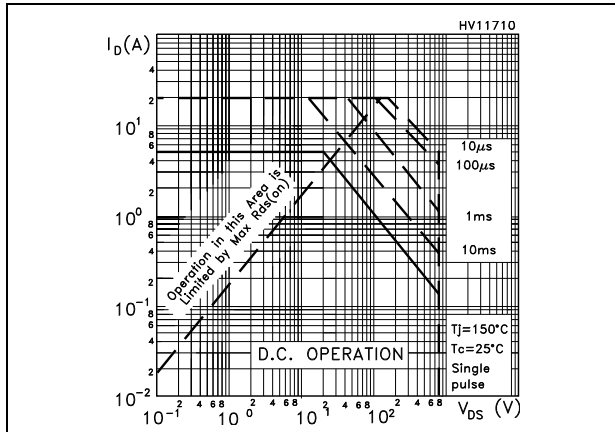


Figure 15. Normalized on resistance vs temperature

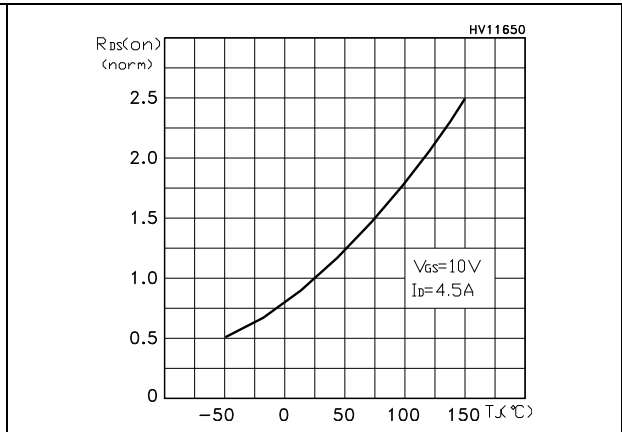


Figure 16. Source-drain diode forward characteristics

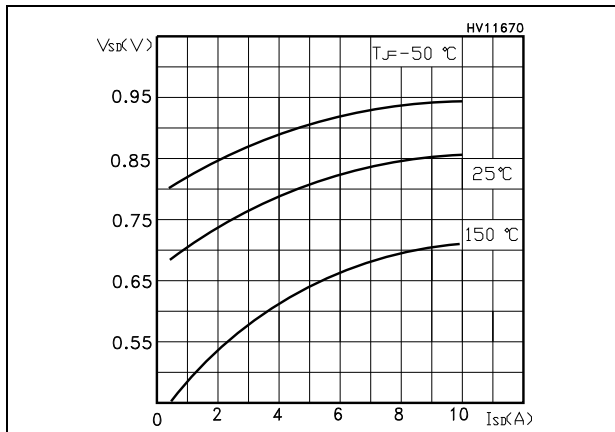


Figure 17. Normalized BV_{DSS} vs temperature

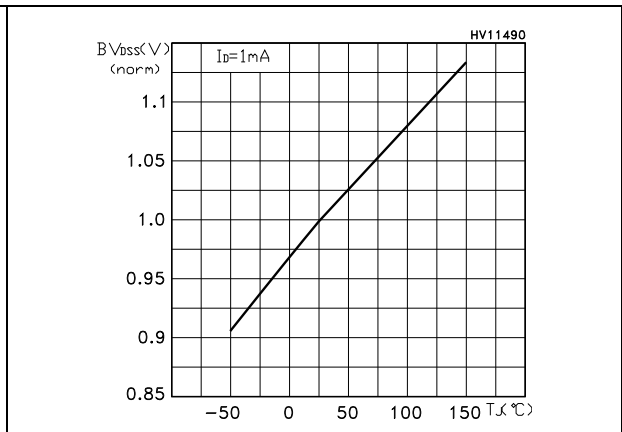
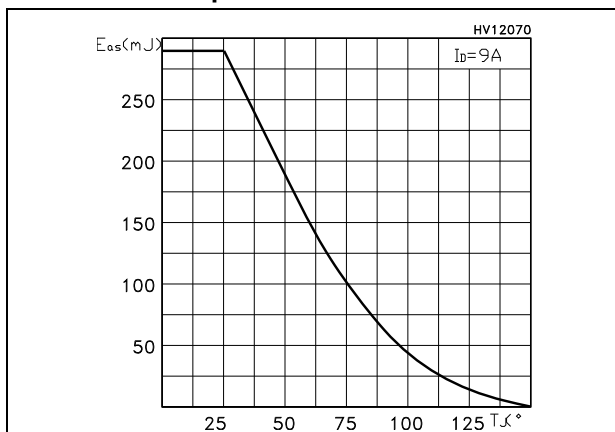


Figure 18. Maximum avalanche energy vs temperature



3 Test circuit

Figure 19. Switching times test circuit for resistive load

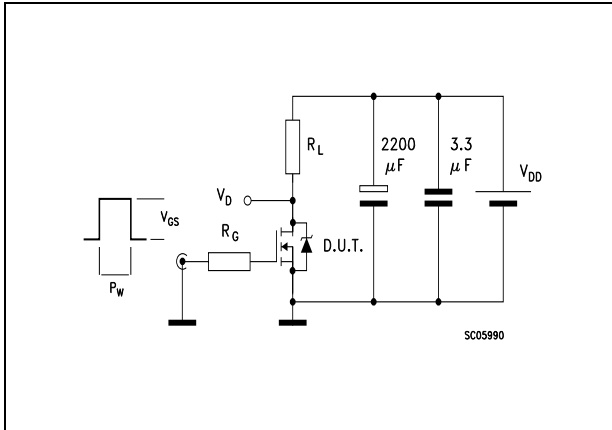


Figure 20. Gate charge test circuit

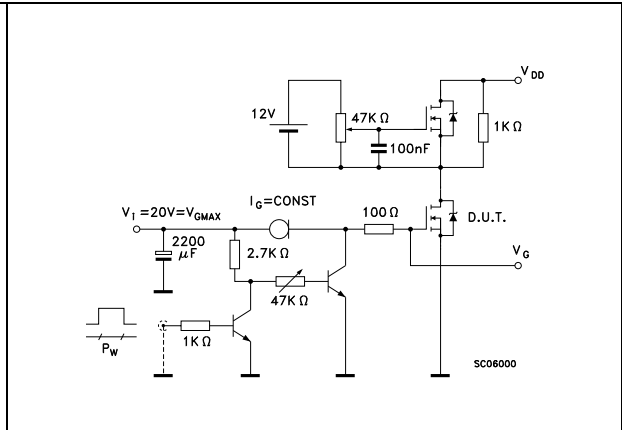


Figure 21. Test circuit for inductive load switching and diode recovery times

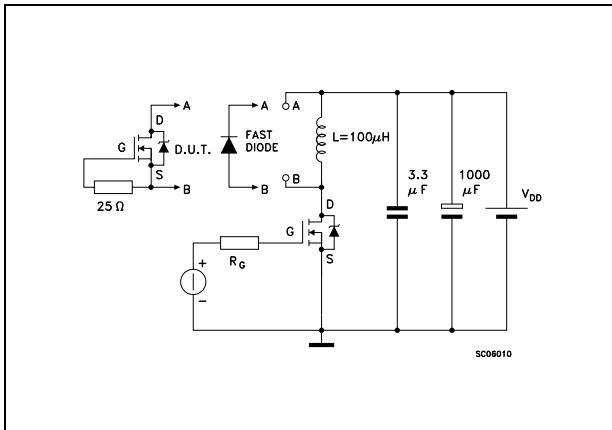


Figure 22. Unclamped Inductive load test circuit

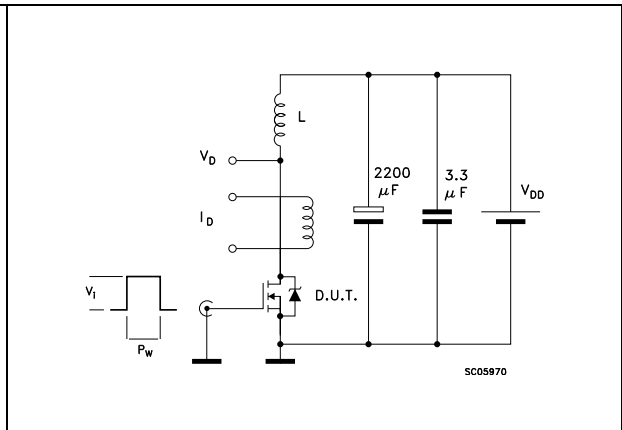


Figure 23. Unclamped inductive waveform

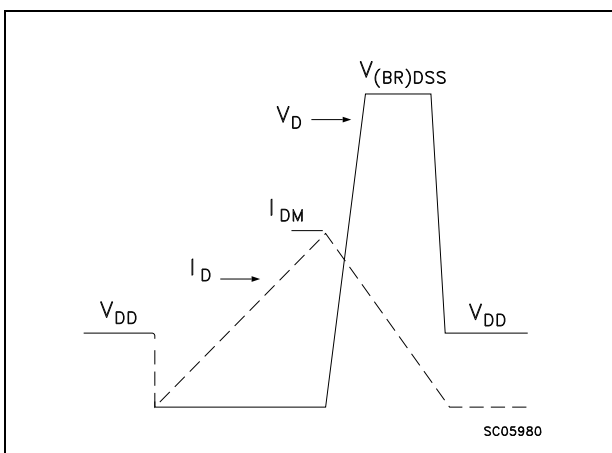
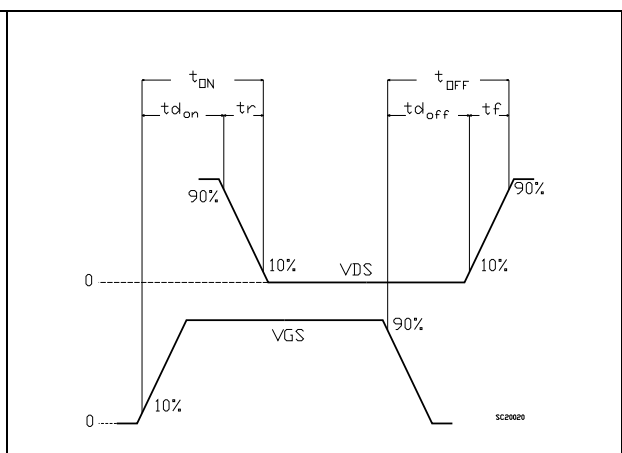


Figure 24. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 25. TO-220 type A drawing

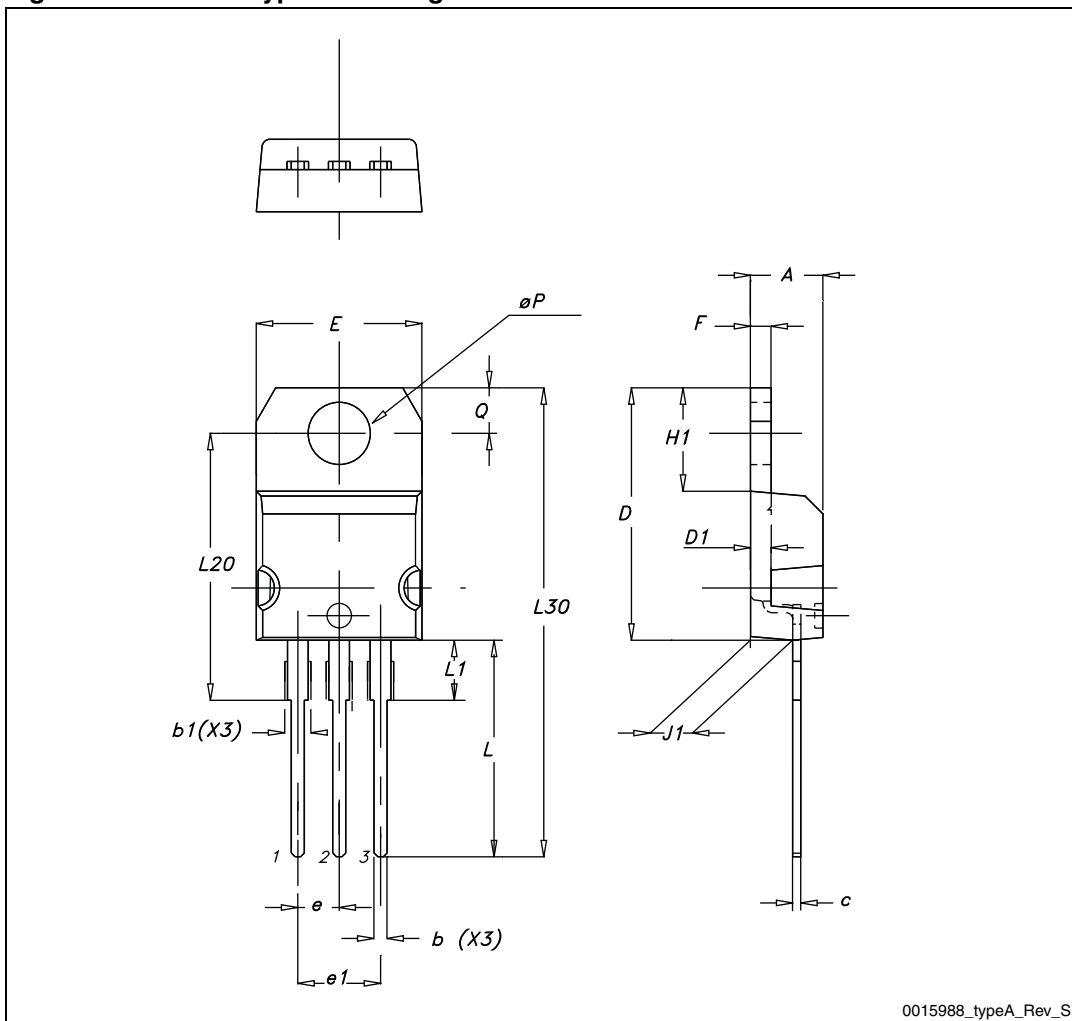


Table 11. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 26. TO-220FP drawing

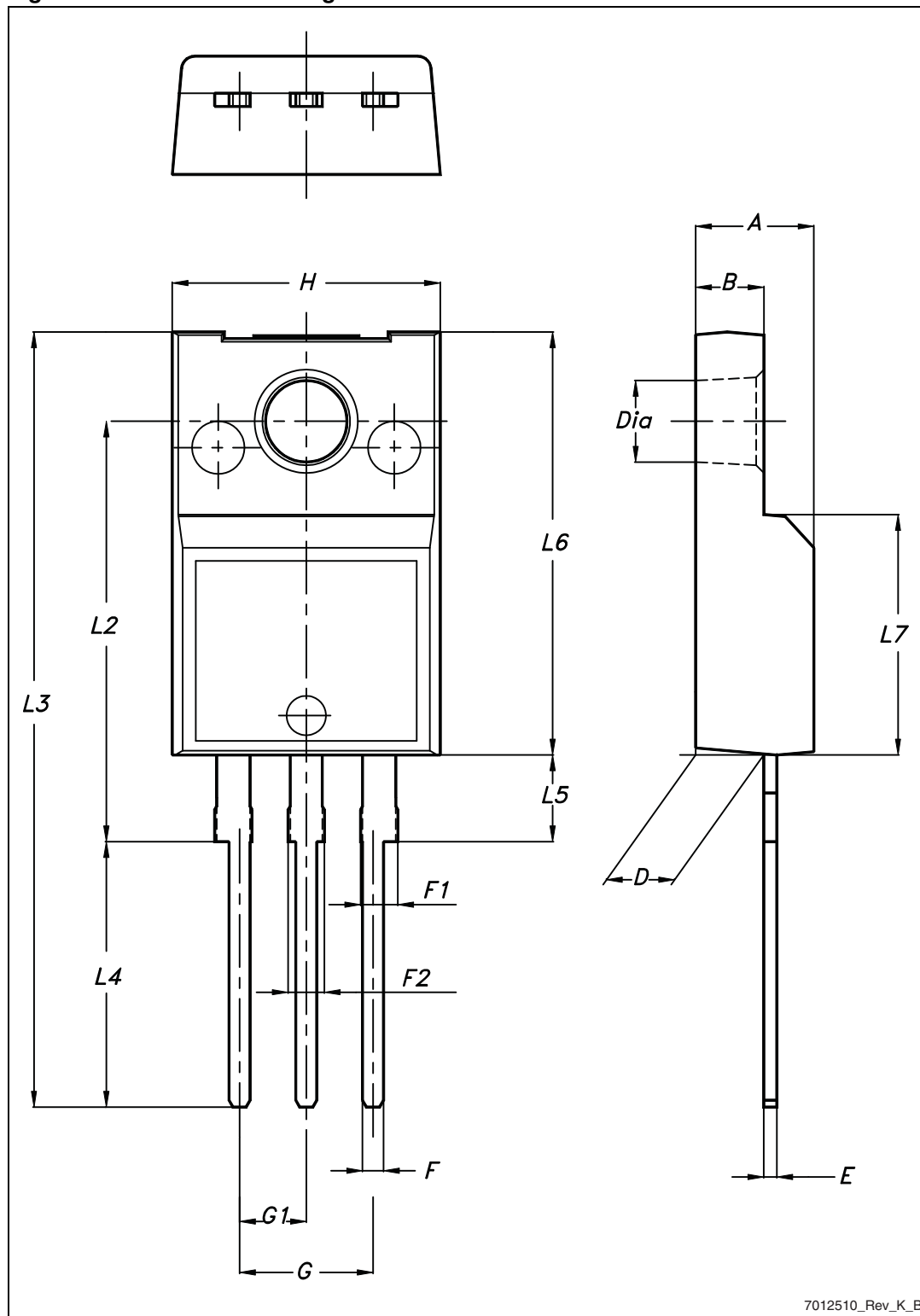
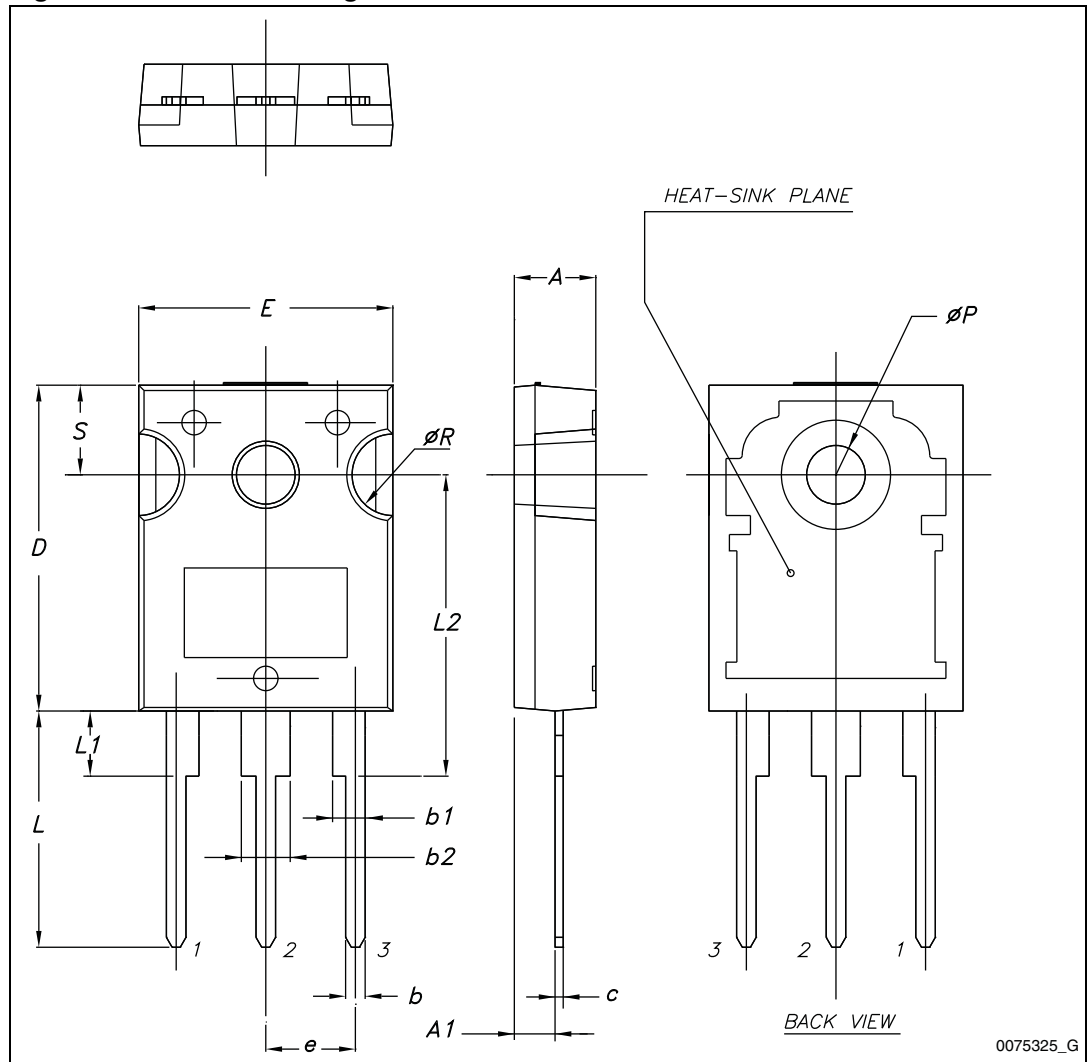


Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 27. TO-247 drawing



0075325_G

5 Revision history

Table 13. Document revision history

Date	Revision	Changes
08-Sep-2005	4	Complete document
10-Mar-2006	5	Inserted ecopack indication
28-Sep-2005	6	New template, no content change
15-Mar-2012	7	Content reworked to improve readability. Minor text changes in cover page. Updated Table 5 . Updated Section 4: Package mechanical data .

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