



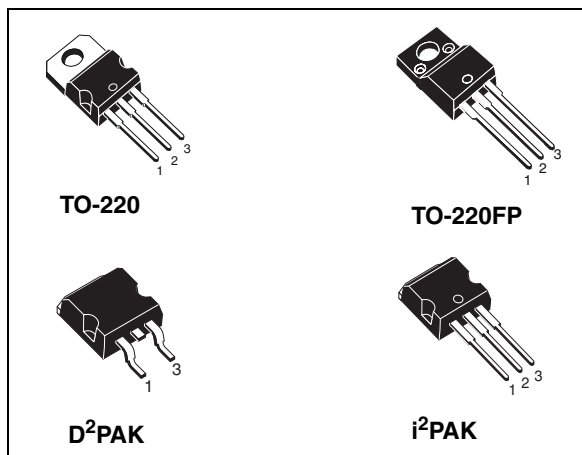
# STP11NM60 - STP11NM60FP STB11NM60 - STB11NM60-1

N-channel 650V @  $T_{Jmax}$  -  $0.4\Omega$  - 11A TO-220/FP/D<sup>2</sup>PAK/I<sup>2</sup>PAK  
MDmesh™ Power MOSFET

## General features

Type	$V_{DSS}$ (@ $T_J=T_{Jmax}$ )	$R_{DS(on)}$	$I_D$
STP11NM60	650V	<0.45 $\Omega$	11A
STP11NM60FP	650V	<0.45 $\Omega$	11A
STB11NM60	650V	<0.45 $\Omega$	11A
STB11NM60-1	650V	<0.45 $\Omega$	11A

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



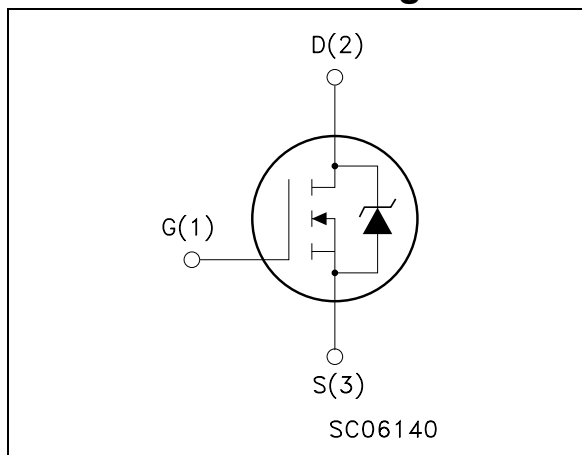
## Description

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

## Applications

- Switching application

## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STB11NM60T4	B11NM60	D <sup>2</sup> PAK	Tape & reel
STB11NM60-1	B11NM60-1	I <sup>2</sup> PAK	Tube
STP11NM60	P11NM60	TO-220	Tube
STP11NM60FP	P11NM60FP	TO-220FP	Tube

## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220/D <sup>2</sup> PAK/I <sup>2</sup> PAK	TO-220FP	
V <sub>GS</sub>	Gate- source voltage	±30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25°C	11	11 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> =100°C	7	7 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	44	44 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25°C	160	35	W
	Derating Factor	1.28	0.28	W/°C
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (DC)	--	2500	V
T <sub>J</sub>	Operating junction temperature	-65 to 150		°C
T <sub>stg</sub>	Storage temperature	150		°C

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- I<sub>SD</sub> ≤ 11A, di/dt ≤ 400A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ T<sub>JMAX</sub>.

**Table 2. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220/D <sup>2</sup> PAK/I <sup>2</sup> PAK	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case Max	0.78	3.57	°C/W
R <sub>thj-a</sub>	Thermal resistance junction-ambient Max	62.5		°C/W
T <sub>I</sub>	Maximum lead temperature for soldering purpose	300		°C

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>J</sub> Max)	5.5	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> =25°C, I <sub>d</sub> =I <sub>ar</sub> , V <sub>dd</sub> =50V)	350	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600 V$ $V_{DS} = 600 V, T_c = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 5.5A$		0.4	0.45	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 5.5A$		5.2		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 MHz, V_{GS} = 0$		1000 230 25		pF pF pF
$C_{oss eq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 480V$		100		pF
$R_G$	Gate input resistance	$f = 1 MHz$ gate DC bias = 0 Test signal level = 20mV open drain		1.6		$\Omega$
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480V, I_D = 11A$ $V_{GS} = 10V$ (see Figure 15)		30 10 15		nC nC nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

2.  $C_{oss eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=300\text{ V}$ , $I_D=5.5\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$ <i>(see Figure 17)</i>		20 20		ns ns
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage rise time Fall time Cross-over time	$V_{DD}=480\text{ V}$ , $I_D=11\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$ <i>(see Figure 17)</i>		6 11 19		ns ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=11\text{ A}$ , $V_{GS}=0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=100\text{ V}$ , $T_j=25^\circ\text{C}$ <i>(see Figure 16)</i>		390 3.8 19.5		ns $\mu\text{C}$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=100\text{ V}$ , $T_j=150^\circ\text{C}$ <i>(see Figure 16)</i>		570 5.7 20		ns $\mu\text{C}$ A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/D<sup>2</sup>PAK/I<sup>2</sup>PAK

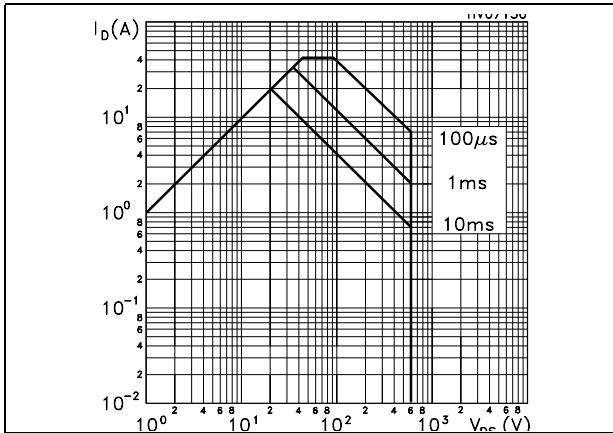


Figure 2. Thermal impedance TO-220 / D<sup>2</sup>PAK/I<sup>2</sup>PAK

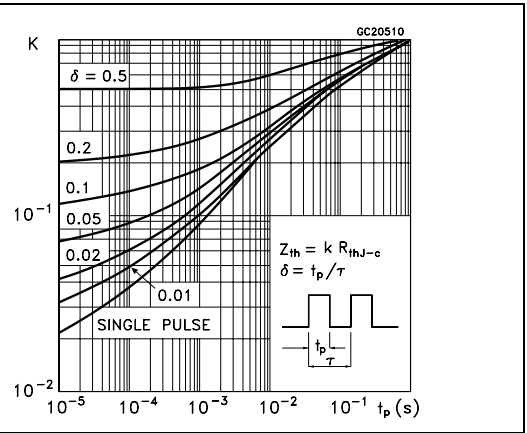


Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

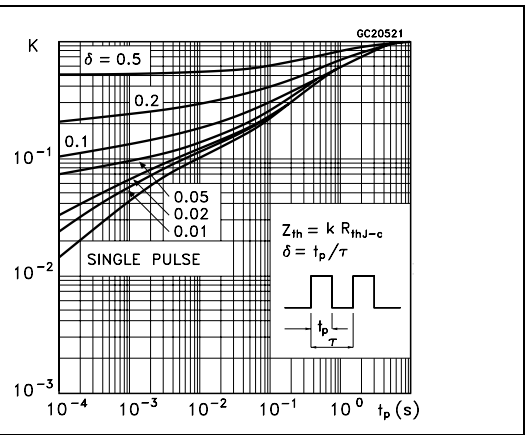
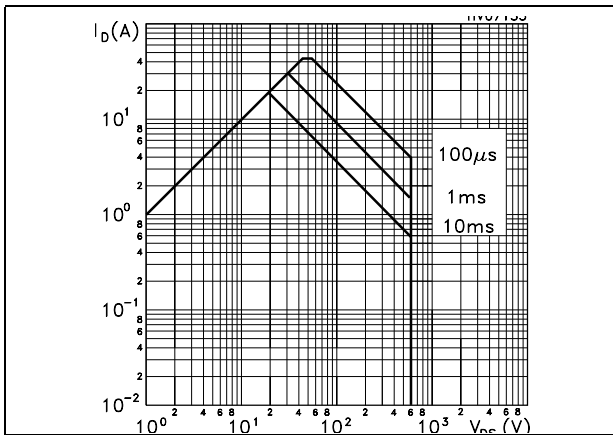


Figure 5. Output characteristics

Figure 6. Transfer characteristics

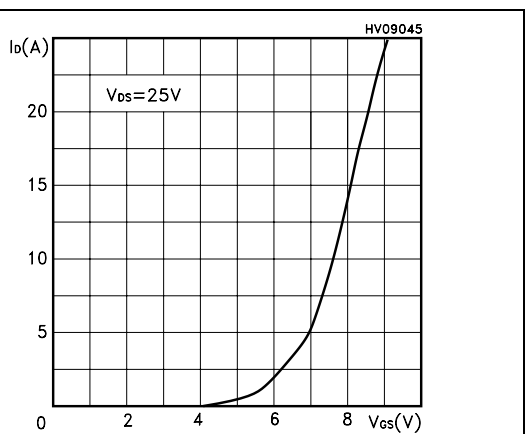
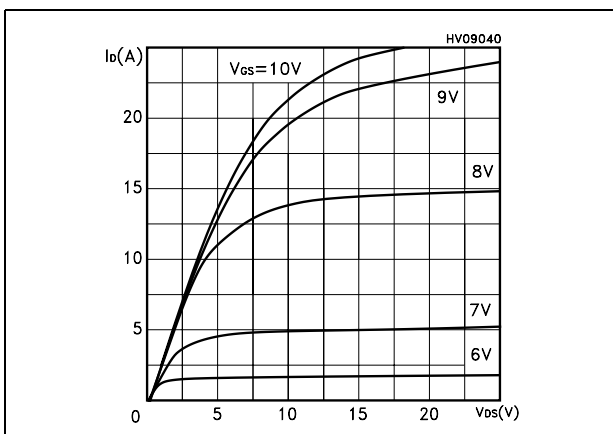


Figure 7. Transconductance

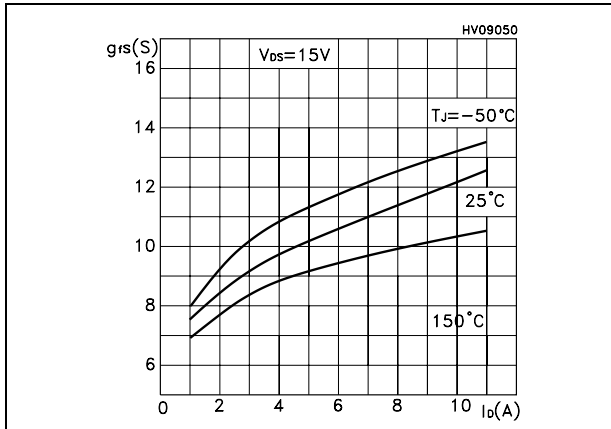


Figure 8. Static drain-source on resistance

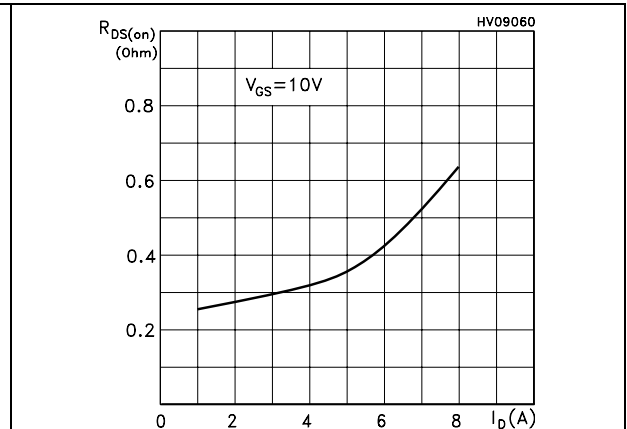


Figure 9. Gate charge vs gate-source voltage

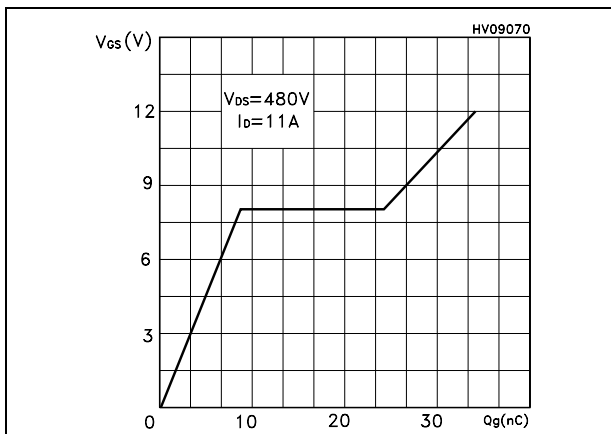


Figure 10. Capacitance variations

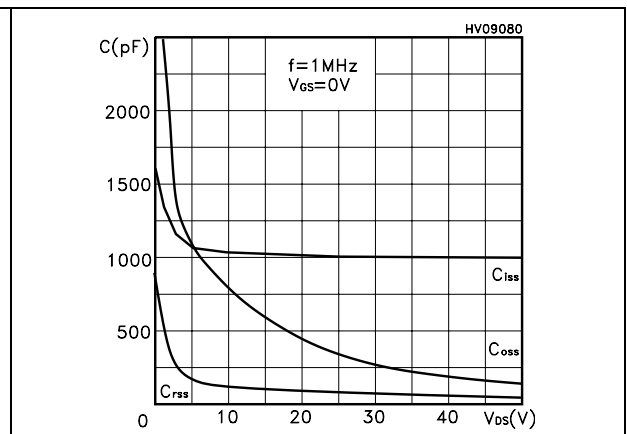


Figure 11. Normalized gate threshold voltage vs temperature

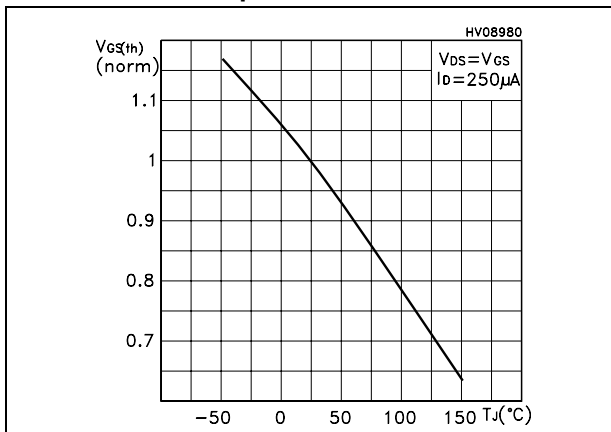
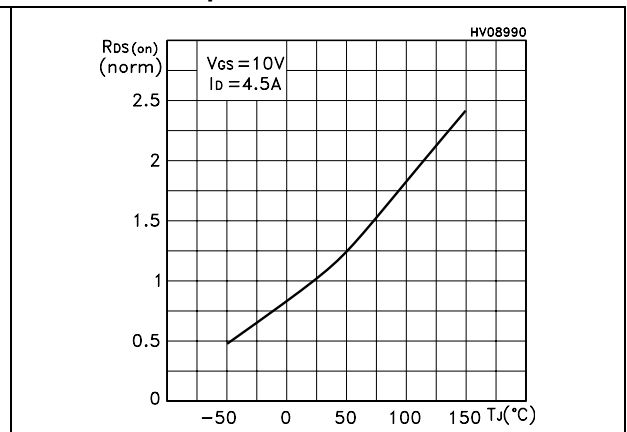
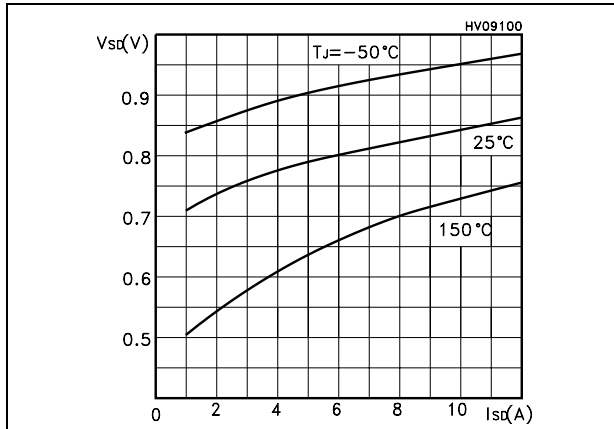


Figure 12. Normalized on resistance vs temperature



**Figure 13. Source-drain diode forward characteristics**





### 3 Test circuit

Figure 14. Switching times test circuit for resistive load

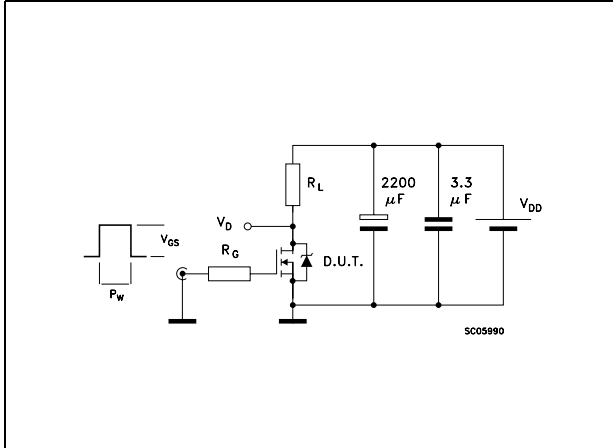


Figure 15. Gate charge test circuit

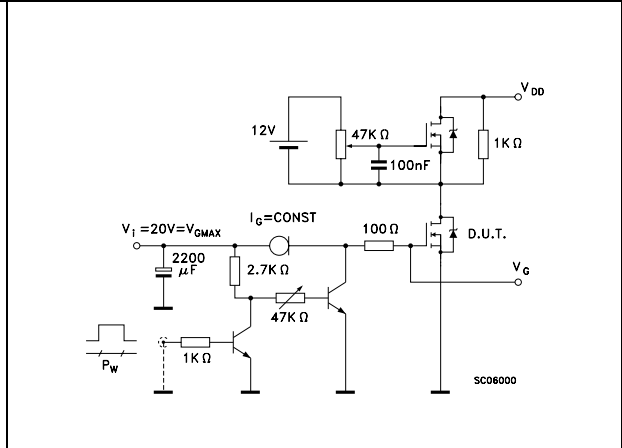


Figure 16. Test circuit for inductive load switching and diode recovery times

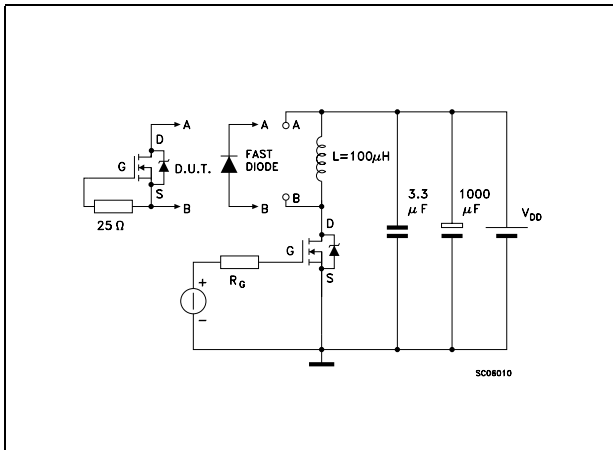


Figure 17. Unclamped Inductive load test circuit

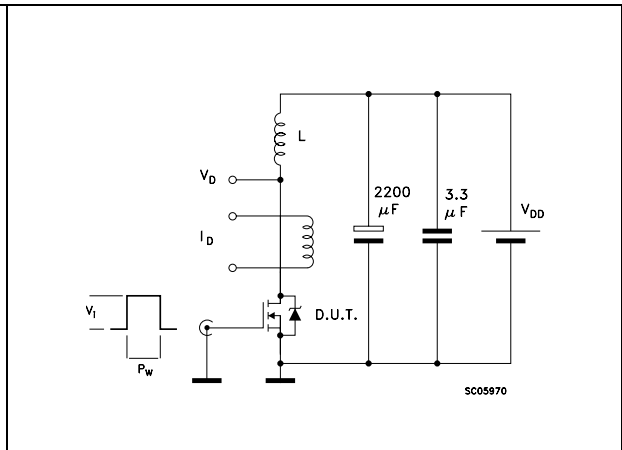


Figure 18. Unclamped inductive waveform

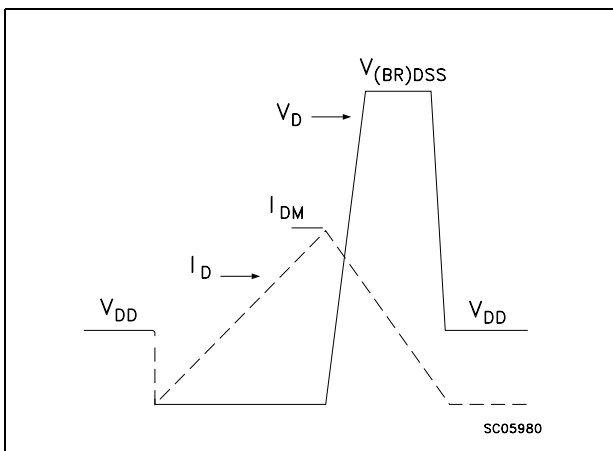
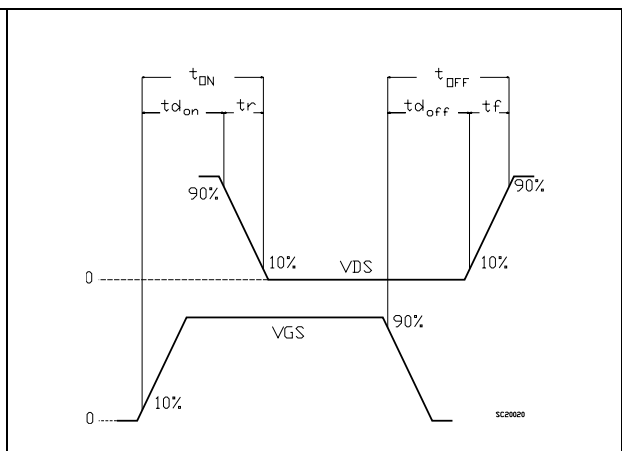


Figure 19. Switching time waveform

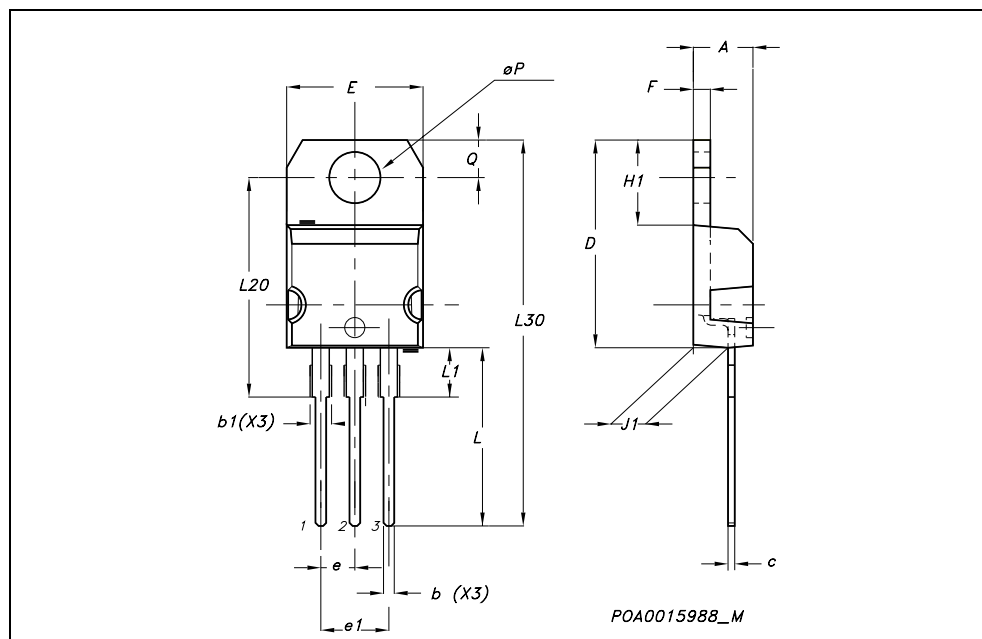


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

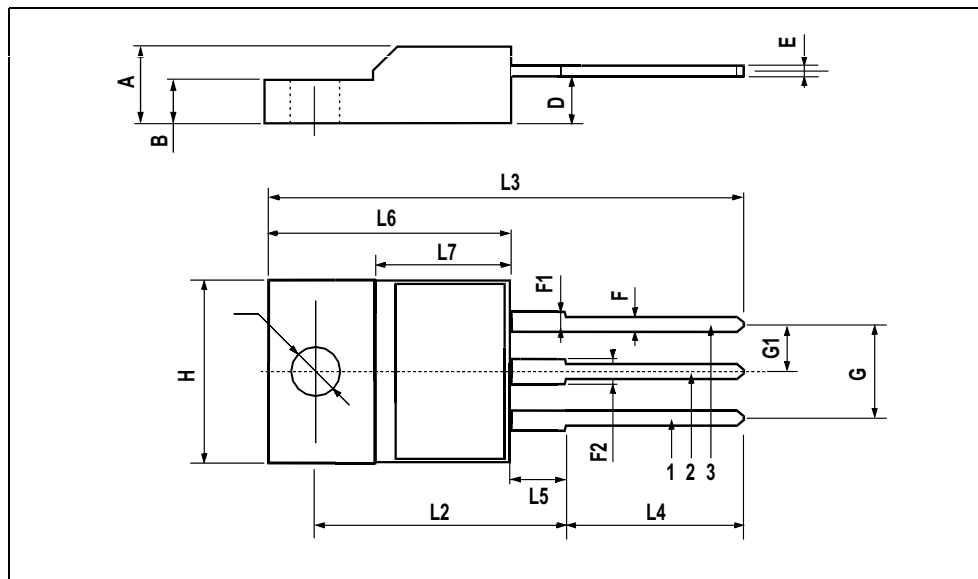
## TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
$\phi P$	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



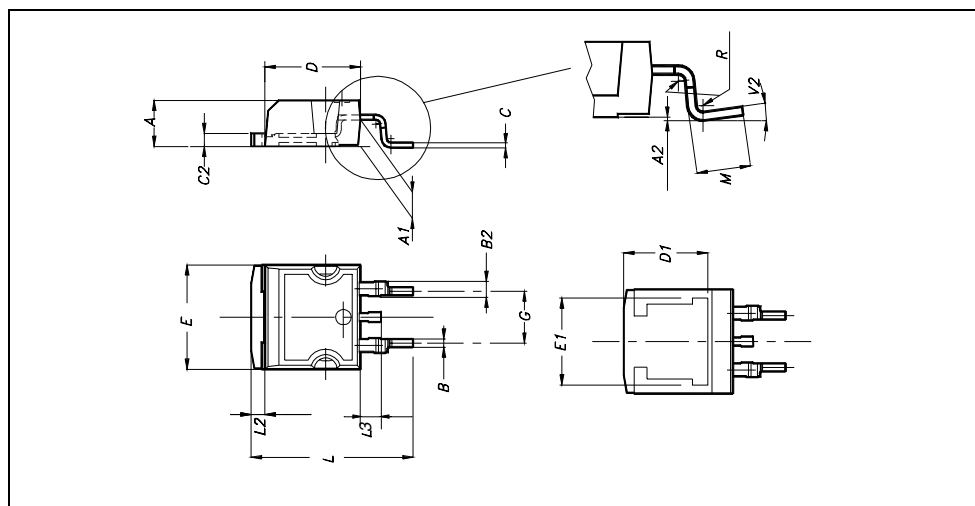
**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



D<sup>2</sup>PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



# 5 Packaging mechanical data

## D<sup>2</sup>PAK FOOTPRINT



## TAPE AND REEL SHIPMENT

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

10 pitches cumulative tolerance on tape +/- 0.2 mm

\* on sales type

## 6 Revision history

**Table 8. Revision history**

Date	Revision	Changes
09-Sep-2004	1	First Release
10-Jun-2005	2	Typing error, wrong description
26-Jul-2006	3	The document has been reformatted, no content change
31-Aug-2006	4	Typo mistake on order code
21-Dec-2006	5	Various changes on "Test conditions" for <a href="#">Table 5.</a> and <a href="#">Table 6.</a>
12-Jan-2007	6	Order code has been corrected

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