

Single line IPAD™, EMI filter and ESD protection

Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency EMI filtering
- Lead-free package
- 400 μm pitch
- Very low PCB space occupation: 0.6 mm²
- Very thin package: 0.6 mm
- High reliability offered by monolithic integration
- Reduction of parasitic elements through CSP integration

Complies with the following standards

- IEC 61000-4-2 level 4 on internal and external pins:
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883F - Method 3015.7 Class 3

Application

- TV analog signal in TV_OUT interface

Description

The EMIF01-TV01F3 is a highly integrated array designed to suppress EMI/RFI noise and provide impedance matching for mobile phone and portable applications. The EMIF01-TV01F3 is in a Flip Chip package to offer space saving and high RF performance.

This low pass filter includes ESD protection circuitry which prevents damage to the protected device when subjected to ESD surges up to 15 kV.

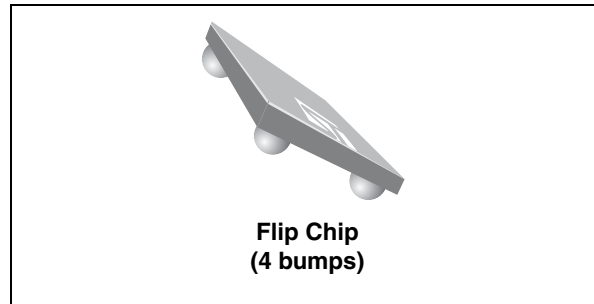


Figure 1. Pin configuration (bump side)

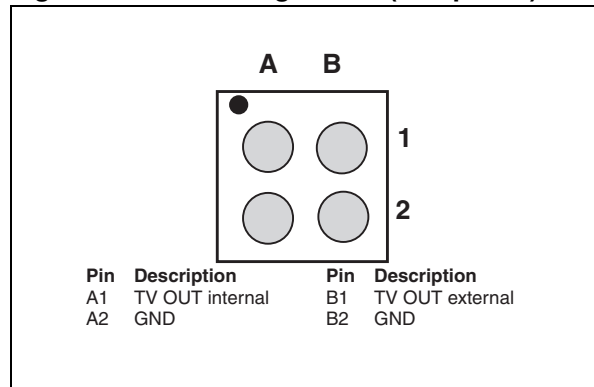
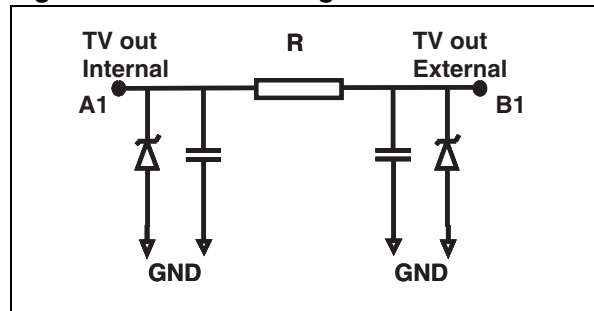


Figure 2. Device configuration



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1 Characteristics

Table 1. Absolute maximum ratings

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	Internal pins (A1) and external pin (B1): ESD discharge IEC 61000-4-2, air discharge	15	kV
	ESD discharge IEC 61000-4-2, contact discharge	8	
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-30 to +85	°C
P	Maximum power dissipation	80	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 2. Electrical characteristics ($T_{amb} = 25\text{ °C}$)

Symbol	Parameters				
V_{BR}	Breakdown voltage				
I_{RM}	Leakage current @ V_{RM}				
V_{RM}	Stand-off voltage				
V_{CL}	Clamping voltage				
R_d	Dynamic impedance				
I_{PP}	Peak pulse current				
$R_{I/O}$	Series resistance between Input & Output				
C_{line}	Input capacitance per line				
Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	$I_R = 1\text{ mA}$	6		8	V
I_{RM}	$V_{RM} = 3\text{ V}$			0.2	μA
R	Tolerance $\pm 5\%$		75		Ω
C_{line}	@ 0 V		30	35	pF

Figure 3. S21 (db) attenuation measurement **Figure 4. ESD response to IEC61000-4-2 (+15 kV air discharge)**

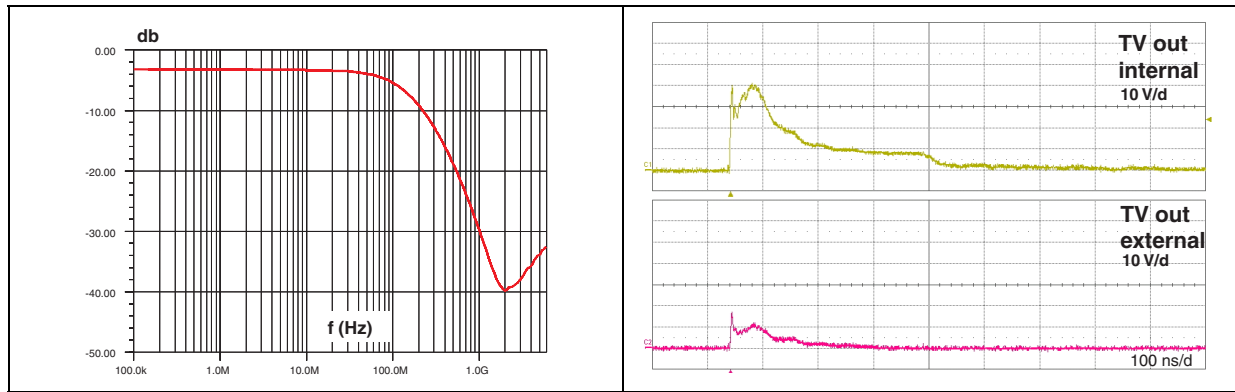
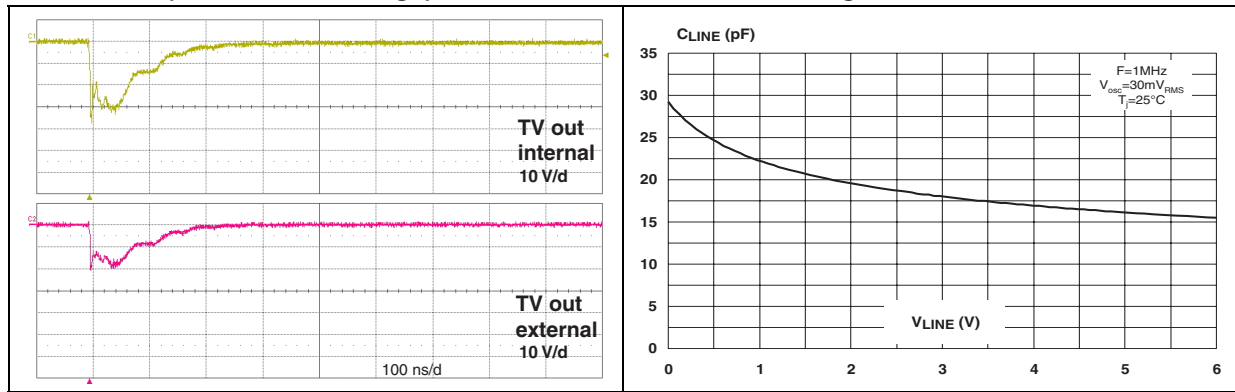


Figure 5. ESD response to IEC61000-4-2 (-15 kV air discharge) **Figure 6. Line capacitance versus applied voltage**



2 Application information

Figure 7. Aplac model

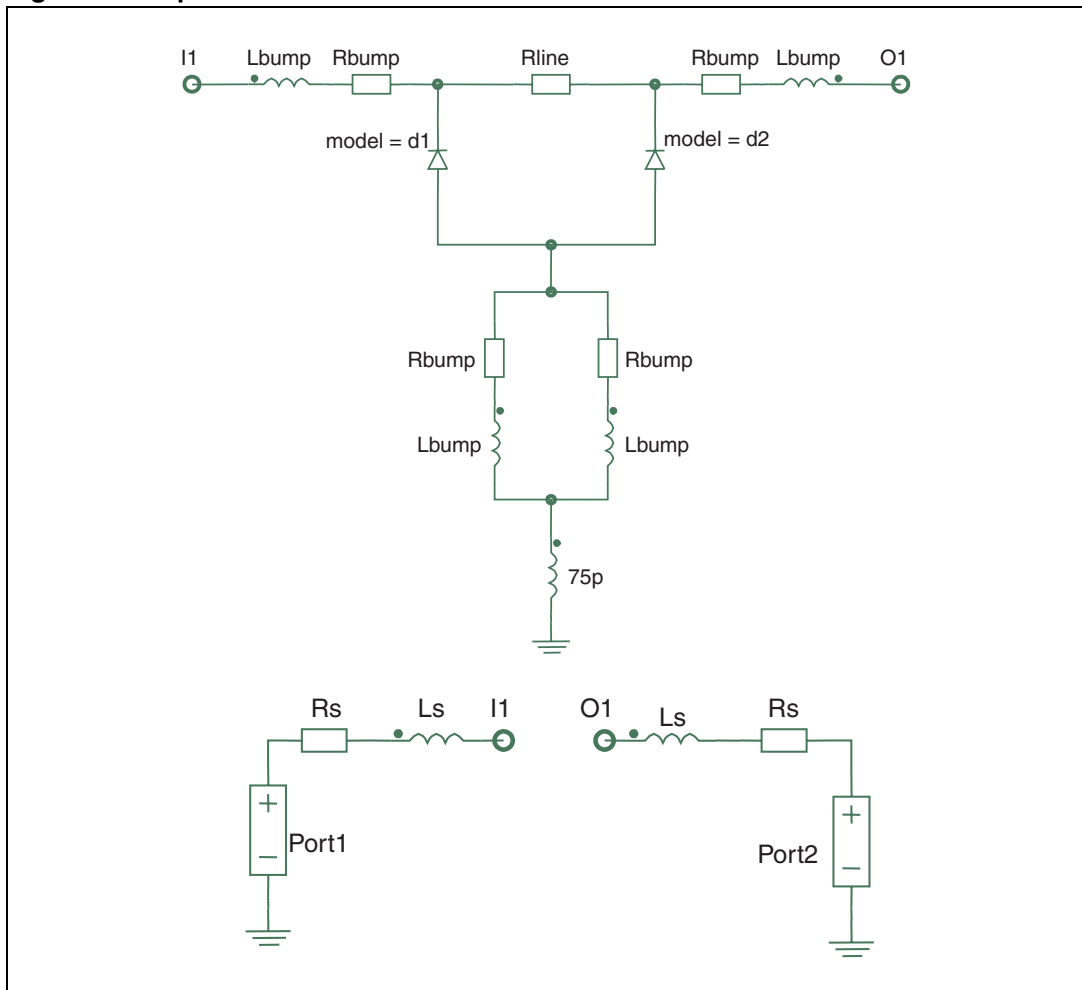
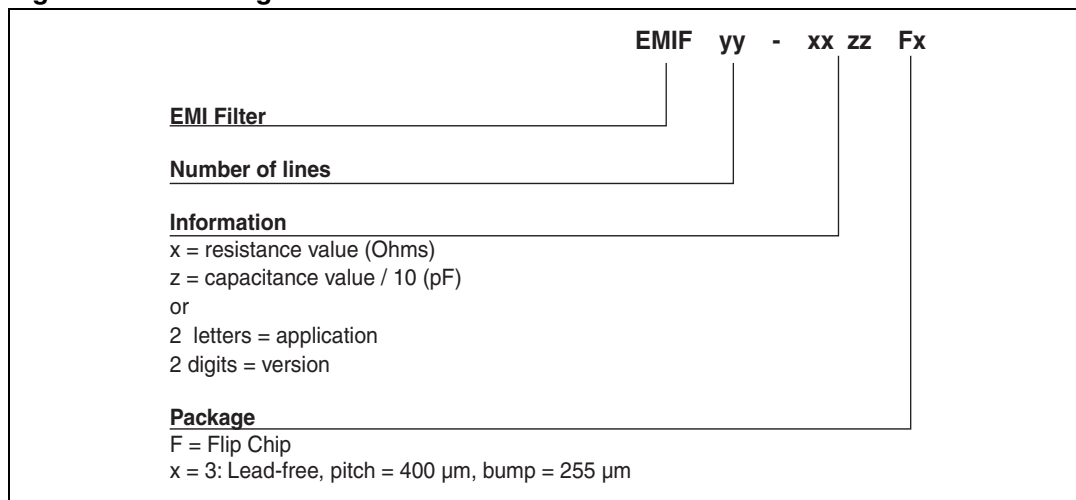


Figure 8. Aplac parameters

Variables		Diode D1	Diode D2
aplacvar Rline 75		BV=7	BV=7
aplacvar C_d1 17.5p		IBV=1m	IBV=1m
aplacvar C_d2 17.5p		CJO=C_d1	CJO=C_d2
aplacvar Ls 950pH		M=0.28	M=0.28
aplacvar Rs 150m		RS=0.48	RS=0.7
aplacvar Lbump96pH		VJ=0.6	VJ=0.6
aplacvar Rbump 20m		TT=100n	TT=100n
aplacvar Lgnd 75pH			

3 Ordering information scheme

Figure 9. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 10. Package dimensions

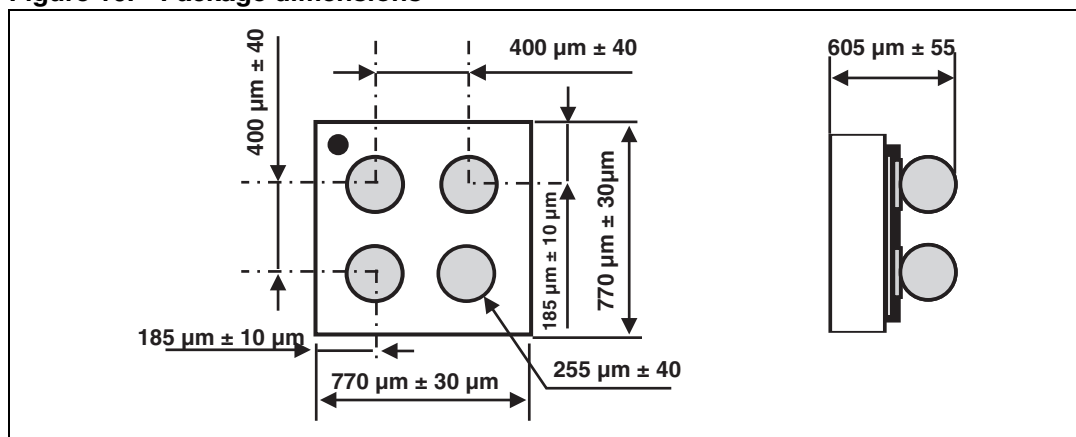


Figure 11. Footprint

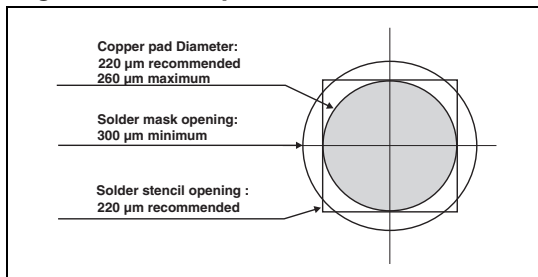


Figure 12. Marking

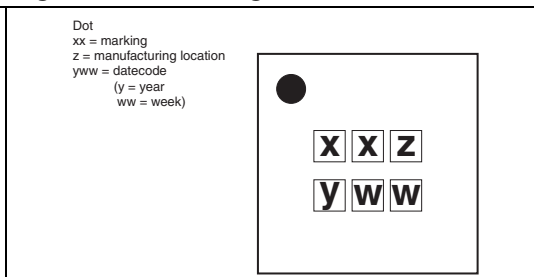
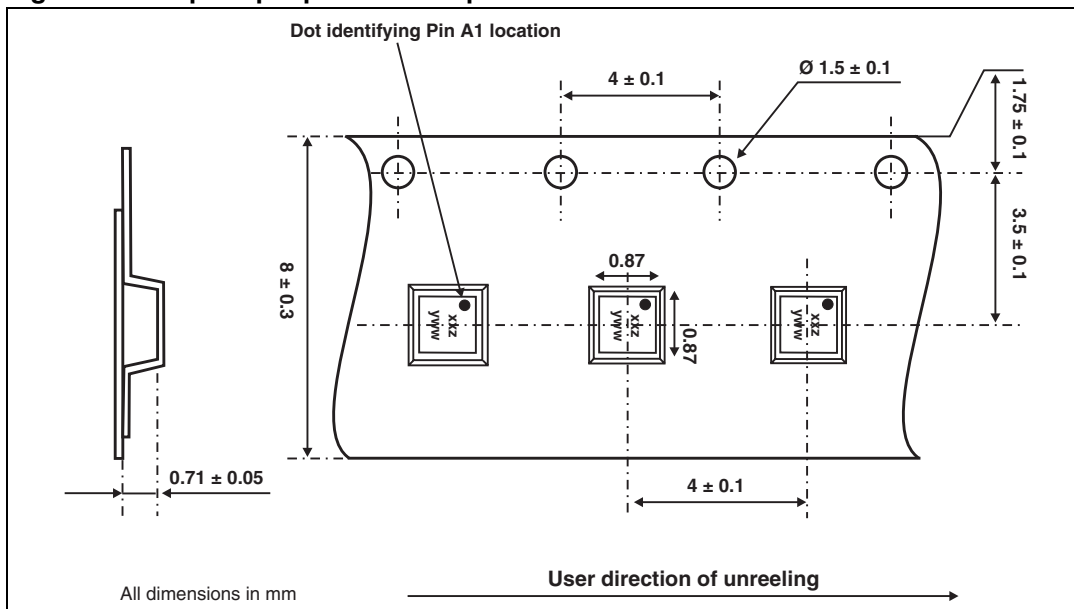


Figure 13. Flip Chip tape and reel specification



Note:

More information is available in the application notes:

AN2348: “STMicroelectronics 400 micro-metre Flip Chip: Package description and recommendation for use”

AN1751: “EMI filters: Recommendations and measurements”

5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF01-TV01F3	HC	Flip Chip	0.79 mg	5000	Tape and reel 7”

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
09-Feb-2006	1	Initial release.
28-Apr-2008	2	Updated ECOPACK statement. Updated Figure 9 , Figure 10 , and Figure 13 . Reformatted to current standards.
26-May-2011	3	Updated figure in Table 2 . Updated ECOPACK statement.

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