IXYS RF

N-Channel Enhancement Mode
Low Q_g and R_g
High dv/dt
Nanosecond Switching

V_{DSS}	=	500 V
I_{D25}	=	4.5 A
$R_{DS(on)}$	≤	1.5 Ω
P_{DC}	=	200W

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	500	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_c = 25°C	4.5	A
I_{DM}	T_c = 25°C, pulse width limited by T_{JM}	27	A
I_{AR}	T_c = 25°C	4.5	A
E_{AR}	T_c = 25°C	-	mJ
dv/dt	$I_S \le I_{DM}$, di/dt $\le$ 100A/µs, $V_{DD} \le V_{DSS}$, $T_j \le$ 150°C, R_G = 0.2Ω	3.5	V/ns
	I_S = 0	>200	V/ns
P_{DC}		200	W
P_{DHS}	T_c = 25°C Derate 4.4W/°C above 25°C	80	W
P_{DAMB}	T_c = 25°C	3.5	W
R_{thJC}		0.74	C/W
R_{thJHS}		1.50	C/W

Symbol	Test Conditions	Characteristic Values T_J = 25°C unless otherwise specified			
		min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 3 ma	500			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µa	2.5	3.4	4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	V_{DS} = 0.8 V_{DSS} T_J = 25°C V_{GS} = 0 T_J = 125°C			25 250	µA µA
$R_{DS(on)}$	V_{GS} = 15 V, I_D = 0.5I_{D25} Pulse test, t $\le$ 300µS, duty cycle d $\le$ 2%		1.2	1.5	Ω
g_{fs}	V_{DS} = 60 V, I_D = 0.5I_{D25}, pulse test		1.9		S
T_J		-55		+175	°C
T_{JM}			175		°C
T_{stg}		-55		+175	°C
T_L	1.6mm (0.063 in) from case for 10 s		300		°C
Weight			2		g

GATE — DRAIN
SG1 SG2 SD1 SD2

Features

- Isolated Substrate
- high isolation voltage (>2500V)
- excellent thermal transfer
- Increased temperature and power cycling capability
- IXYS advanced low Q_g process
- Low gate charge and capacitances
- easier to drive
- faster switching
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

Advantages

- Optimized for RF and high speed switching at frequencies to >100MHz
- Easy to mount—no insulators needed
- High power density

Symbol	Test Conditions	Characteristic Values			
(T$_J$ = 25°C unless otherwise specified)		**min.**	**typ.**	**max.**	
R$_G$				5	Ω
C$_{iss}$	V$_{GS}$ = 0 V, V$_{DS}$ = 0.8 V$_{DSS(max)}$, f = 1 MHz		570		pF
C$_{oss}$			75		pF
C$_{rss}$			3		pF
C$_{stray}$	Back Metal to any Pin		16		pF
T$_{d(on)}$	V$_{GS}$ = 15 V, V$_{DS}$ = 0.8 V$_{DSS}$ I$_D$ = 0.5 I$_{DM}$ R$_G$ = 0.2 Ω (External)		4		ns
T$_{on}$			4		ns
T$_{d(off)}$			4		ns
T$_{off}$			4		ns
Q$_{g(on)}$	V$_{GS}$ = 10 V, V$_{DS}$ = 0.5 V$_{DSS}$ I$_D$ = 0.5 I$_{D25}$, Ig = 3 ma		14		nC
Q$_{gs}$			3.5		nC
Q$_{gd}$			5.5		nC

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T$_J$ = 25°C unless otherwise specified)			
		min.	**typ.**	**max.**	
I$_S$	V$_{GS}$ = 0 V			4.5	A
I$_{SM}$	Repetitive; pulse width limited by T$_{JM}$			27	A
V$_{SD}$	I$_F$ = I$_S$, V$_{GS}$ = 0 V, Pulse test, t $\leq$ 300 μs, duty cycle $\leq$ 2%			1.4	V
T$_{rr}$			900		ns

CAUTION: Operation at or above the Maximum Ratings values may impact device reliability or cause permanent damage to the device.

Information in this document is believed to be accurate and reliable. IXYSRF reserves the right to make changes to information published in this document at any time and without notice.

For detailed device mounting and installation instructions, see the "*Device Installation & Mounting Instructions*" technical note on the IXYSRF web site at;

http://www.ixysrf.com/pdf/switch_mode/appnotes/7de_series_mosfet_installation_instructions.pdf

Fig. 1

Typical Transfer Characteristics
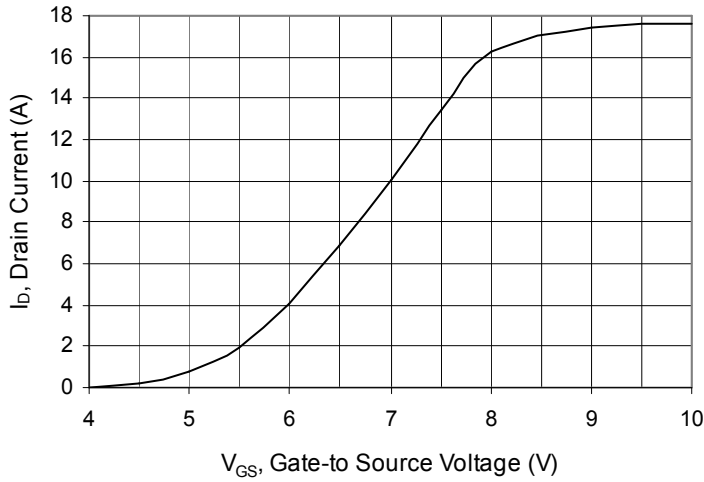$V_{DS} = 60V$, PW = 20µS
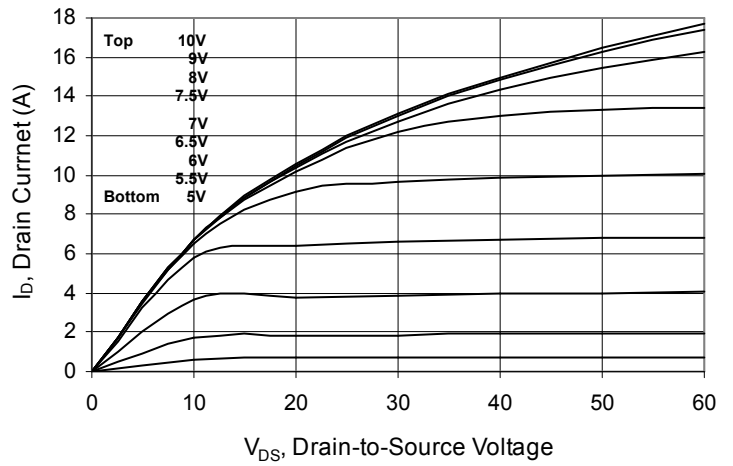

Fig. 2

Typical Output Characteristics

Fig. 3

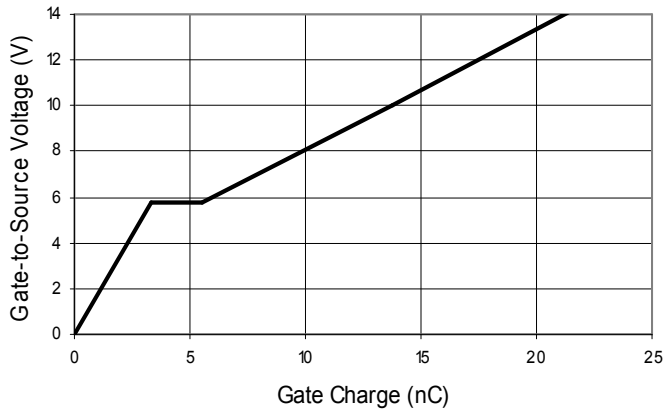**Gate Charge vs. Gate-to-Source Voltage**
$V_{DS} = 250V$, $I_D = 2.25A$

Fig. 4

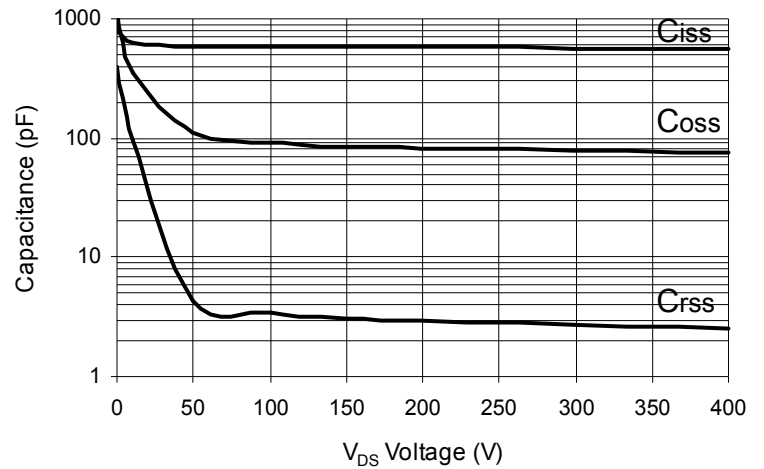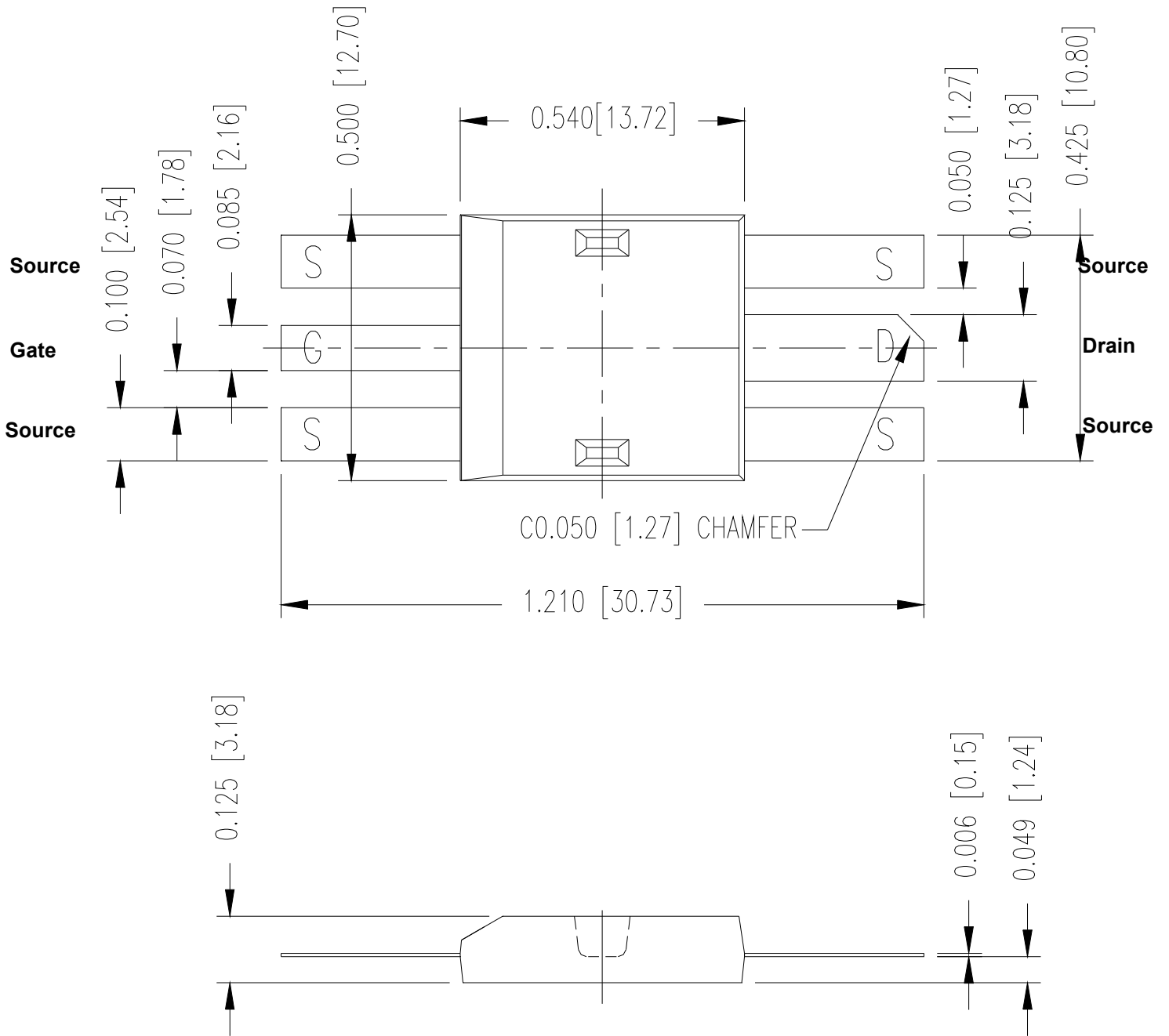**V_{DS} Voltage vs. Capacitance**

Fig. 5 Package drawing

501N04A DE-SERIES SPICE Model

The DE-SERIES SPICE Model is illustrated in Figure 6. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms L_G, L_S and L_D. Rd is the $R_{DS(ON)}$ of the device, Rds is the resistive leakage term. The output capacitance, C_{OSS}, and reverse transfer capacitance, C_{RSS} are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via Ron and Roff.
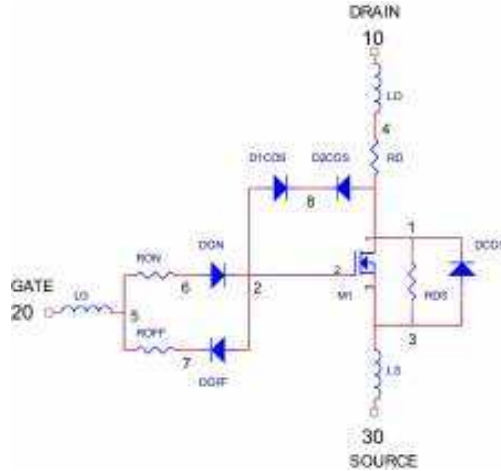

Figure 6 DE-SERIES SPICE Model

This SPICE model may be downloaded as a text file from the IXYSRF web site at

http://www.ixysrf.com/products/switch_mode.html

http://www.ixysrf.com/spice/de150-501n04a.html

Net List:
*SYM=POWMOSN
.SUBCKT 501N04A 10 20 30
*   TERMINALS: D G S
* 500 Volt 4.5 Amp 1.5 Ohm N-Channel Power MOSFET 10-30-2001
M1 1 2 3 3 DMOS L=1U W=1U
RON 5 6 9.5
DON 6 2 D1
ROF 5 7 3.5
DOF 2 7 D1
D1CRS 2 8 D2
D2CRS 1 8 D2
CGS 2 3 .6N
RD   4 1 1.5
DCOS 3 1 D3
RDS 1 3 5.0MEG
LS 3 30 .1N
LD 10 4 1N
LG 20 5 1N
.MODEL DMOS NMOS (LEVEL=3 VTO=3.0 KP=6.0)
.MODEL D1 D (IS=.5F CJO=1P BV=100 M=.5 VJ=.6 TT=1N)
.MODEL D2 D (IS=.5F CJO=175P BV=500 M=.5 VJ=.6 TT=1N RS=10M)
.MODEL D3 D (IS=.5F CJO=250P BV=500 M=.3 VJ=.4 TT=400N RS=10M)
.ENDS