20 Ampere Ultrafast RF MOSFET Driver With Kelvin Connection

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected
- High Peak Output Current: 20A Peak
- Wide Operating Range: 8V to 30V
- Rise and Fall Times of <4ns
- Minimum Pulse Width of 8ns
- High Capacitive Load Drive Capability: 4nF in <4ns
- Matched Rise and Fall Times
- 32ns Input to Output Delay Time
- Low Output Impedance
- Low Quiescent Supply Current
- Kelvin input ground connection
- Reduced internal inductance

Applications

- Driving RF MOSFETs
- Class D or E Switching Amplifier Drivers
- Multi-MHz Switch Mode Power Supplies (SMPS)
- Pulse Generators
- Acoustic Transducer Drivers
- Pulsed Laser Diode Drivers
- Pulse Transformer Driver

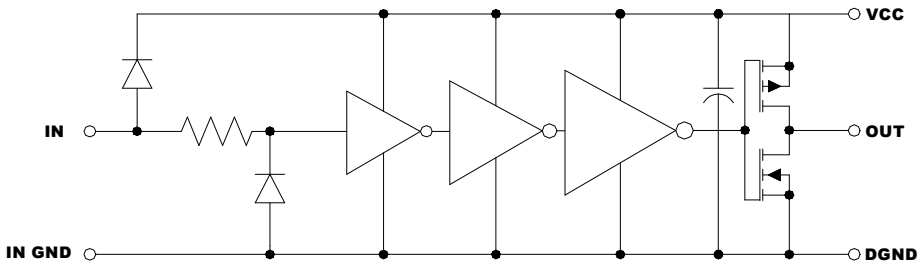
Description

The DEIC421 is a CMOS high speed high current gate driver specifically designed to drive MOSFETs in Class D, E, and RF applications at up to 45MHz, as well as other applications requiring ultrafast rise and fall times or short minimum pulse widths. The DEIC421 is an improved version of the DEIC420. The DEIC421 has a Kelvin ground connection on the input side to allow the use of a common mode choke to avoid problems with ground bounce. The internal layout of the package has been improved to reduce inductance. The DEIC421 can source and sink 20A of peak current while producing voltage rise and fall times of less than 4ns, and minimum pulse widths of 8ns. The input of the driver is compatible with +5V or CMOS and is fully immune to latch up over the entire operating range. Its features and wide safety margin in operating voltage and power make the DEIC421 unmatched in performance and value.

The DEIC421 is packaged in DEI's new 7 leaded low inductance RF package. The DEIC421 is a surface-mount device, and incorporates patented[1] RF layout techniques to minimize stray lead inductances for optimum switching performance.

[1] DEI U.S. Patent #4,891,686

Figure 1 - DEIC421 Functional Diagram



Absolute Maximum Ratings

Parameter	Value
Supply Voltage	30V
Input Pin	-5V to V_{CC}+0.3V
All Other Pins	-0.3V to V_{CC}+0.3V
Power Dissipation	
$T_{AMBIENT}$ ≤ 25°C	2W
T_{CASE} ≤ 25°C	100W

Parameter	Value
Storage Temperature	65°C to 150°C
Soldering Lead Temperature (10 seconds maximum)	300°C
Maximum Junction Temperature	150°C
Operating Temperature Range	-40°C to 85°C
Thermal Impedance $Rth_{(JC)}$ (Junction to Case)	1.3°C/W

Electrical Characteristics

Unless otherwise noted, T_A = 25 °C, 8V ≤ V_{CC} ≤ 30V.
All voltage measurements with respect to DGND. DEIC421 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage		3.5			V
V_{IL}	Low input voltage				0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	mA
V_{OH}	High output voltage		V_{CC} - .025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ output high	I_{OUT} = 10mA, V_{CC} = 15V		0.4	0.6	Ω
R_{OL}	Output resistance @ output low	I_{OUT} = 10mA, V_{CC} = 15V		0.4	0.6	Ω
I_{PEAK}	Peak output current	V_{CC} = 15V		20		A
I_{DC}	Continuous output current				4	A
f_{MAX}	Maximum frequency	C_L = 4nF, V_{CC} = 15V			45	MHz
t_R	Rise time(1)	C_L = 1nF, V_{CC} = 15V, V_{OH} = 2V to 12V C_L = 4nF, V_{CC} = 15V, V_{OH} = 2V to 12V		3 4		ns ns
t_F	Fall time(1)	C_L = 1nF, V_{CC} = 15V, V_{OH} = 12V to 2V C_L = 4nF, V_{CC} = 15V, V_{OH} = 12V to 2V		3 3.5		ns ns
t_{ONDLY}	On-time propagation delay(1)	C_L = 4nF, V_{CC} = 15V		32	38	ns
t_{OFFDLY}	Off-time propagation delay(1)	C_L = 4nF, V_{CC} = 15V		29	35	ns
P_{Wmin}	Minimum pulse width	FWHM, C_L = 1nF, V_{CC} = 15V +3V to +3V, C_L = 1nF, V_{CC} = 15V		8 9		ns ns
V_{CC}	Power supply voltage		8	15	30	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = +V_{CC}		1 0	3 10 10	mA µA µA

(1)Refer to Figures 2 and 3

Lead Description

SYMBOL	FUNCTION	DESCRIPTION
VCC	Supply Voltage	Positive power-supply voltage input. These leads provide power to the entire chip. The range for this voltage is 8V to 30V.
IN	Input	Input signal. TTL and CMOS compatible. 5V to 8V optimum.
IN GND	Input Ground	Input ground Kelvin connection.
OUT	Output	Driver output. For application purposes, this lead is connected directly to the gate of a MOSFET.
GND	Power Ground	Power grounds should be connected to a low noise analog ground plane for optimum performance.

Note: Operating the device beyond parameters with listed "absolute maximum ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Figure 2 - Characteristics Test Diagram

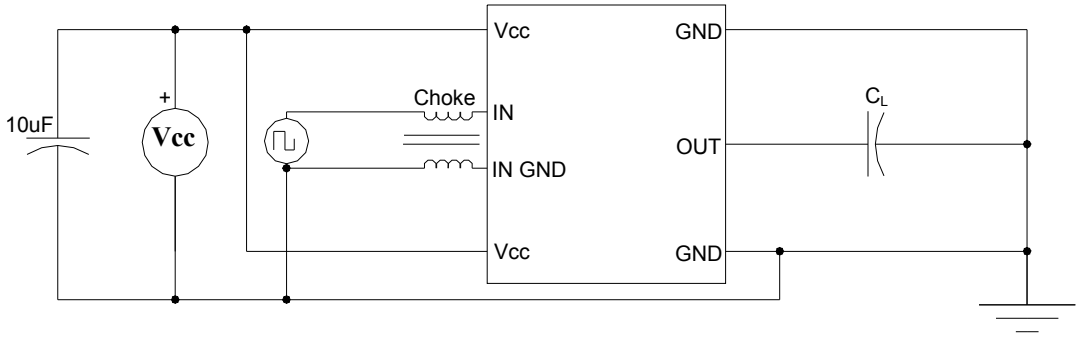
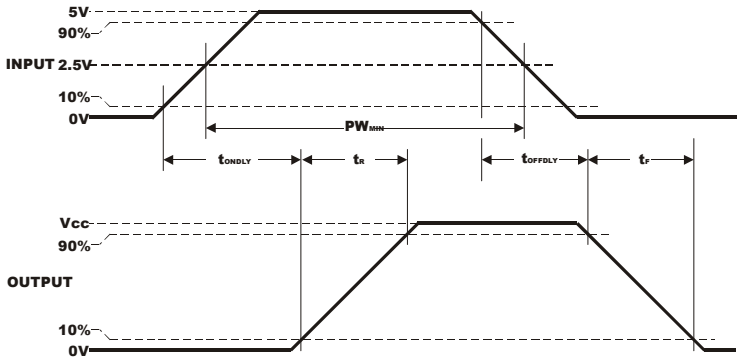


Figure 3 - Timing Diagram



Typical Performance Characteristics

Fig. 4 Rise Time vs. Load Capacitance
V_{CC} = 15V, V_{OH} = 2V To 12V

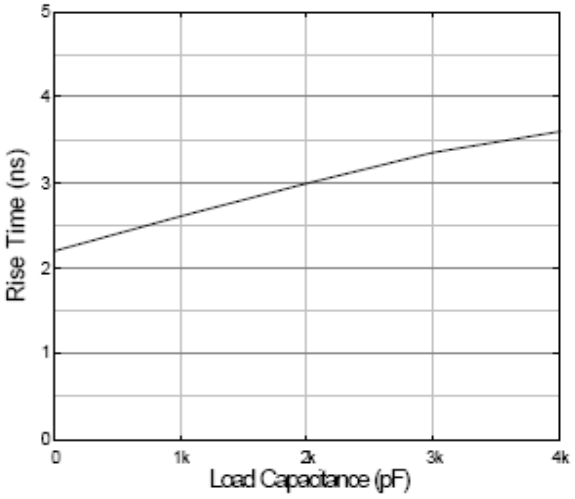


Fig. 5 Fall Time vs. Load Capacitance
V_{CC} = 15V, V_{OH} = 12V To 2V

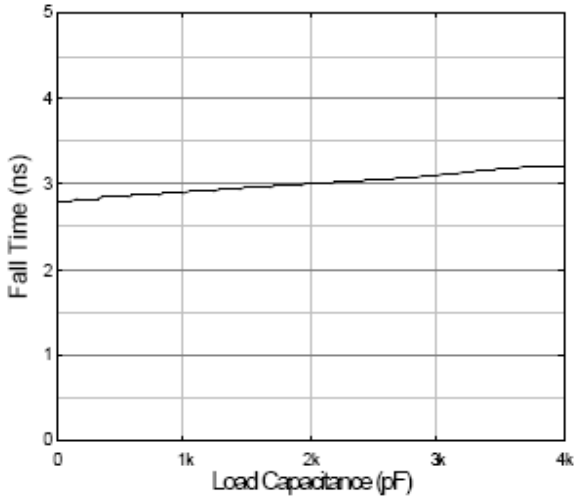


Fig. 6 Supply Current vs. Frequency
Vcc=15V

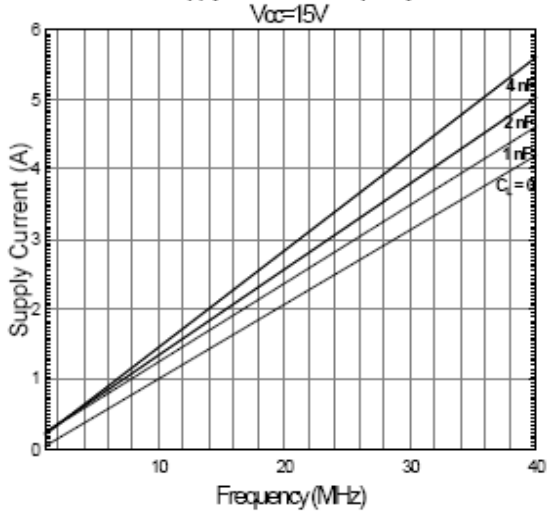


Fig. 7 Supply Current vs. Load Capacitance
Vcc=15V

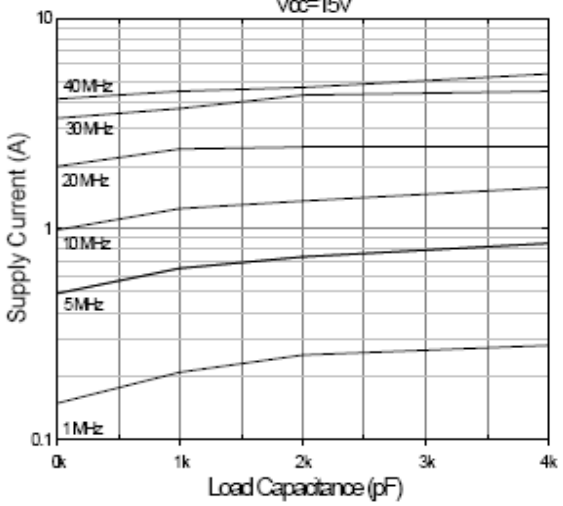


Fig. 8 Propagation Delay Times vs. Input Voltage
C_L=4nF V_{CC}=15V

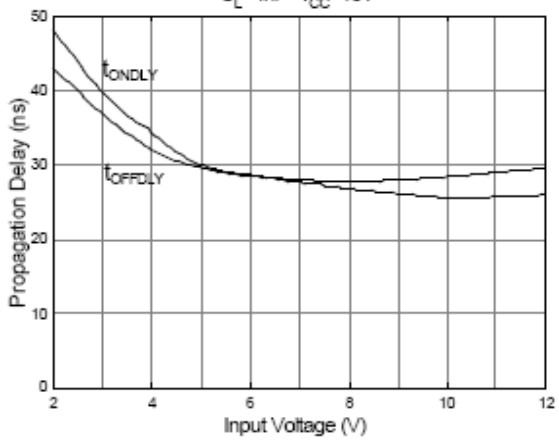


Fig. 9 Propagation Delay Times vs. Junction Temperature
C_L = 4nF, V_{CC} = 15V

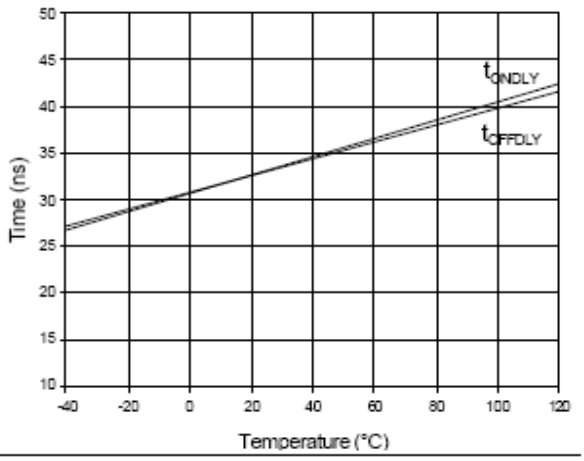


Fig. 10 Propagation Delay vs. Supply Voltage
C_L=4nF V_{IN}=5V@100kHz

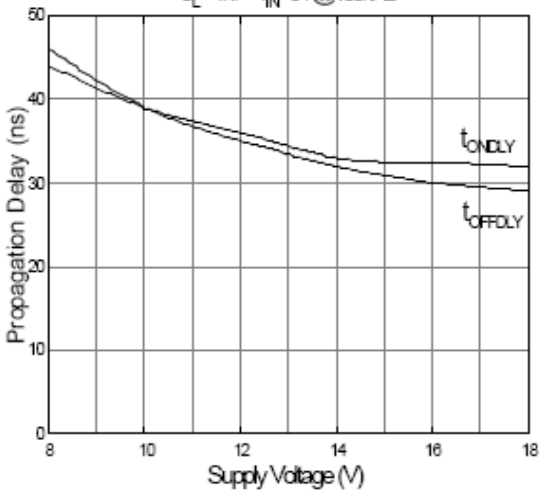
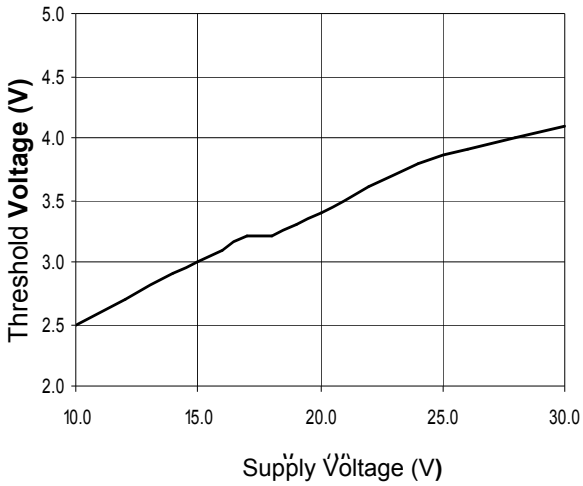


Fig. 11 Threshold vs. Supply Voltage



Typical Output Waveforms

Unless otherwise noted, all waveforms are taken driving a 1nF load, 1 MHz repetition frequency, V_{CC} = 15V, case temperature = 25°C

Fig. 12 3ns Rise Time

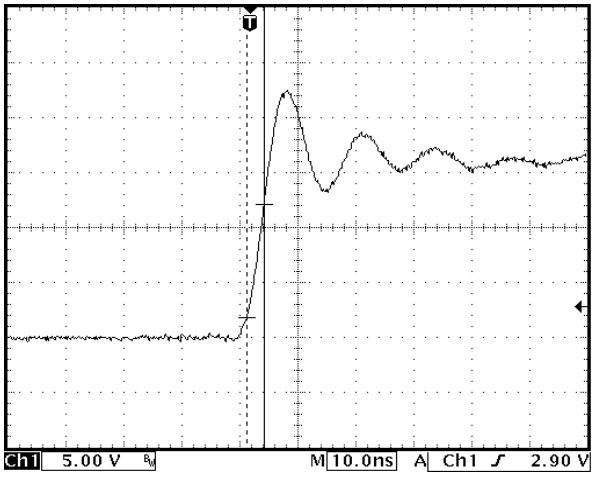


Fig. 13 3ns Fall Time

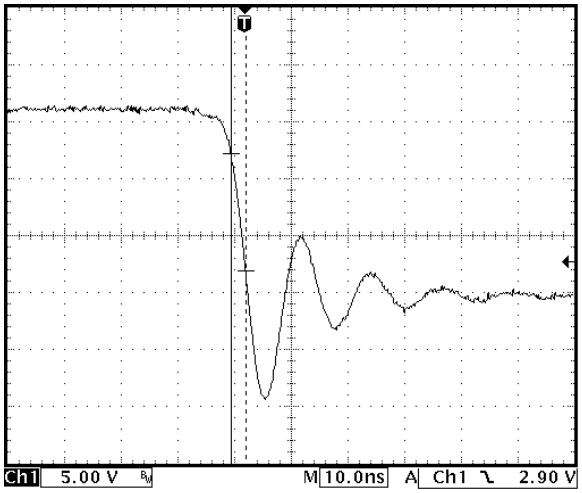


Fig. 14 <8ns Minimum Pulse Width

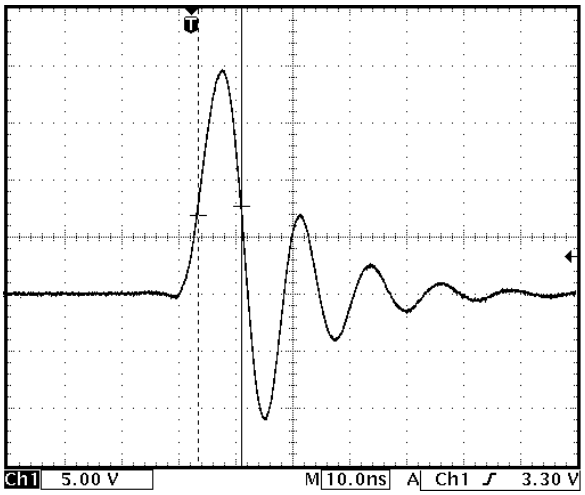


Fig. 15 1MHz CW Repetition Frequency

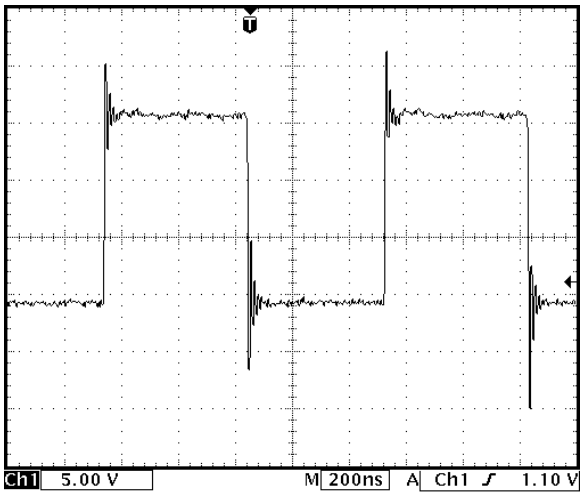


Fig. 16 13.56MHz CW Repetition Frequency

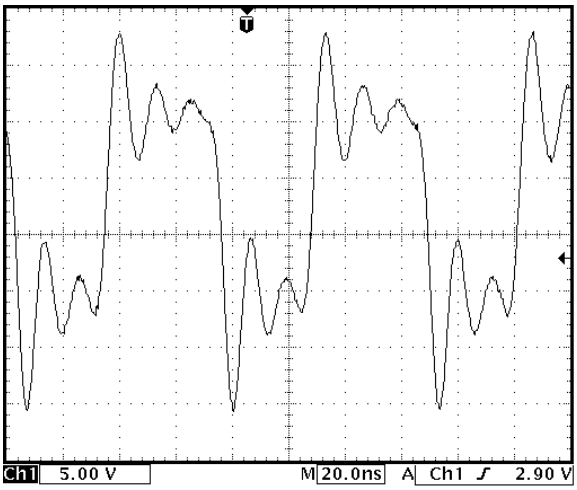
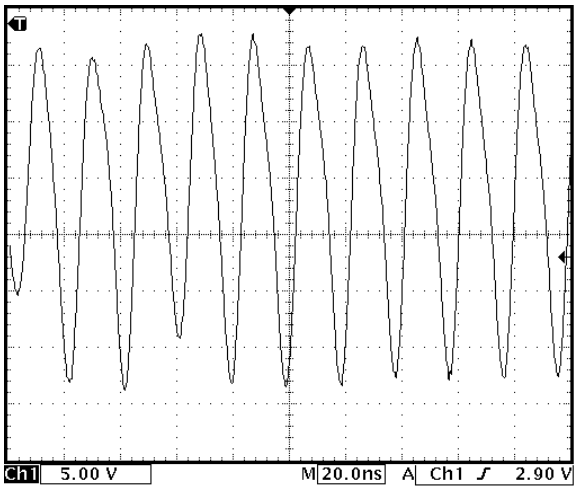


Fig. 17 50MHz Burst Repetition Frequency



Applications Information

Introduction
Circuits capable of very high switching speeds and high frequency operation require close attention to several important issues. Key elements include circuit loop inductance, Vcc bypassing, and grounding.

Circuit Loop Inductance
The Vcc to Vcc Ground current path defines the loop which will generate the inductive term. This loop must be kept as short as possible. The output lead must be no further than 0.375 inches (9.5mm) from the gate of the MOSFET. Furthermore, the output ground leads must provide a balanced symmetric coplanar ground return for optimum operation.

Vcc Bypassing
In order to turn a MOSFET on properly, the DEIC421 must be able to draw up to 20A of current from the Vcc power supply in 2-6ns (depending upon the input capacitance of the MOSFET being driven). Good performance requires very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value much larger than the load capacitance. Usually, this is achieved by placing two or three different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse-current-service capacitors.) Care should be taken to keep the lengths of the leads between these bypass capacitors and the DEIC421 to an absolute minimum.

The bypassing should be comprised of several values of chip capacitors symmetrically placed on either side of the IC. Recommended values are .01uF and .47uF chips and at least two 4.7uF tantalums.

Grounding
In order for the design to turn the load off properly, the DEIC421 must be able to drain this 20A of current into an adequate grounding system. There are two paths for returning current that need to be considered: Path #1 is between the DEIC421 and its load, and path #2 is between the DEIC421 and its power supply. Both of these paths should be as low in resistance and inductance as possible, and thus as short as practical.

The DEI421 has separate ground leads for input and power which allows the addition of a common mode choke in the input and input ground leads (see Fig. 2).

The common mode choke will provide a means of preventing ground bounce from affect the input to the driver. The selection of the common mode choke is related to the device being driven, the board layout, and the Vcc bypassing.

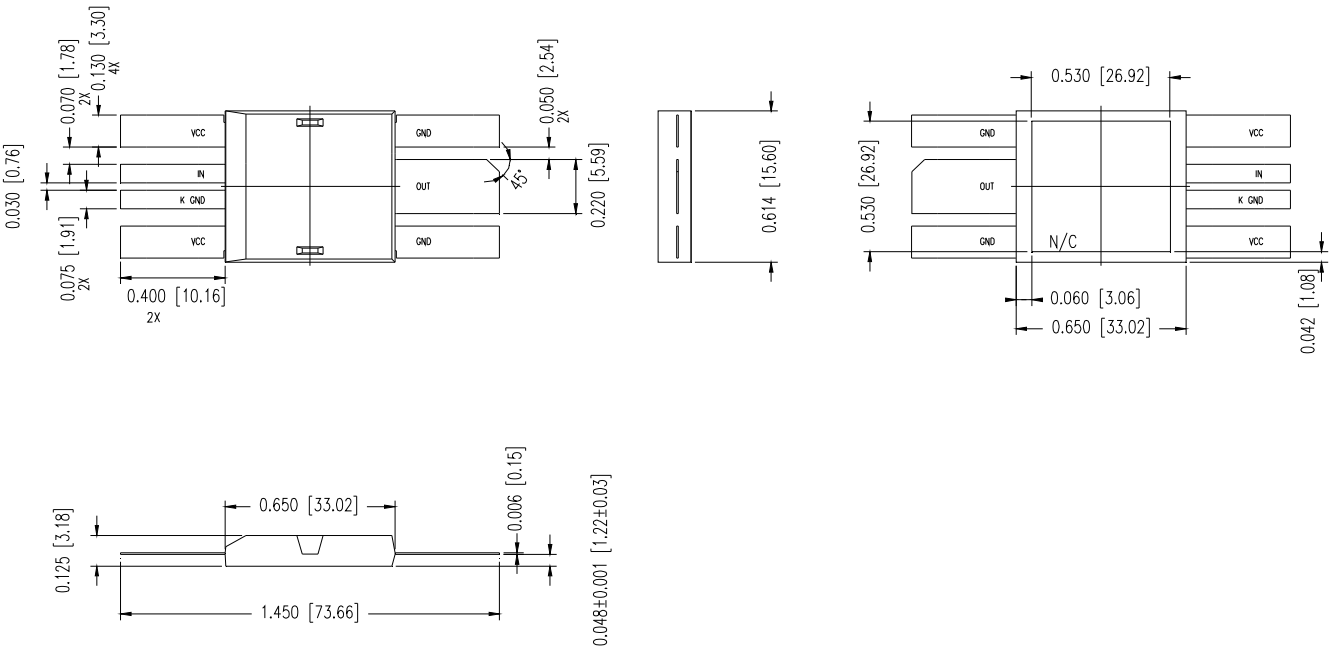
Output Lead Inductance
Of equal importance to supply bypassing and grounding are issues related to the output lead inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible, and treated as coplanar transmission lines.

In configurations where the optimum configuration of circuit layout and bypassing cannot be used, a series resistance of a few ohms in the gate lead may be necessary to prevent ringing.

Heat Sinking
For high power operation, the bottom side metalized substrate should be placed in compression against an appropriate heat sink. The substrate is metalized for improved heat dissipation, and is not electrically connected to the device or to ground.

See the DEI technical note “DE-Series MOSFET and IC Mounting Instructions” on the IXYSRF website at www.ixysrf.com for detailed mounting instructions.

Figure 18 - DEIC421 Package Outline



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