

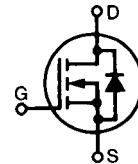
High Current MegaMOS™FET

IXTK 33N50

$V_{DSS} = 500 \text{ V}$
 $I_D(\text{cont}) = 33 \text{ A}$
 $R_{DS(on)} = 0.17 \Omega$

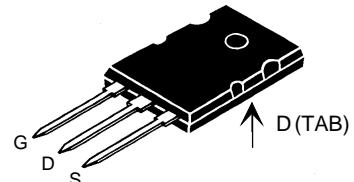
N-Channel Enhancement Mode

Preliminary data



Symbol	Test conditions	Maximum ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1.0 \text{ M}\Omega$	500	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_c = 25^\circ\text{C}$	33	A
I_{DM}	$T_c = 25^\circ\text{C}$, pulse width limited by T_{JM}	132	A
P_D	$T_c = 25^\circ\text{C}$	416	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		10	g
Max lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	$^\circ\text{C}$

TO-264 AA



G = Gate
S = Source

D = Drain
TAB = Drain

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 5 \text{ mA}$ BV_{DSS} temperature coefficient	500		V
			0.087	%/K
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$ $V_{GS(th)}$ temperature coefficient	2.0		4.0 V
			-0.25	%/K
I_{GSS}	$V_{GS} = \pm 20 \text{ V DC}$, $V_{DS} = 0$			$\pm 100 \text{ nA}$
I_{DSS}	$V_{DS} = 0.8 V_{DSS}$, $T_J = 25^\circ\text{C}$ $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$			200 μA 3 mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 I_{D25}$			0.17 Ω

Features

- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- International standard package
- Fast switching times

Applications

- Motor controls
- DC choppers
- Uninterruptable Power Supplies (UPS)
- Switch-mode and resonant-mode

Advantages

- Easy to mount with one screw (isolated mounting screw hole)
- Space savings
- High power density

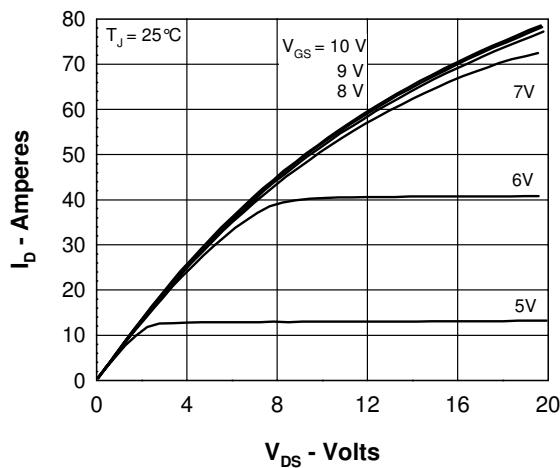
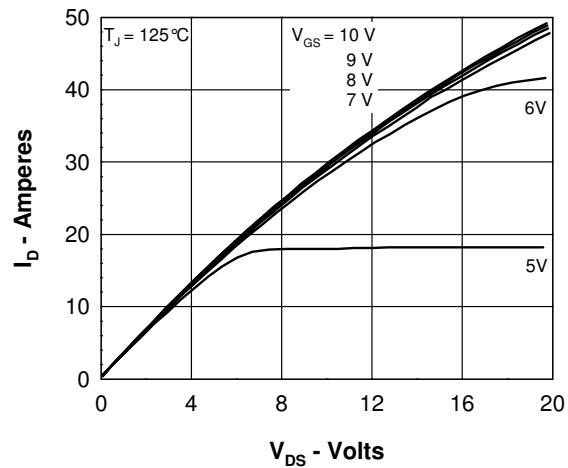
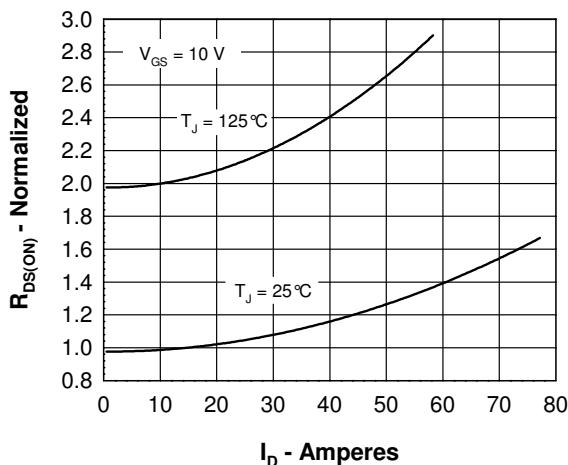
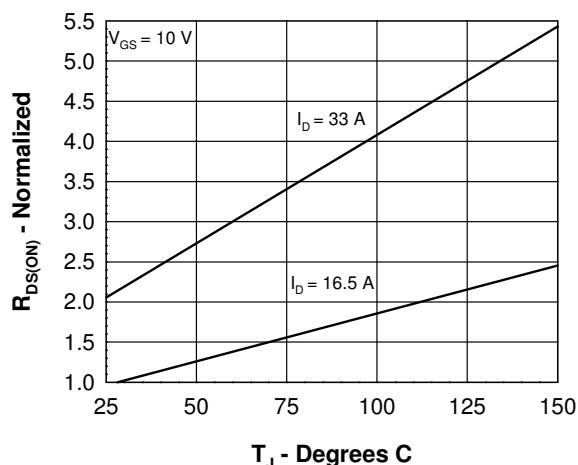
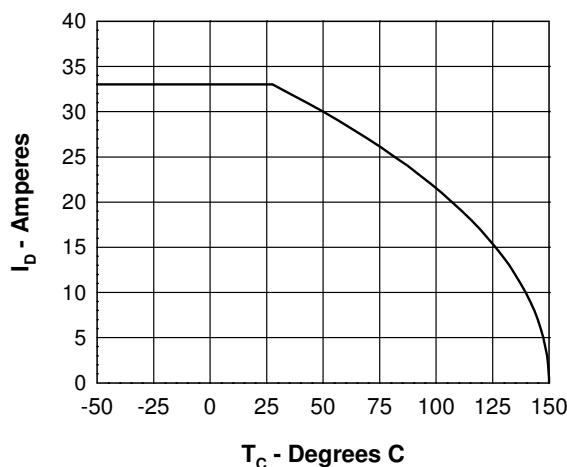
Figure 1. Output Characteristics at 25°C Figure 2. Output Characteristics at 125°C Figure 3. $R_{DS(on)}$ normalized to $16.5\text{A}/25^\circ\text{C}$ vs. I_D Figure 4. $R_{DS(on)}$ normalized to $16.5\text{A}/25^\circ\text{C}$ vs. T_J 

Figure 5. Drain Current vs. Case Temperature

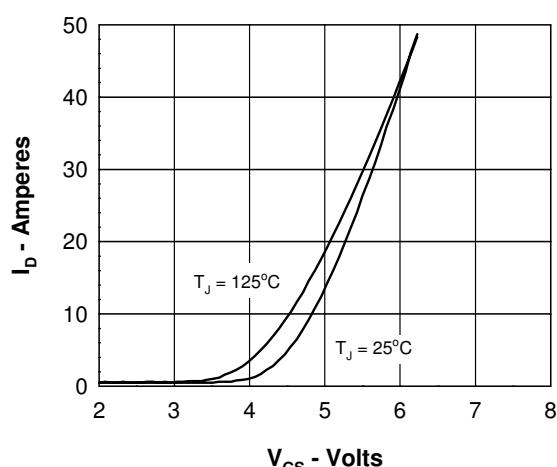


Figure 6. Admittance Curves

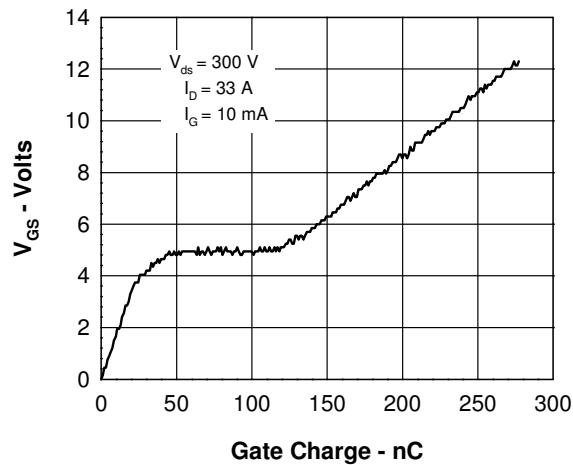


Figure 7. Gate Charge

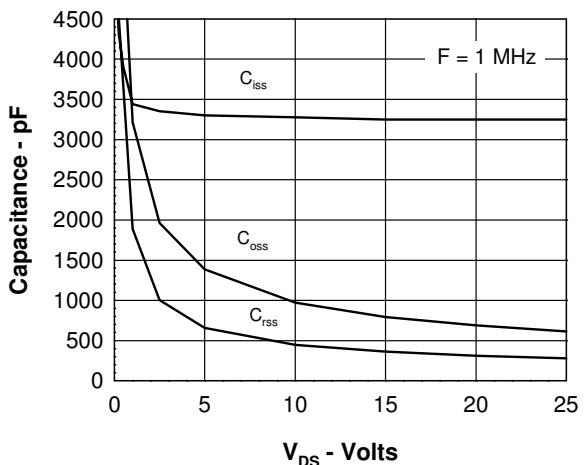


Figure 8. Capacitance Curves

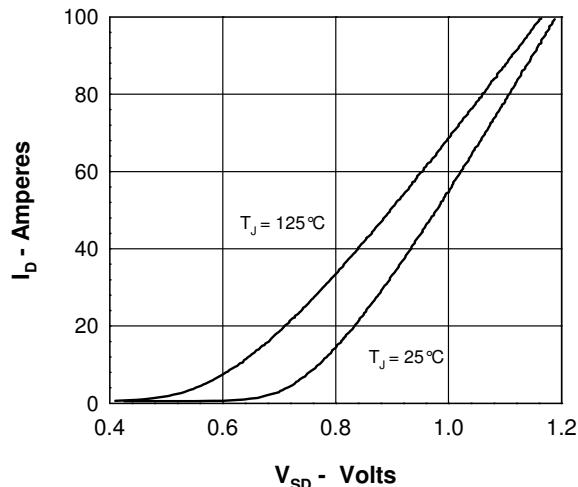


Figure 9. Source Current vs. Source-to-Drain Voltage

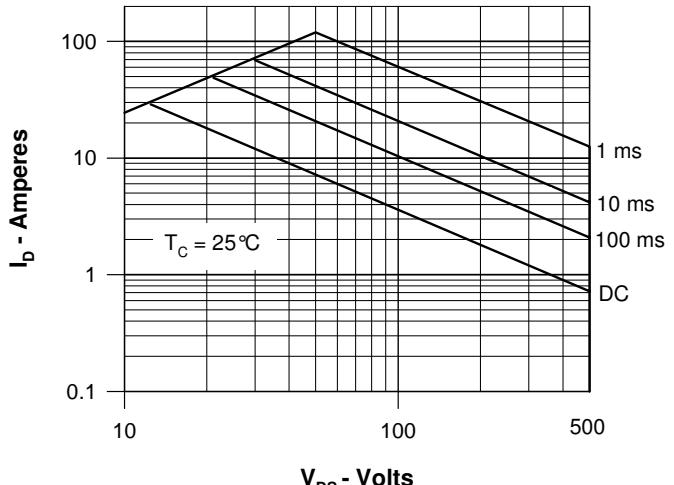


Figure 10. Forward Biased SOA

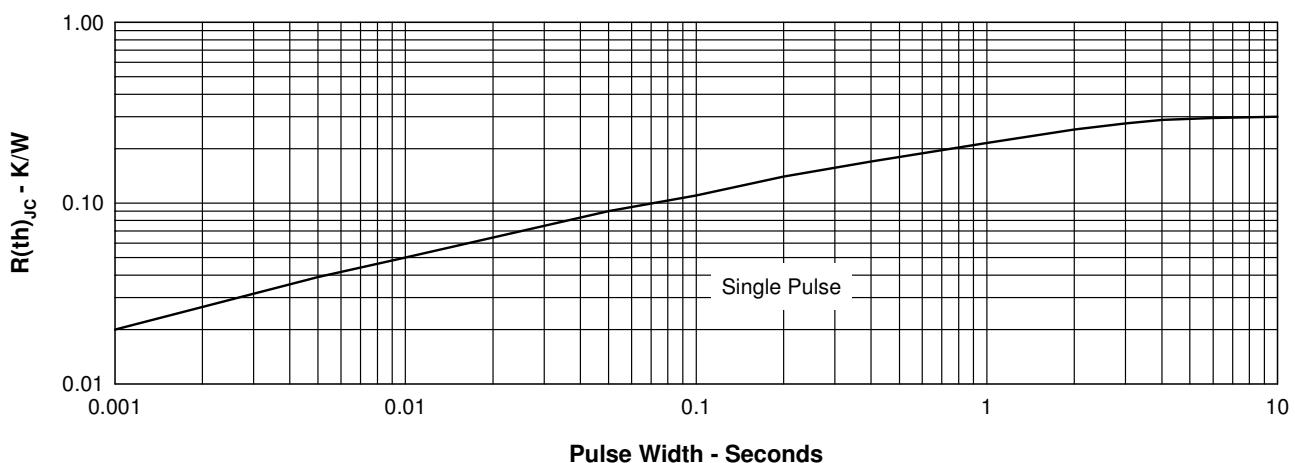


Figure 11. Transient Thermal Resistance