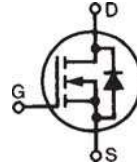


High Voltage Power MOSFET

IXTY01N100D
IXTU01N100D
IXTP01N100D

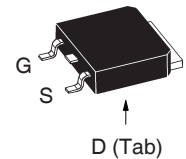
$V_{DSX} = 1000V$
 $R_{DS(on)} \leq 80\Omega$

N-Channel, Depletion Mode

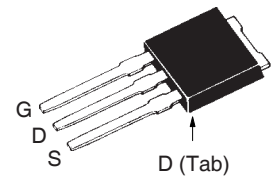


Symbol	Test Conditions	Maximum Ratings	
V_{DSX}	$T_J = 25^\circ\text{C}$ to 150°C	1000	V
V_{DGX}	$T_J = 25^\circ\text{C}$ to 150°C	1000	V
V_{GSX}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_J	400	mA
P_D	$T_C = 25^\circ\text{C}$	25	W
	$T_A = 25^\circ\text{C}$	1.1	W
T_J		- 55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		- 55 ... +150	$^\circ\text{C}$
T_L	1.6mm (0.062 in.) from Case for 10s	300	$^\circ\text{C}$
T_{SOLED}	Plastic Body for 10s	260	$^\circ\text{C}$
M_d	Mounting Torque (TO-220)	1.13 / 10	Nm/lb.in.
Weight	TO-252	0.35	g
	TO-251	0.40	g
	TO-220	3.00	g

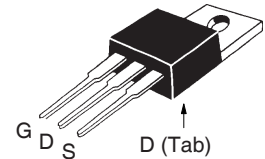
TO-252 (IXTY)



TO-251 (IXTU)



TO-220AB (IXTP)



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSX}	$V_{GS} = -10V$, $I_D = 25\mu\text{A}$	1000		V
$V_{GS(off)}$	$V_{DS} = 25V$, $I_D = 25\mu\text{A}$	- 2.0		- 4.5 V
I_{GSX}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 100 nA
$I_{DSX(off)}$	$V_{DS} = V_{DSX}$, $V_{GS} = -10V$ $T_J = 125^\circ\text{C}$			10 μA 250 μA
$R_{DS(on)}$	$V_{GS} = 0V$, $I_D = 50\text{mA}$, Note 1		50	80 Ω
$I_{D(on)}$	$V_{GS} = 0V$, $V_{DS} = 25V$, Note 1		400	mA

Features

- Normally ON Mode
- International Standard Packages
- Low $R_{DS(on)}$ HDMOS™ Process
- Rugged Polysilicon Gate Cell Structure
- Fast Switching Speed

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

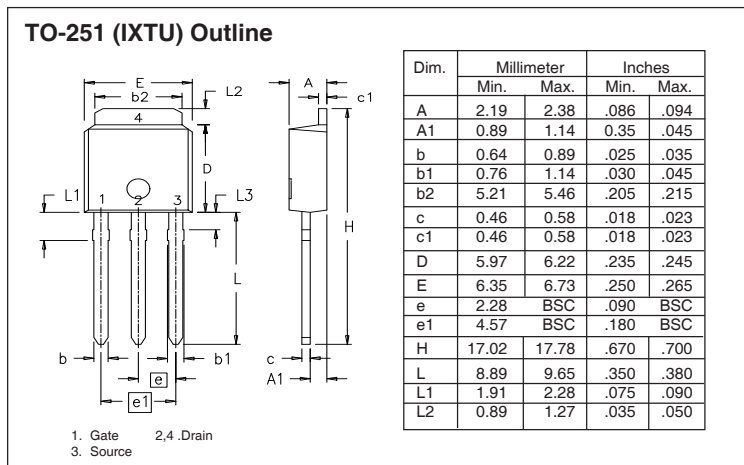
- Level Shifting
- Triggers
- Solid State Relays
- Current Regulators

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 100\text{V}$, $I_D = 100\text{mA}$, Note 1	100	200	mS
C_{iss}	$V_{GS} = -10\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		100	pF
C_{oss}			12	pF
C_{rss}			2	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = \pm 5\text{V}$, $V_{DS} = 50\text{V}$, $I_D = 50\text{mA}$ $R_G = 30\Omega$ (External)		7	ns
t_r			10	ns
$t_{d(off)}$			34	ns
t_f			64	ns
$Q_{g(on)}$	$V_{GS} = \pm 5\text{V}$, $V_{DS} = 500\text{V}$, $I_D = 50\text{mA}$		5.8	nC
Q_{gs}			3.6	nC
Q_{gd}			0.4	nC
R_{thJC}	TO-220			5.0 $^\circ\text{C/W}$
R_{thCS}			0.50	$^\circ\text{C/W}$

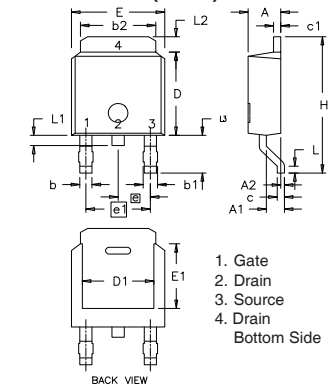
Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
V_{SD}	$I_F = 100\text{mA}$, $V_{GS} = -10\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 750\text{mA}$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 25\text{V}$, $V_{GS} = -10\text{V}$			1.5 μs

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

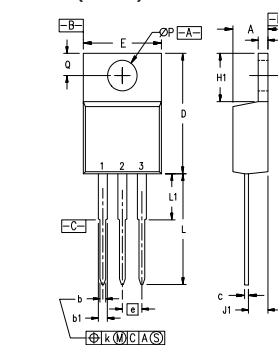


TO-252 AA (IXTY) Outline



Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
A2	0	0.13	0	0.005
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.32	5.21	0.170	0.205
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.170	0.205
e	2.28	BSC	0.090	BSC
e1	4.57	BSC	0.180	BSC
H	9.40	10.42	0.370	0.410
L	0.51	1.02	0.020	0.040
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	2.54	2.92	0.100	0.115

TO-220 (IXTP) Outline



Pins: 1 - Gate 2 - Drain
3 - Source 4 - Drain

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338 B2
by one or more of the following U.S. patents: 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

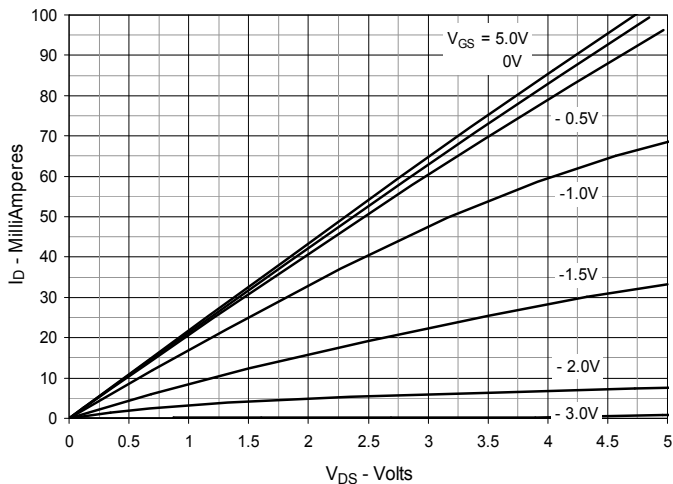


Fig. 2. Output Characteristics @ $T_J = 125^\circ\text{C}$

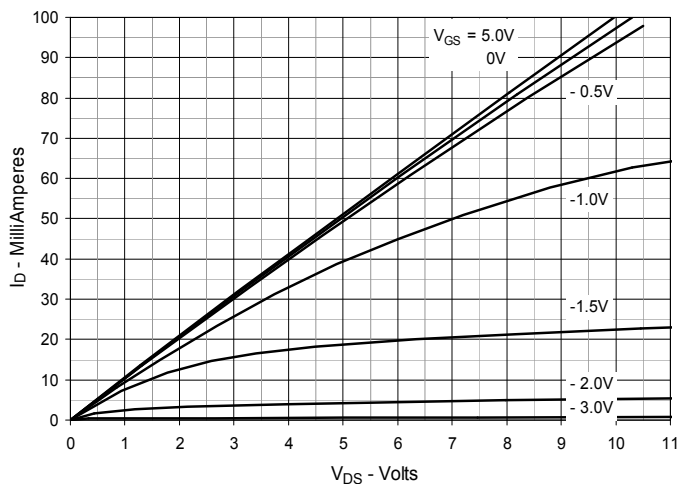


Fig. 3. Drain Current @ $T_J = 25^\circ\text{C}$

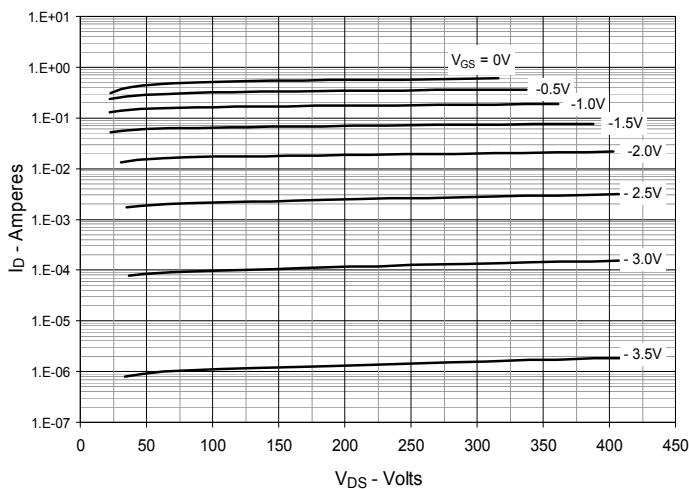


Fig. 4. Drain Current @ $T_J = 100^\circ\text{C}$

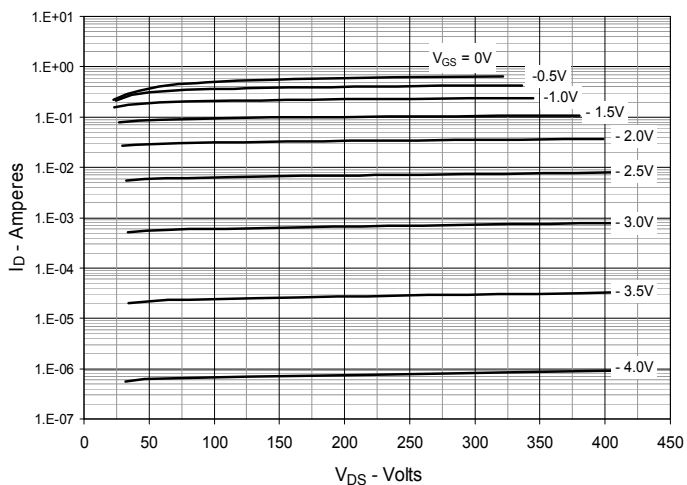


Fig. 5. Dynamic Resistance vs. Gate Voltage

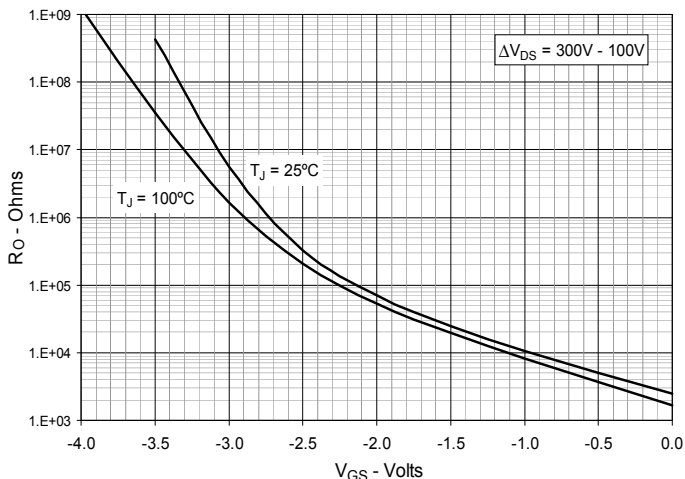


Fig. 6. Normalized $R_{DS(on)}$ vs. Junction Temperature

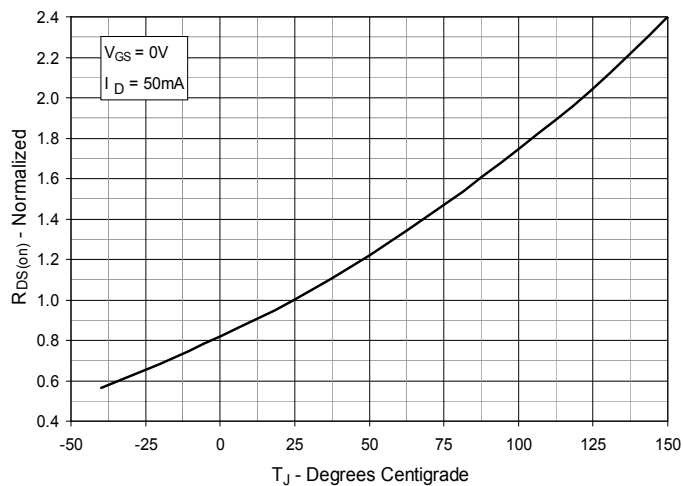


Fig. 7. $R_{DS(on)}$ Normalized to $I_D = 50mA$ Value vs. Drain Current

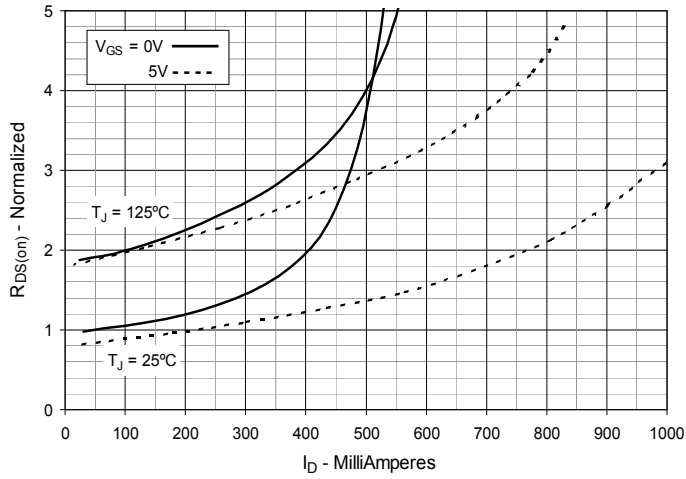


Fig. 8. Input Admittance

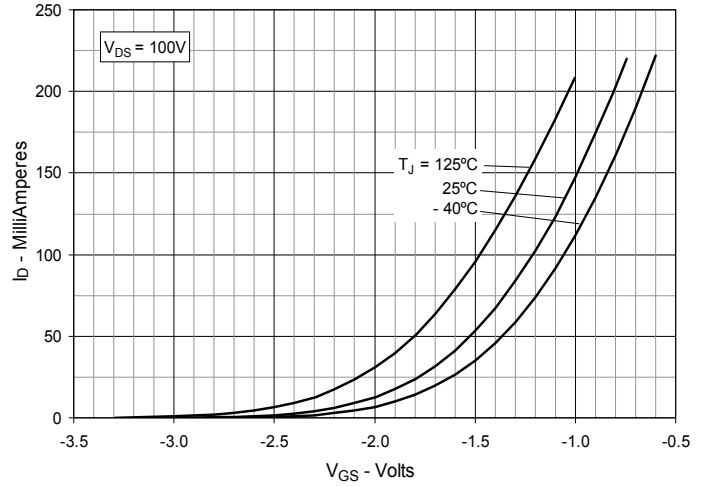


Fig. 9. Transconductance

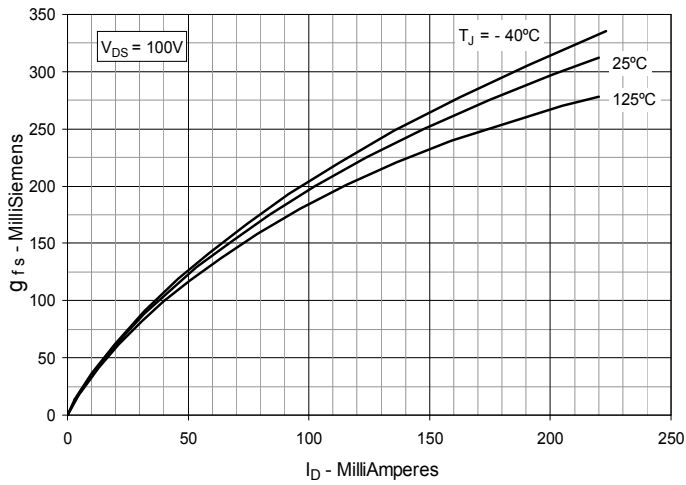


Fig. 10. Forward Voltage Drop of Intrinsic Diode

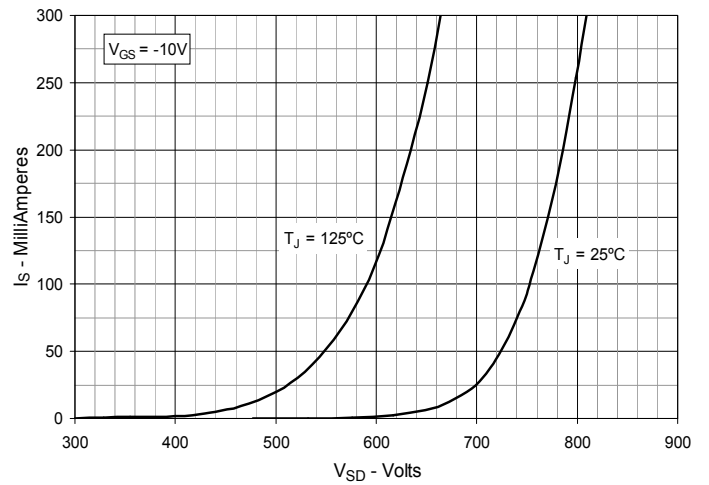


Fig. 11. Capacitance

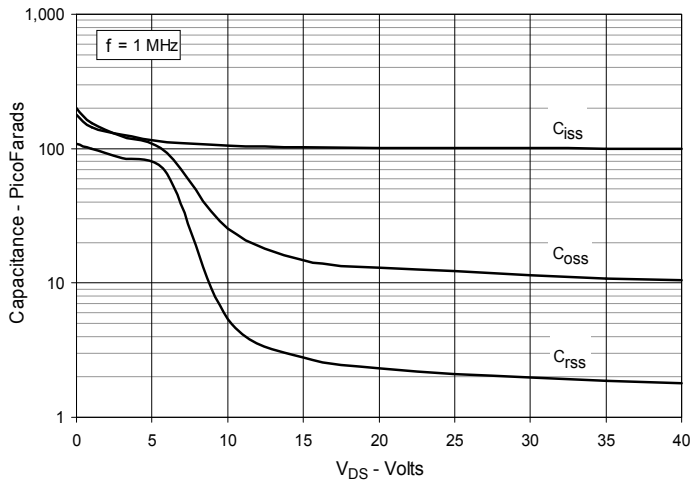


Fig. 12. Gate Charge

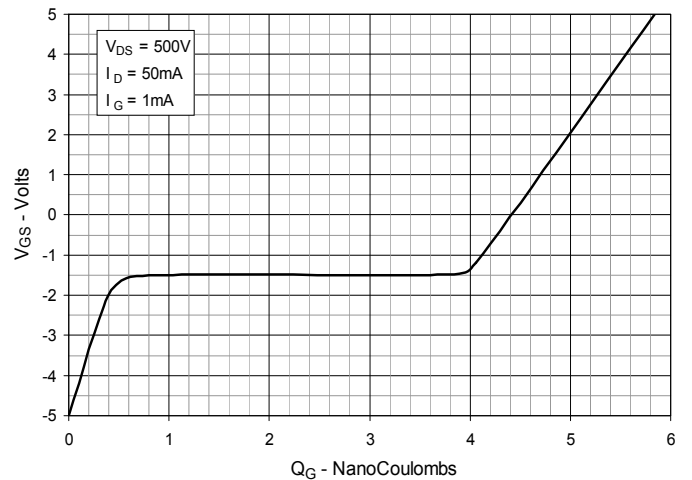


Fig. 13. Forward-Bias Safe Operating Area
@ $T_C = 25^\circ\text{C}$

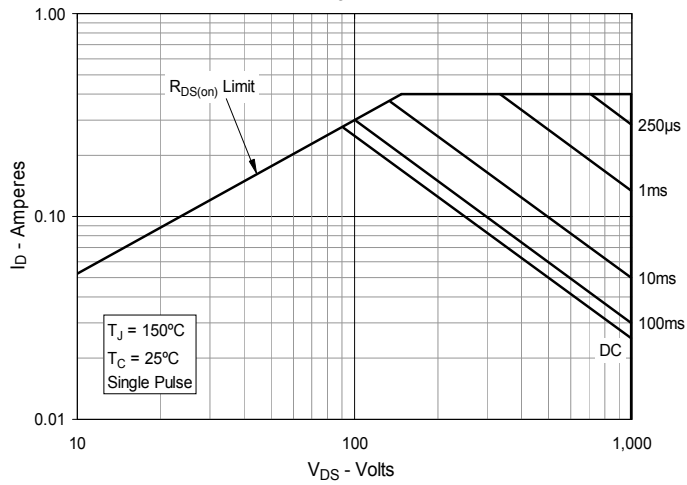


Fig. 14. Forward-Bias Safe Operating Area
@ $T_C = 75^\circ\text{C}$

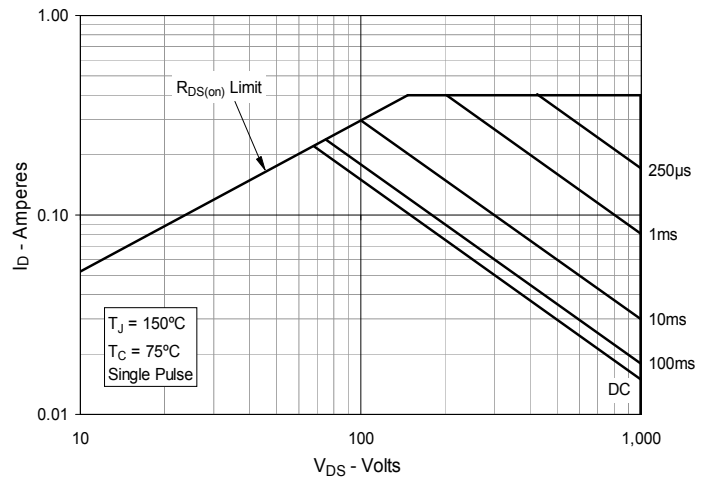


Fig. 15. Maximum Transient Thermal Impedance

