SM802124

ClockWorks™ DUAL 125MHz Ultra-Low Jitter, CMOS Frequency Synthesizer

General Description

The SM802124 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for Ethernet clock signals. It is based upon a unique patented RotaryWave® architecture that provides very-low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes two CMOS output clocks at 125MHz from a 15MHz LVCMOS reference clock.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

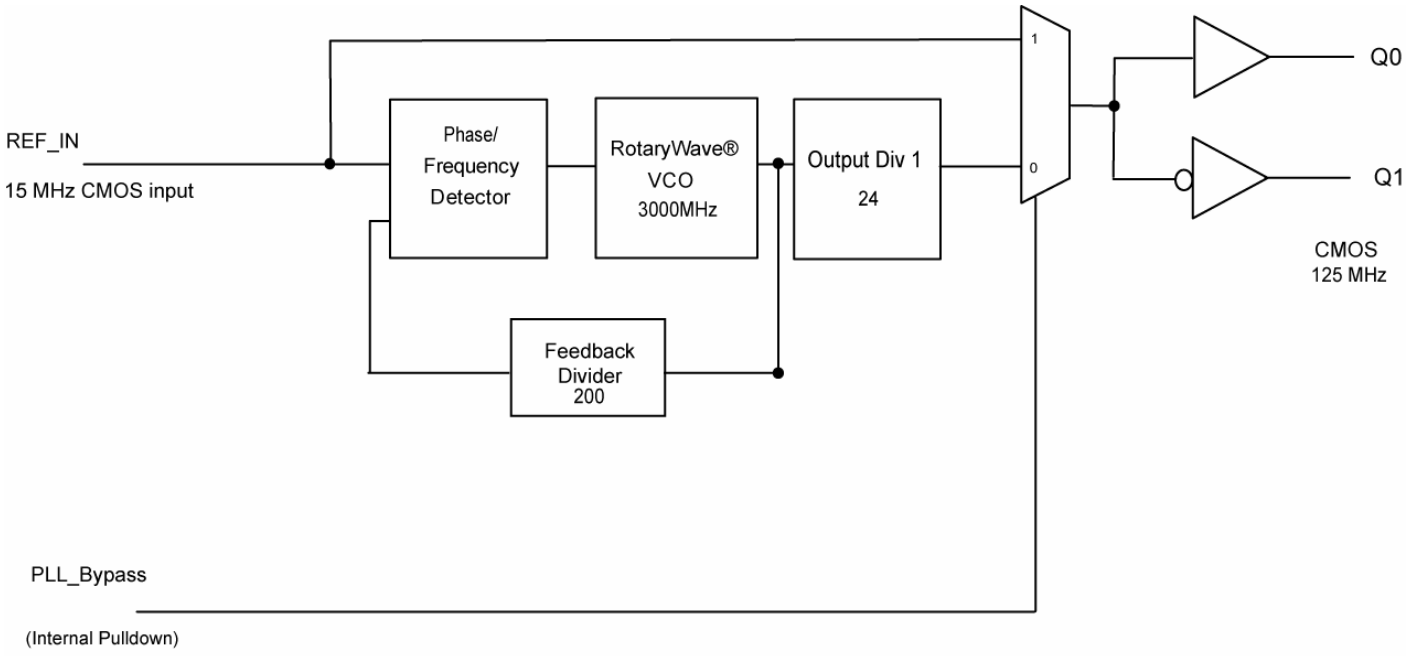
Features

- Generates two LVCMOS clock outputs at 125MHz
- 2.5V or 3.3V operating range
- Typical rms phase jitter @ 125MHz
  1.875MHz to 20MHz : 85fs
  (Input source dependent)
- Industrial temperature range (–40°C to +85°C)
- Green, RoHS, and PFOS compliant
- Available in 24-pin 4mm × 4mm QFN package

Applications

- Gigabit Ethernet

Block Diagram



ClockWorks is a trademark of Micrel, Inc
RotaryWave is a registered trademark of Multigig, Inc.

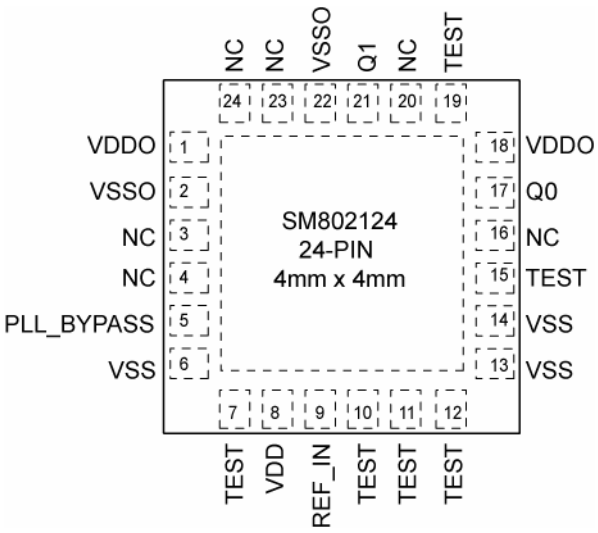
Ordering Information[1]

Part Number	Marking	Shipping	Temperature Range	Package
SM802124UMG	802124	Tube	–40°C to +85°C	24-Pin QFN
SM802124UMGTR	802124	Tape and Reel	–40°C to +85°C	24-Pin QFN

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



24-Pin QFN (code)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
17	Q0	O	CMOS	125MHz Clock Output
21	Q1	O	CMOS	180 deg,125MHz Clock Output
3, 4, 16 , 20, 23, 24	NC	-	-	No Connection. Do not connect anything to these pins.
1, 18	VDDO	PWR		Power Supply for Output
2, 22	VSSO	PWR		Power Supply Ground for Output
5	PLL_BYPASS	I, (SE)	LVCMOS	PLL Bypass, Selects Output Source 0 = Normal PLL Operation 1 = Output from Input Reference Clock 45KΩ pull-down
7, 10, 11, 12, 15, 19	TEST			Factory Test pins, Do not connect anything to these pins.
8	VDD	PWR		Core Power Supply
6, 13 , 14	VSS	PWR		Core Power Supply Ground
9	REF_IN	I, (SE)	LVCMOS	Reference Clock Input

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}, V_{DDO}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to V_{DD} + 0.5V
Lead Temperature (soldering, 20s) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{DD}, V_{DDO}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[3]
QFN (θ_{JA})
Still-Air ..... 50°C/W
QFN (ψ_{JB})
Junction-to-Board ..... 30°C/W

DC Electrical Characteristics[4]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, V_{DDO} = 2.5V ±5%

T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, V_{DDO}	2.5V Operating Voltage		2.375	2.5	2.625	V
V_{DD}, V_{DDO}	3.3V Operating Voltage		3.135	3.3	3.465	V
I_{DD}	Supply current V_{DD} + V_{DDO}	Outputs open		70	90	mA

LVCMOS OUTPUT DC Electrical Characteristics[4]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, V_{DDO} = 2.5V ±5%

T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO}/2.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage	Fig. 4	V_{DD} -0.7			V
V_{OL}	Output Low Voltage	Fig. 4			0.6	V

LVCMOS (PLL_BYPASS) DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–5			µA

REF_IN DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.6	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	–5		5	µA

AC Electrical Characteristics[4, 5]

V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5%

V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%

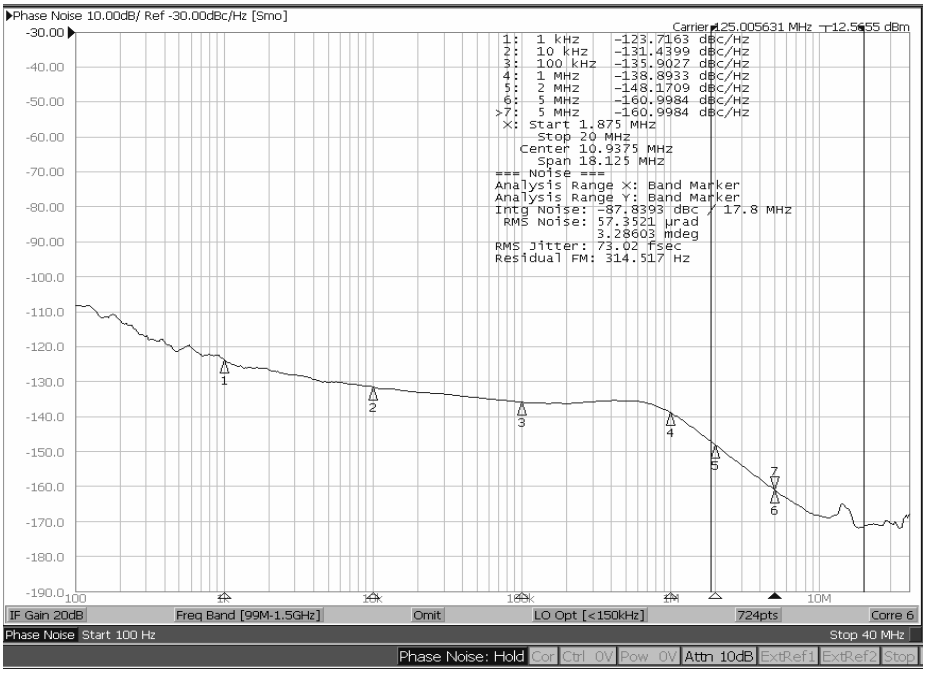
T_A = -40°C to 85°C. R_L = 50Ω to V_{DDO}/2

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency			125		MHz
F_{REF}	Reference Input Frequency			15		MHz
T_R/T_F	LVCMOS Output Rise/Fall Time	20% – 80%	100	300	500	ps
ODC	Output Duty Cycle		45	50	55	%
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter[6]	Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz)		85 320		fs
	Spurious Noise Components	5MHz 10MHz 20MHz 25MHz		-73 -82 -89 -96		dBc

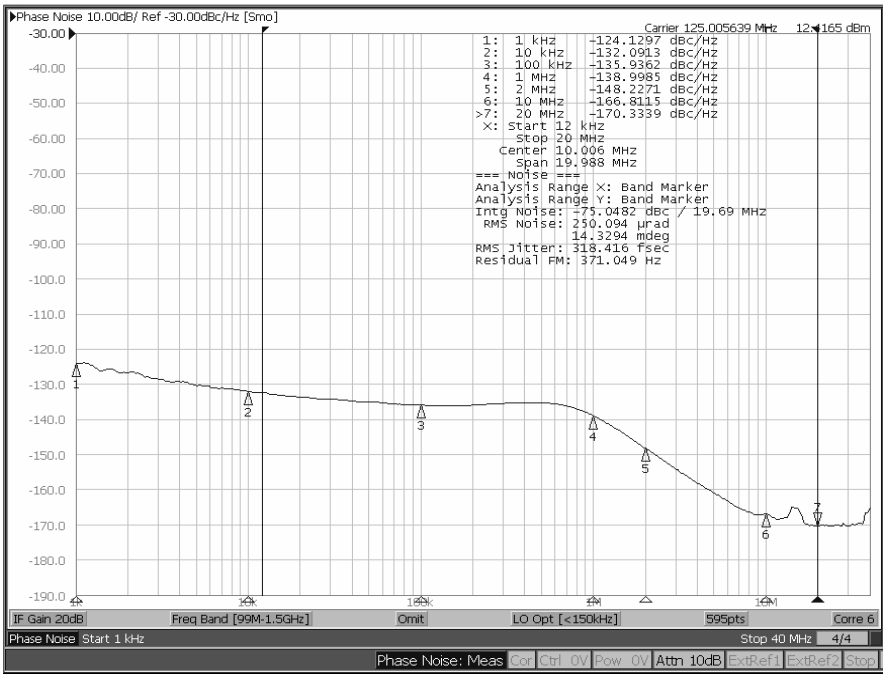
Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table after thermal equilibrium has been established.
5. All phase-noise measurements were taken with an Agilent 5052B phase-noise system.
6. Ref_IN driven with a low-noise source ClockWorks SM802001 programmed for a 15MHz CMOS output. Phase noise will track the input phase noise up to about 1MHz offset frequency.

Phase Noise Plots



Phase Noise Plot: 125MHz, 1.875MHz – 20MHz 73fS



Phase Noise Plot: 125MHz, 12kHz – 20MHz 318fS

Timing Diagrams

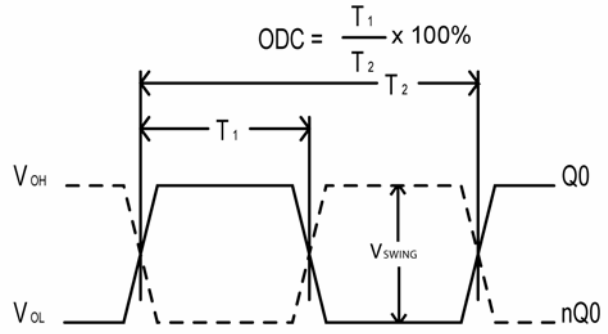


Figure 1. Duty Cycle Timing

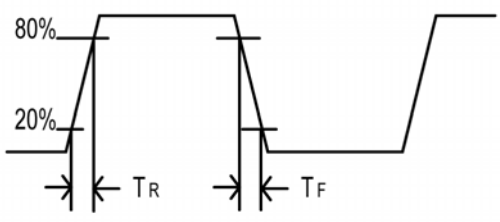


Figure 2. All outputs Rise/Fall Time

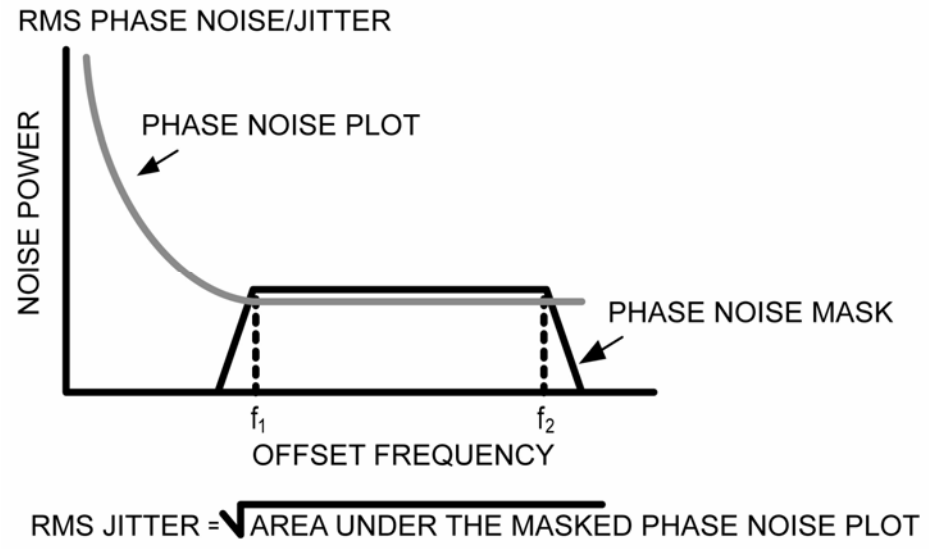


Figure 3. RMS Phase/Noise Jitter

Input and Output Stage

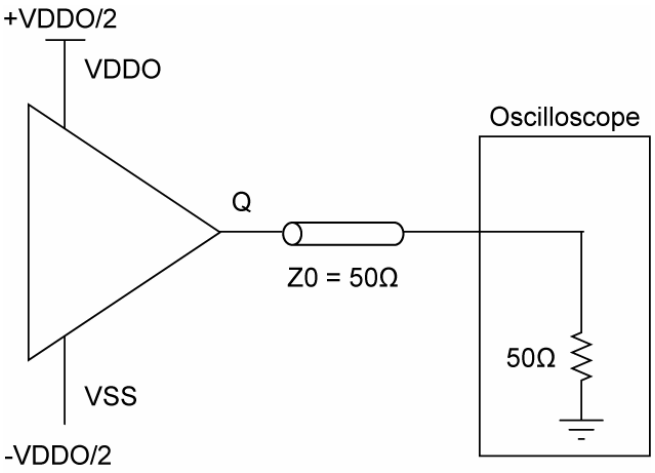
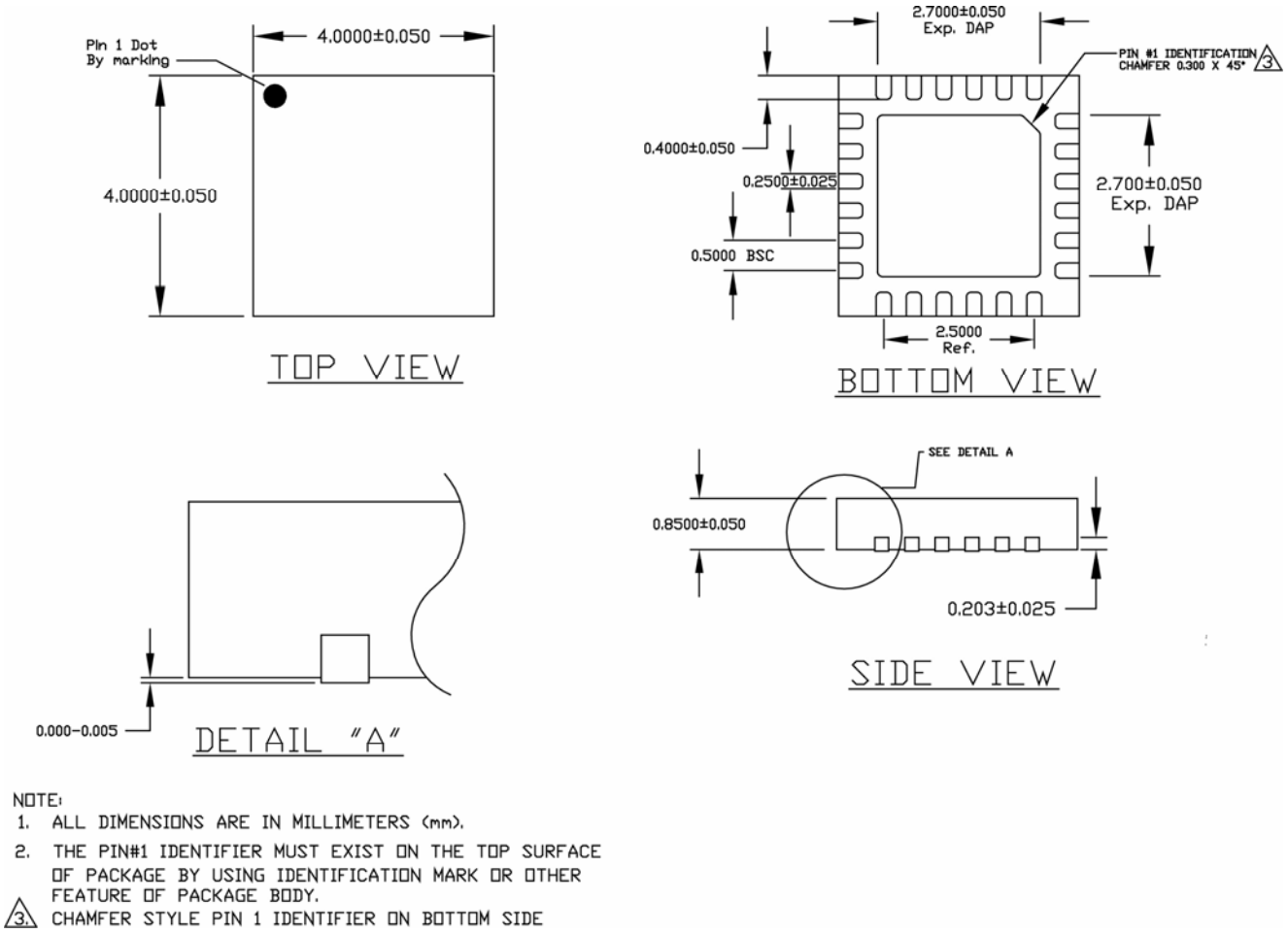


Figure 4. CMOS Output Load and Test Circuit

Package Information



24-Pin Package Type

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