



SY58608U

3.2Gbps Precision, 1:2 LVDS Fanout Buffer with Internal Termination and Fail Safe Input

General Description

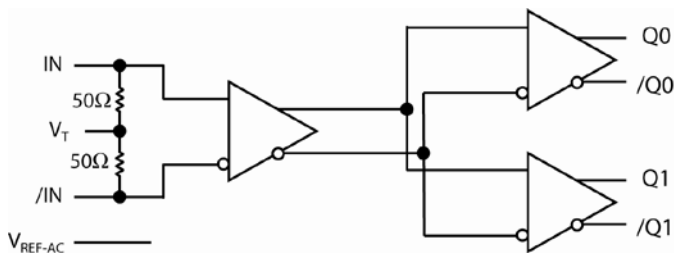
The SY58608U is a 2.5V, high-speed, fully differential 1:2 LVDS fanout buffer optimized to provide two identical output copies with less than 20ps of skew and less than 10ps_{PP} total jitter. The SY58608U can process clock signals as fast as 2GHz or data patterns up to 3.2Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled) as small as 100mV (200mV_{PP}) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated voltage reference (V_{REF-AC}) is provided to bias the V_T pin. The outputs are 325mV LVDS, with rise/fall times guaranteed to be less than 100ps.

The SY58608U operates from a 2.5V $\pm 5\%$ supply and is guaranteed over the full industrial temperature range (-40°C to $+85^\circ\text{C}$). For applications that require CML or LVPECL outputs, consider Micrel's SY58606U and SY58607U, 1:2 fanout buffers with 400mV and 800mV output swings respectively. The SY58608U is part of Micrel's high-speed, Precision Edge[®] product line.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Precision Edge[®]

Features

- Precision 1:2, 325mV LVDS fanout buffer
- Guaranteed AC performance over temperature and voltage:
 - DC-to > 3.2Gbps throughput
 - <300ps propagation delay (IN-to-Q)
 - <20ps within-device skew
 - <100ps rise/fall times
- Fail Safe Input
 - Prevents outputs from oscillating when input is invalid
- Ultra-low jitter design
 - <1ps_{RMS} cycle-to-cycle jitter
 - <10ps_{PP} total jitter
 - <1ps_{RMS} random jitter
 - <10ps_{PP} deterministic jitter
- High-speed LVDS outputs
- 2.5V $\pm 5\%$ power supply operation
- Industrial temperature range: -40°C to $+85^\circ\text{C}$
- Available in 16-pin (3mm x 3mm) QFN package

Applications

- All SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution
- Backplane distribution

Markets

- DataCom
- Telecom
- Storage
- ATE
- Test and Measurement

Precision Edge is a registered trademark of Micrel, Inc.

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • <http://www.micrel.com>

October 2006

M9999-102706-A
hbwhelp@micrel.com or (408) 955-1690

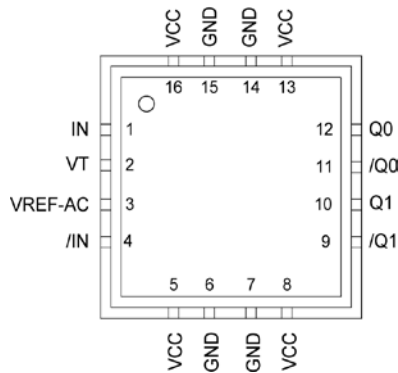
Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|-----------------------------|--------------|-----------------|--------------------------------------|----------------|
| SY58608UMG | QFN-16 | Industrial | 608U with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY58608UMGTR ⁽²⁾ | QFN-16 | Industrial | 608U with Pb-Free bar-line indicator | NiPdAu Pb-Free |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



16-Pin QFN

Pin Description

| Pin Number | Pin Name | Pin Function |
|-----------------|--------------------|--|
| 1, 4 | IN, /IN | Differential Inputs: This input pair is the differential signal input to the device. Input accepts DC-coupled differential signals as small as 100mV (200mV _{PP}). Each pin of this pair internally terminates with 50Ω to the VT pin. If the input swing falls below a certain threshold (typical 30mV), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the outputs to its last valid state. See “Input Interface Applications” section for more details. |
| 2 | VT | Input Termination Center-Tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See “Input Interface Applications” section. |
| 3 | VREF-AC | Reference Voltage: This output bias to V _{CC} -1.2V. It is used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the VT pin. Bypass with 0.01μF low ESR capacitor to V _{CC} . Maximum sink/source current is ±1.5mA. See “Input Interface Applications” section for more details. |
| 5, 8, 13, 16 | VCC | Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors as close to the VCC pins as possible. |
| 6, 7, 14, 15 | GND, Exposed pad | Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin. |
| 9, 10 11, 12 | /Q1, Q1 /Q0, Q0 | LVDS Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 325mV. Normally terminated 100Ω across the output pairs (Q and /Q). See “LVDS Output Termination” section. |

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC}) -0.5V to +4.0V
 Input Voltage (V_{IN}) -0.5V to $V_{CC} + 0.3V$
 LVDS Output Current (I_{OUT}) $\pm 10mA$
 Input Current
 Source or Sink Current on (IN, /IN) $\pm 50mA$
 Current (V_{REF})
 Source or sink current on V_{REF-AC} ⁽⁴⁾ $\pm 1.5mA$
 Maximum Operating Junction Temperature 125°C
 Lead Temperature (soldering, 20sec.) 260°C
 Storage Temperature (T_s) -65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{IN}) +2.375V to +2.635V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance⁽³⁾
 QFN
 Still-air (θ_{JA}) 60°C/W
 Junction-to-board (ψ_{JB}) 33°C/W

DC Electrical Characteristics⁽⁵⁾

$T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|---|------------------------------|--------------|--------------|--------------|----------|
| V_{CC} | Power Supply Voltage Range | | 2.375 | 2.5 | 2.625 | V |
| I_{CC} | Power Supply Current | No load, max. V_{CC} | | 55 | 75 | mA |
| R_{DIFF_IN} | Differential Input Resistance (IN-to-/IN) | | 90 | 100 | 110 | Ω |
| V_{IH} | Input HIGH Voltage (IN, /IN) | IN, /IN | 1.2 | | V_{CC} | V |
| V_{IL} | Input LOW Voltage (IN, /IN) | IN, /IN | 0 | | $V_{IH}-0.1$ | V |
| V_{IN} | Input Voltage Swing (IN, /IN) | see Figure 3a, Note 6 | 0.1 | | 1.7 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing (IN - /IN) | see Figure 3b | 0.2 | | | V |
| V_{IN_FSI} | Input Voltage Threshold that Triggers FSI | | | 30 | 100 | mV |
| V_{REF-AC} | Output Reference Voltage | | $V_{CC}-1.3$ | $V_{CC}-1.2$ | $V_{CC}-1.1$ | V |
| IN to V_T | Voltage from Input to V_T | | | | 1.28 | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IN} (max) is specified when V_T is floating.

LVDS Outputs DC Electrical Characteristics⁽⁷⁾

$V_{CC} = +2.5V \pm 5\%$, $R_L = 100\Omega$ across the output pairs; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------|-----------------------------------|---------------|-------|------|-------|-------|
| V_{OUT} | Output Voltage Swing | See Figure 3a | 250 | 325 | | mV |
| V_{DIFF_OUT} | Differential Output Voltage Swing | See Figure 3b | 500 | 650 | | mV |
| V_{OCM} | Output Common Mode Voltage | | 1.125 | 1.20 | 1.275 | V |
| ΔV_{OCM} | Change in Common Mode Voltage | | -50 | | 50 | mV |

Notes:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics⁽⁸⁾

$V_{CC} = +2.5V \pm 5\%$, $R_L = 100\Omega$ across the output pairs, Input $t_r/t_f \leq 300ps$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------|------------------------------------|-------------------------|-----|------|-----|---------------|
| f_{MAX} | Maximum Frequency | NRZ Data | 3.2 | 4.25 | | Gbps |
| | | $V_{OUT} > 200mV$ Clock | 2 | 3 | | GHz |
| t_{PD} | Propagation Delay IN-to-Q | $V_{IN}: 100mV-200mV$ | 170 | 280 | 420 | ps |
| | | $V_{IN}: 200mV-800mV$ | 130 | 200 | 300 | ps |
| t_{Skew} | Within Device Skew | Note 9 | | 5 | 20 | ps |
| | Part-to-Part Skew | Note 10 | | | 135 | ps |
| t_{Jitter} | Data Random Jitter | Note 11 | | | 1 | μs_{RMS} |
| | Deterministic Jitter | Note 12 | | | 10 | μs_{PP} |
| | Clock Cycle-to-Cycle Jitter | Note 13 | | | 1 | μs_{RMS} |
| | Total Jitter | Note 14 | | | 10 | μs_{PP} |
| t_r, t_f | Output Rise/Fall Time (20% to 80%) | At full output swing. | 35 | 60 | 100 | ps |
| | Duty Cycle | Differential I/O | 47 | | 53 | % |

Notes:

8. These high-speed parameters are Guaranteed by design and characterization.
9. Within-device skew is measured between two different outputs under identical input transitions.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
11. Random jitter is measured with a K28.7 pattern, measured at $\leq f_{MAX}$.
12. Deterministic jitter is measured at 2.5Gbps with both K28.5 and $2^{23}-1$ PRBS pattern.
13. Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input frequency of $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Functional Description

Fail-Safe Input (FSI)

The input includes a special fail-safe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below 100mV_{PK} (200mV_{PP}), typically 30mV_{PK} . Maximum frequency of SY58608U is limited by the FSI function.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing such that the differential voltage across the input pair is less than 100mV , the FSI function will eliminate a metastable condition and latch the outputs to the last valid state. No ringing and no indeterminate state will occur at the output under these conditions. The output recovers to normal operation once the input signal returns to a valid state with a differential voltage $\geq 100\text{mV}$.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to "Typical Characteristics" for detailed information.

Timing Diagrams

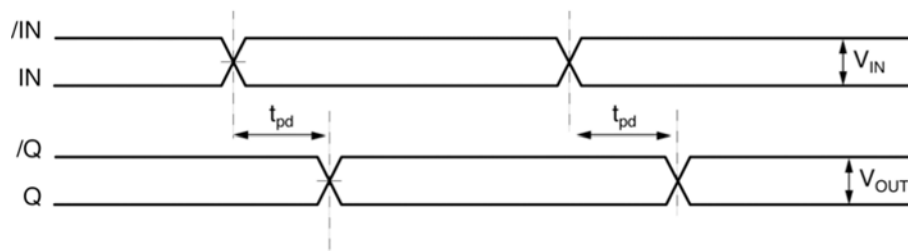


Figure 1a. Propagation Delay

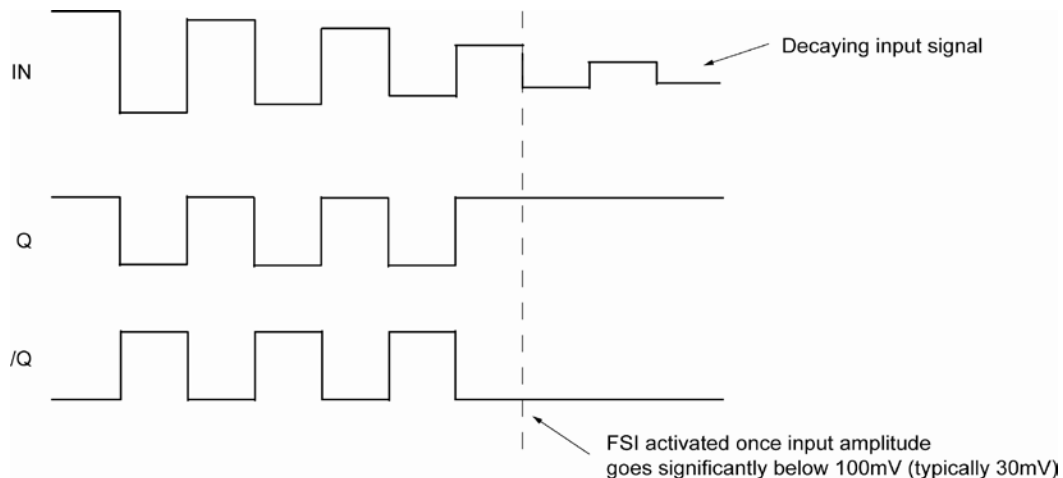
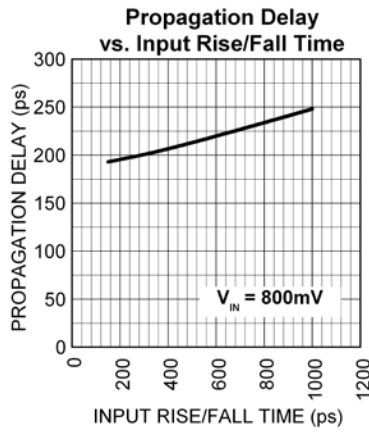
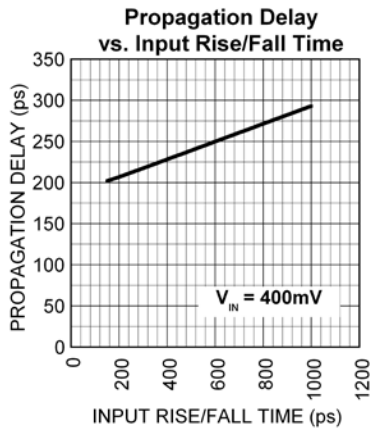
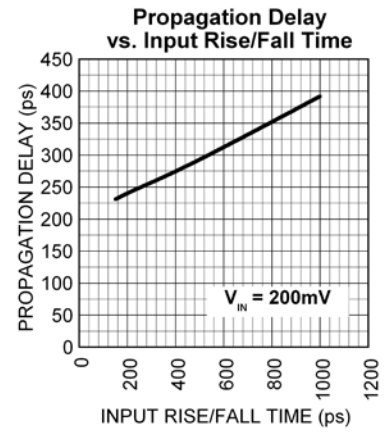
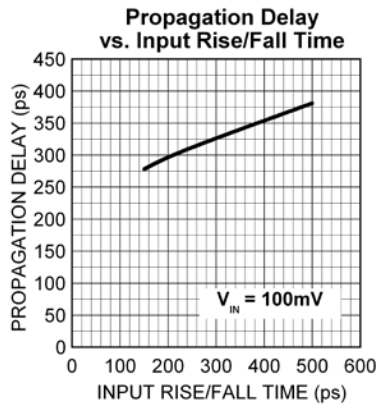
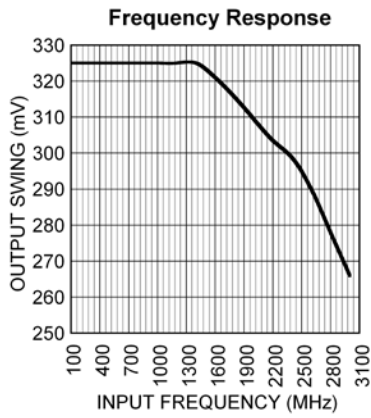


Figure 1b. Fail Safe Feature

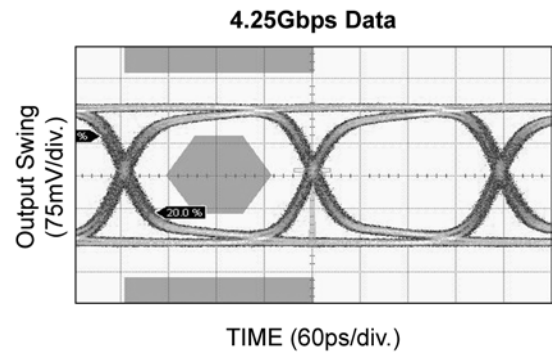
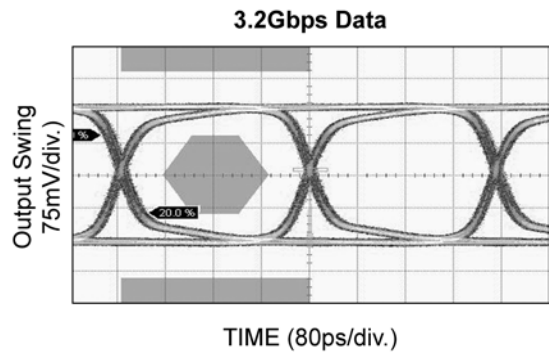
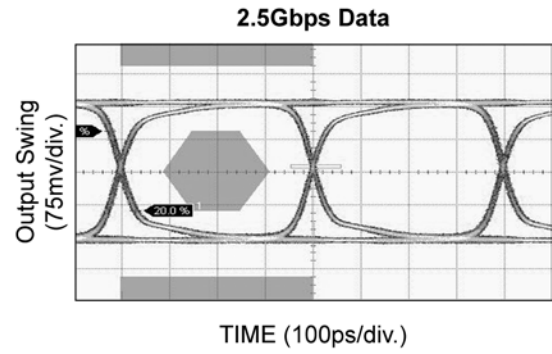
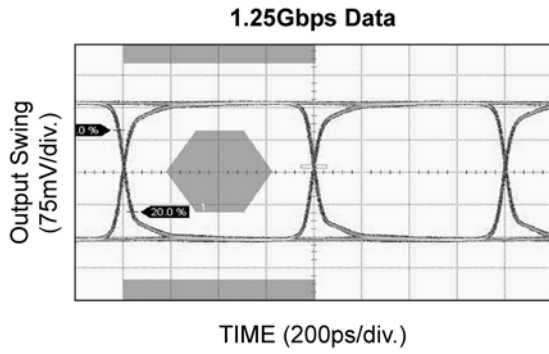
Typical Characteristics

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 100mV$, $R_L = 100\Omega$ across the output pairs, $T_A = 25^\circ C$, unless otherwise stated.



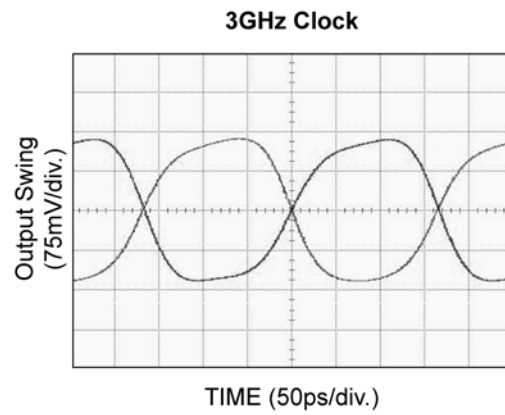
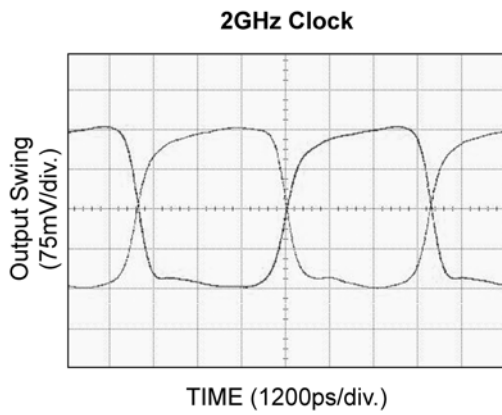
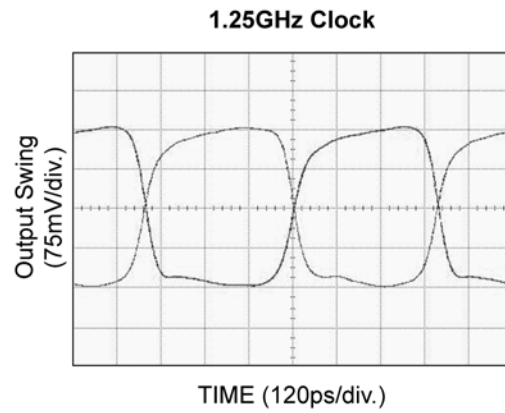
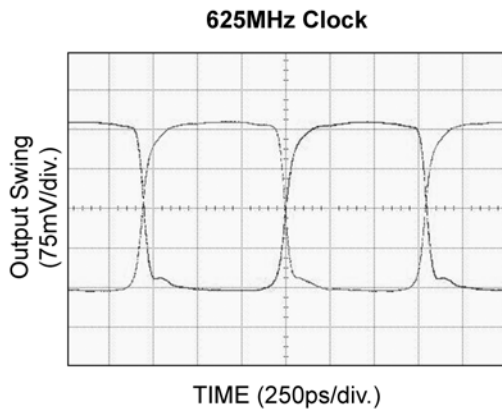
Functional Characteristics

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 250mV$, Data Pattern: $2^{23}-1$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



Functional Characteristics (continued)

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 250mV$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



Input Stage

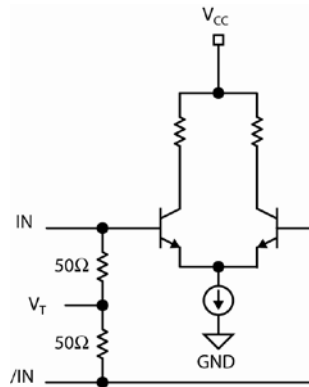


Figure 2. Simplified Differential Input Buffer



Figure 3a. Single-Ended Swing

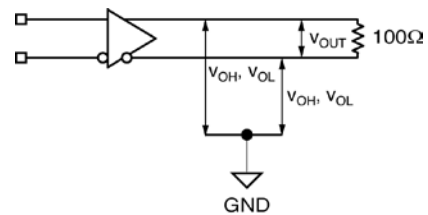


Figure 3c. LVDS Differential Measurement

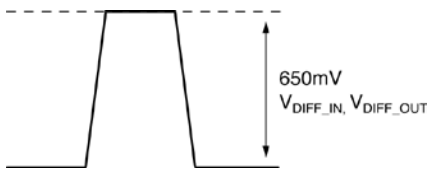


Figure 3b. Differential Swing

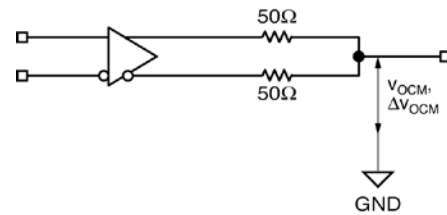


Figure 3d. LVDS Common Mode Measurement

Input Interface Applications

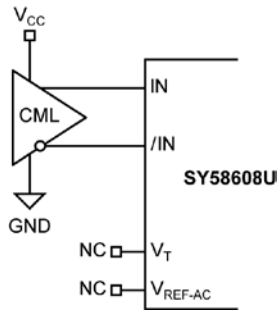


Figure 4a. CML Interface (DC-Coupled)

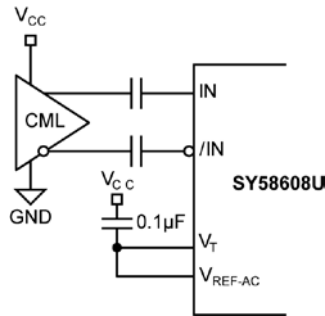


Figure 4b. CML Interface (AC-Coupled)

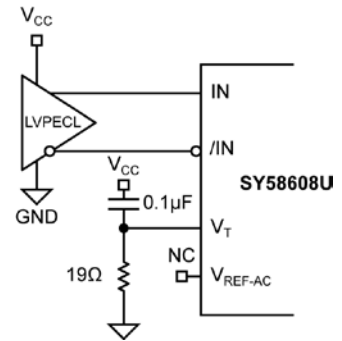


Figure 4c. LVPECL Interface (DC-Coupled)

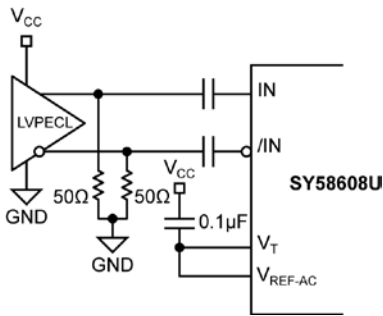


Figure 4d. LVPECL Interface (AC-Coupled)

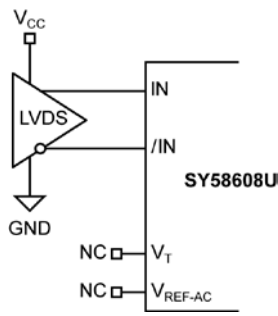
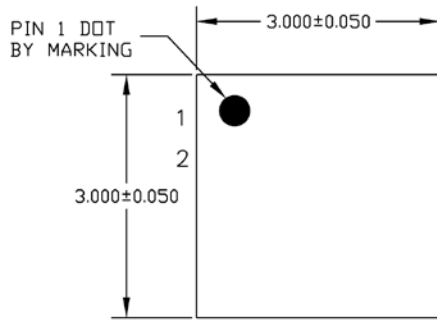


Figure 4e. LVDS Interface (DC-Coupled)

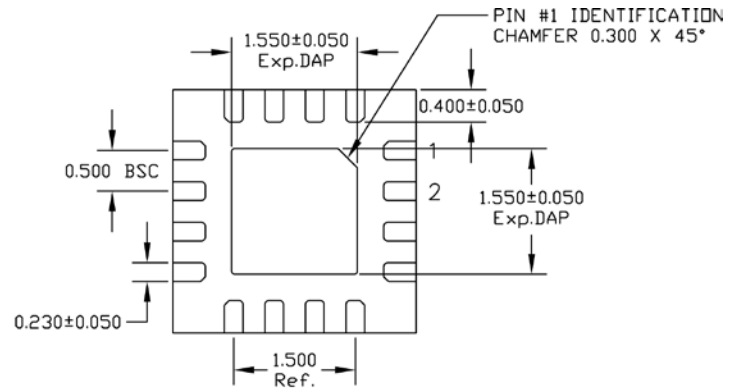
Related Product and Support Documents

| Part Number | Function | Data Sheet Link |
|---------------|---|---|
| SY58606U | 4.25Gbps Precision, 1:2 CML Fanout Buffer with Internal Termination and Fail Safe Input | http://www.micrel.com/page.do?page=/product-info/products/sy58606u.shtml |
| SY58607U | 3.2Gbps Precision, 1:2 LVPECL Fanout Buffer with Internal Termination and Fail Safe Input | http://www.micrel.com/page.do?page=/product-info/products/sy58607u.shtml |
| HBW Solutions | New Products and Termination Application Notes | http://www.micrel.com/product-info/products/sy89830u.shtml |

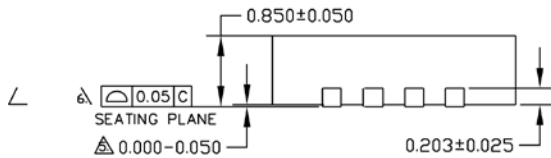
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- ⚠ APPLIED ONLY FOR TERMINALS.
- ⚠ APPLIED FOR EXPOSED PAD AND TERMINALS.

16-Pin (3mm x 3mm) QFN

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
 TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

The information furnished by Micrel in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2006 Micrel, Incorporated.