

QUINT EXCLUSIVE OR/NOR GATE

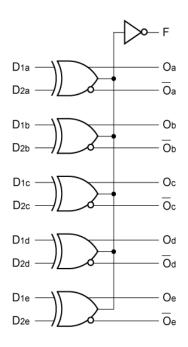
FEATURES

- Max. propagation delay of 1000ps
- IEE min. of –58mA
- Extended supply voltage option: VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 50% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

The SY100S307 is an ultra-fast quint exclusive-OR/NOR gate designed for use in high-performance ECL systems. A function output that is the wire-OR result of the exclusive-OR outputs is also available. The inputs on the device have $75k\Omega$ pull-down resistors.

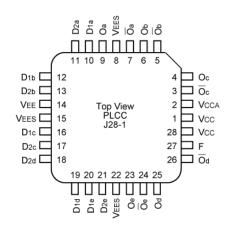
BLOCK DIAGRAM



PIN NAMES

Pin	Function
Dna – Dne	Data Inputs (n-15)
E	Enable Input
Oa – Oe	Data Outputs
Oa – Oe	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S307JC	J28-1	Commercial	SY100S307JC	Sn-Pb
SY100S307JCTR ⁽¹⁾	J28-1	Commercial	SY100S307JC	Sn-Pb
SY100S307JZ ⁽²⁾	J28-1	Commercial	SY100S307JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S307JZTR ^(1, 2)	J28-1	Commercial	SY100S307JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S307JY ⁽²⁾	J28-1	Industrial	SY100S307JY with Pb-Free bar-line indicator	Matte-Sn
SY100S307JYTR ^(1,2)	J28-1	Industrial	SY100S307JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.

2. Pb-Free package is recommended for new designs.

LOGIC EQUATION

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\begin{split} \mathsf{F} &= (\mathsf{D}\mathtt{1a} \oplus \mathsf{D}\mathtt{2a}) + (\mathsf{D}\mathtt{1b} \oplus \mathsf{D}\mathtt{2b}) + (\mathsf{D}\mathtt{1c} \oplus \mathsf{D}\mathtt{2c}) + (\mathsf{D}\mathtt{1d} \oplus \mathsf{D}\mathtt{2d}) \\ &+ (\mathsf{D}\mathtt{1e} \oplus \mathsf{D}\mathtt{2e}). \end{split}
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DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

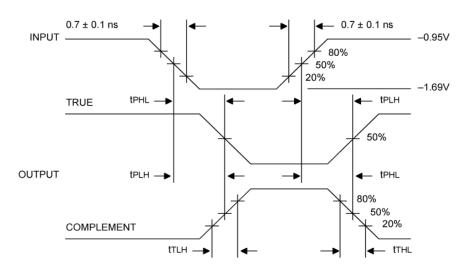
Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition
Іін	Input HIGH Current				μA	VIN = VIH (Max.)
	D2a — D2e	—	—	200		
	D2a — D2e	—	—	250		
IEE	Power Supply Current	-58	-40	-27	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

		TA = -40°C		TA = 0°C		TA = +25°C		TA = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
tPLH tPH2	Propagation Delay D2a — D2e to O, O	300	1000	300	1000	300	1000	300	1000	ps	
tplh tphl	Propagation Delay D1a — D1e to O, O	300	900	300	900	300	900	300	930	ps	
tplh tphl	Propagation Delay Data to F	300	1425	300	1425	300	1425	300	1425	ps	
tт∟н tтн∟	Transition Time 3 20% to 80%, 80% to 20%	00	900	00	900	300	900	300	900	ps	

TIMING DIAGRAM

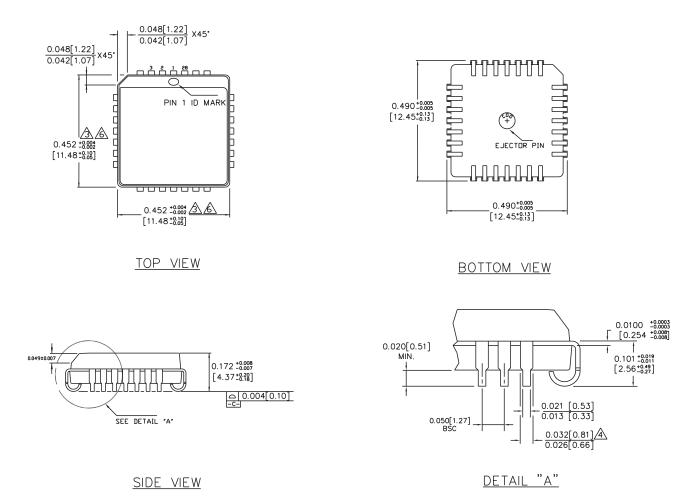


Propagation Delay and Transition Times

NOTE:

VEE = -4.2V to -5.5V unless otherwise specified, Vcc = VccA = GND

28-PIN PLCC (J28-1)



NOTES:

1.

- ITES: DIMENSIONS ARE IN INCHES [MM]. CONTROLLING DIMENSION: INCHES. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203]. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN DACKAGE TOP DIMENSION MAX BE SUICHTLY ∕3∖
- <u>A</u>
- 5.
- \triangle
- PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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