

**FEATURES**

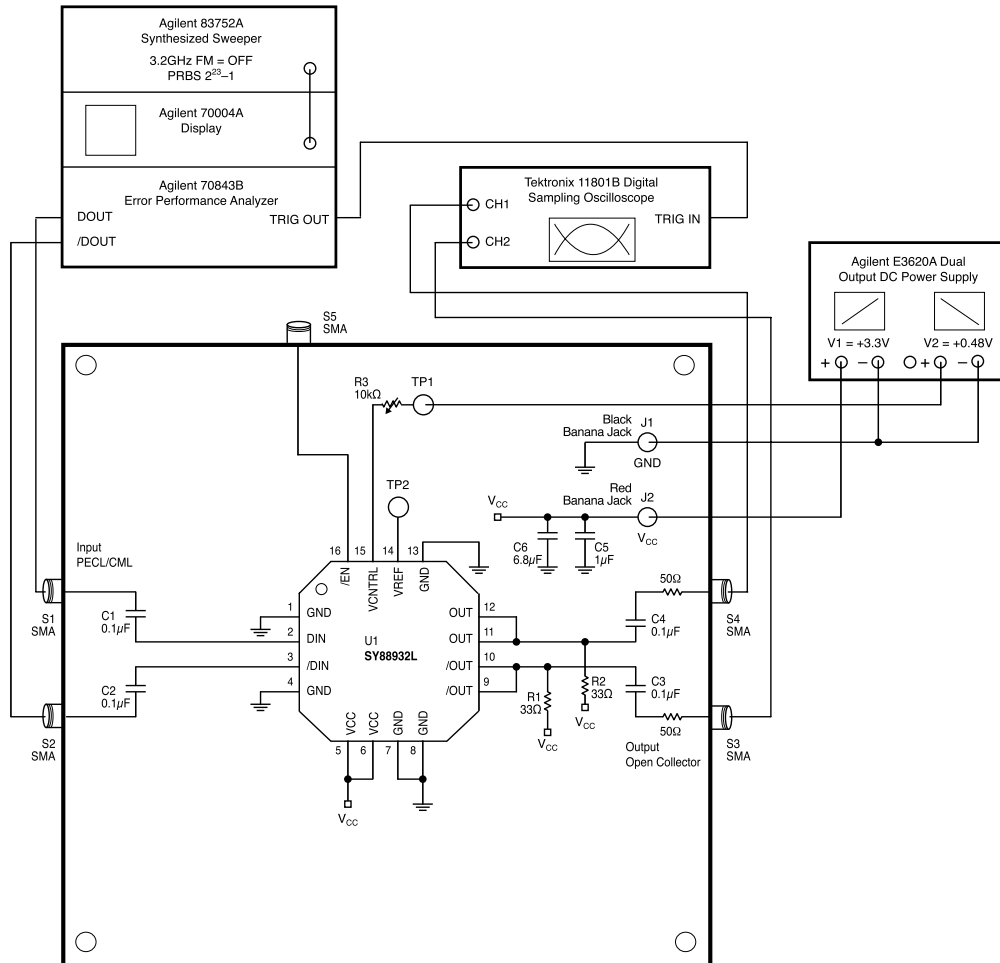
- Up to 3.2Gbps operation
- Modulation current to 60mA
- 50Ω input termination
- Rise/fall times < 70ps
- Programmable laser modulation voltage
- Operating temperature range: -40°C to +85°C
- Available in tiny 16-pin (3mm × 3mm) MLF™ package

**DESCRIPTION**

The SY88932L 3.3V SONET laser driver is the smallest laser driver with programmable modulation current used for applications up to 3.2Gbps. The device accepts either PECL or CML level data inputs. The SY88932L provides modulation voltage/current of up to 60mA for FP (Fabry-Perot) or DFB (Distribution Feedback) lasers. There is a 75kΩ pull-down resistor to V<sub>EE</sub> at the input of /EN. An active TTL enable signal shuts off the modulation current.

This document provides design and implementation information, as well as, a detailed description of the SY88932L evaluation board. The evaluation board is AC-coupled, and has both differential inputs and outputs, and a resistor port to vary the modulation voltage.

**TEST SET-UP FOR EVALUATION BOARD**



**Figure 1. Test Set-Up for the SY88932L Evaluation Board**

## Functional Description

The evaluation board for the SY88932L is AC-coupled and is meant to show the AC-performance of the part in terms of  $I_{MOD}$  vs.  $t_{rise}$ ,  $t_{fall}$ , RMS jitter, and eye diagram. In addition, since the evaluation board is AC-coupled, no laser can be mounted. Further, biasing of the board does not require complex split power supplies and requires only a single-dual power source.

Note, however, that the output level is inverted, meaning that a high signal input generates a low signal output, likewise, a low signal input generates a high signal output. Further, the modulation current  $I_{MOD}$  varies linearly with the modulation voltage  $V_{CNTRL}$ . See Figure 8  $I_{MOD}$  vs.  $V_{CNTRL}$ .

## Power Supply

The SY88932L is a +3.3V device, therefore,  $V_{CC}$  or Jack 2 should be connected to +3.3V, and GND or Jack 1 should be connected to 0V.

## Board Layout and Design

The evaluation board is fabricated using standard FR-4 dielectric material, using coplanar transmission line structure and has been designed to minimize crosstalk, noise, and achieve high bandwidth.

Layer 1	Signal $Z_0 = 50\Omega$ /GND
Layer 2	Impedance GND
Layer 3	$V_{CC}$
Layer 4	GND

**Table 1. Layer Stack**

Pin	Function
$D_{IN}$ , $/D_{IN}$	CML/PECL, Internal $50\Omega$ termination, NRZ Data.
$/EN$	TTL Compatible Input.
GND	Ground.
OUT, $/OUT$	Open Collector Output Signal AC-Coupled with $33\Omega$ to $V_{CC}$ .
$V_{CC}$	Power Supply.
TP1, TP2	Connected if you chose to use $V_{REF}$ as source for $V_{CNTRL}$ pin.
R3	Variable Resistor Pot to Control $V_{CNTRL}$ , and $I_{MOD}$ .

**Table 2. Evaluation Board Signal Inputs and Outputs**

**Note 1:** *PECL Operation:* Typical voltage swing is 700mV to 800mV into  $50\Omega$ . In addition, common mode voltage for PECL is  $V_{CC} - 1.3V$ .

**Note 2:** *CML Operation:* Typical voltage swing is  $V_{CC}$  to  $V_{CC} - 400mV$  or 400mV.

## Test Description

This section contains step-by-step instructions for evaluating the SY88932L in terms of AC and DC performance. AC performance being  $t_{rise}$ ,  $t_{fall}$ , RMS jitter, and eye-diagram generation. DC performance being,  $I_{MOD}$  vs.  $V_{MOD}$  linearity.

## Equipment used for measurement

- Agilent E3620A dual output DC power supply
- Tektronix 11801 digital sampling oscilloscope
- Agilent 83752A Synthesized Sweeper
- HP7000A display
- Agilent 70843B error performance analyzer
- Matched high-speed cables w/SMA connectors
- SY88932L evaluation board

## SET-UP FOR MEASUREMENTS

1. Connect  $V_{CC}$  to Jack 2 to +3.3V and connect GND or Jack 1 to ground.
2. Connect TP1 to a power source as shown in Figure 1, Test Set-Up for for the SY88932L.
3. Using an Agilent 83752A Synthesized Sweeper, set the frequency, and choose PRBS 2<sup>23</sup>-1 with FM mode off.
4. Connect  $D_{OUT}$ , and  $/D_{OUT}$  of the Agilent 70843B to drive SMA1 and SMA2,  $D_{IN}$  and  $/D_{IN}$ , of the SY88932L evaluation board. Then connect the trigger out to the trigger input of the Tektronix 11801B digital sampling oscilloscope.
5. Next, connect SMA3 and SMA4 which are the outputs of the evaluation board to Tektronix 11801B's CH1 and CH2 inputs.
6. By varying the modulation current and voltage, a set of AC measurements such Table 3,  $I_{MOD}$  vs.  $t_{rise}$ ,  $t_{fall}$ , and jitter can be generated.

Unit	I <sub>MOD</sub> (mA)	V <sub>CC</sub> = +3.0V						V <sub>CC</sub> = +3.3V			V <sub>CC</sub> = +3.6V					
		T <sub>A</sub> = -40°C			T <sub>A</sub> = +85°C			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C			T <sub>A</sub> = +85°C		
		t <sub>r</sub> (ps)	t <sub>f</sub> (ps)	Jitter(RMS)	t <sub>r</sub> (ps)	t <sub>f</sub> (ps)	Jitter(RMS)	t <sub>r</sub> (ps)	t <sub>f</sub> (ps)	Jitter (RMS)	t <sub>r</sub> (ps)	t <sub>f</sub> (ps)	Jitter (RMS)	t <sub>r</sub> (ps)	t <sub>f</sub> (ps)	Jitter (RMS)
1	10	46.2	43.2	2.46	49.2	41.2	2.31	46.5	40.8	2.44	46.2	41.1	2.5	47.9	39.3	2.55
	30	53.3	55.8	2.5	56.2	53.6	2.62	56	55	2.45	55	53.3	2.34	59.1	53.2	3.12
	50	60.7	72.4	3.73	62.2	90.4	8.33	63.6	72.2	7.18	62.7	67	2.26	63.4	72.1	7.06

Table 3. AC Parameters

**OUTPUT WAVEFORM MEASUREMENTS**

Figures 2 through Figure 7, illustrates the output waveforms of the SY88932L at different data rates and different I<sub>MOD</sub> current.

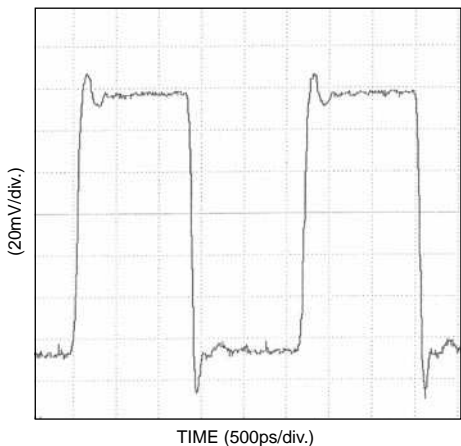


Figure 2. Output Waveform (750Mbps w/I<sub>MOD</sub> ~ 10mA, +3.3V)

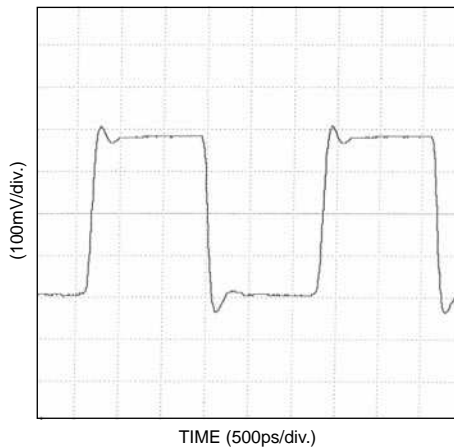


Figure 4. Output Waveform (750Mbps w/I<sub>MOD</sub> ~ 30mA, +3.3V)

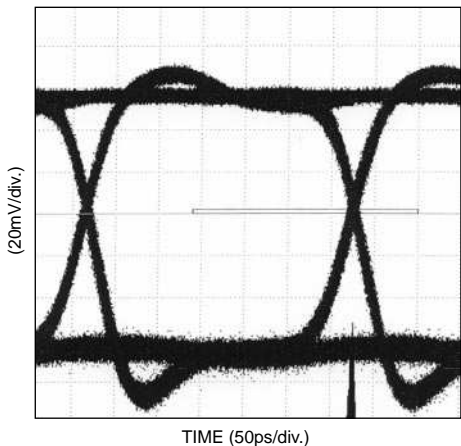


Figure 3. Output Waveform (3.2Gbps w/I<sub>MOD</sub> ~ 10mA, +3.3V)

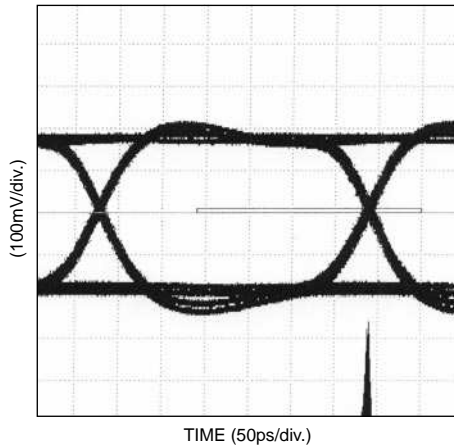
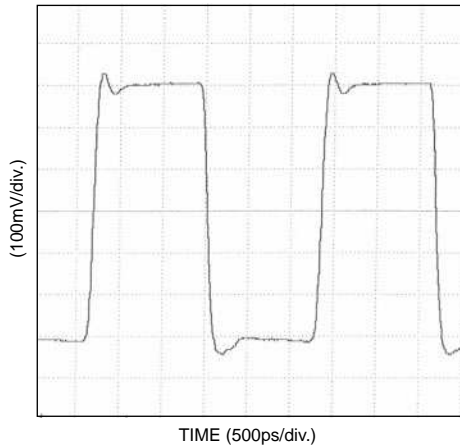
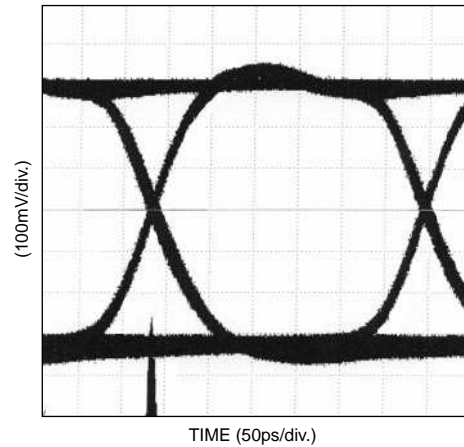


Figure 5. Output Waveform (3.2Gbps w/I<sub>MOD</sub> ~ 30mA, +3.3V)



**Figure 6. Output Waveform (750Mbps w/ $I_{MOD} \sim 50\text{mA}$ , +3.3V)**



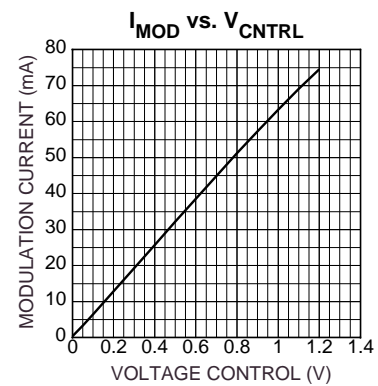
**Figure 7. Output Waveform (3.2Gbps w/ $I_{MOD} \sim 50\text{mA}$ , +3.3V)**

Note: Figure 7 is shown with a DC-coupled board, rather than an AC-coupled board. If a SY88932L is tested at  $I_{MOD} \sim 50\text{mA}$ , on an AC-coupled board, the outputs may saturate since the output is expecting  $V_{CC}$  as the DC-operating point.

By varying  $V_{CNTRL}$ , a set of DC measurements of  $I_{MOD}$  vs.  $V_{CNTRL}$  can be generated as shown in Table 4 and Figure 8.

$V_{CC} = +3.3\text{V}$	
$T_A = +25^\circ\text{C}$ (Unit 1)	
$V_{CNTRL}$ (V)	$I_{MOD}$ (mA)
0	0.4
0.05	3.3
0.10	6.4
0.15	9.6
0.2	12.8
0.3	19.3
0.4	25.7
0.5	32.2
0.6	38.5
0.7	44.9
0.8	51.2
0.9	57.3
1.0	63.3
1.1	69.1
1.2	74.5

**Table 4. DC Parameters**



**Figure 8.  $I_{MOD}$  vs.  $V_{CNTRL}$  (Typical Condition)**

## LAYOUT TIPS

1. Establish controlled impedance stripline, microstrip, or co-planar construction techniques for high-speed signal paths.
2. All differential paths are critical timing paths, and skew should be matched to within  $\pm 5\%$ . If in doubt, perform TDR analysis of signal traces.
3. Isolate the input, and output signals from other signal sources. Isolation can be achieved by putting ground traces in between.
4. Place output load resistors as close to the open collector output as possible.
5. DIN and /DIN traces should layout symmetrically, likewise, OUT and /OUT should layout symmetrically.
6. The 16-pin MLF™ package contains a soldermask which should be grounded. The soldermask is used for thermo considerations. Further, the die internal to the package is grounded to the soldermask. See the SY88932L data sheet for details.

## DESCRIPTION OF CONNECTORS

Connector	Name	Type	Connects to	Description
SMA1	DIN	CML/PECL	Pin 2	AC-Coupled Input
SMA2	/DIN	CML/PECL	Pin 3	AC-Coupled Input
SMA3	/OUT	Open Collector	Pin 9 and 10	AC-Coupled Output
SMA4	OUT	Open Collector	Pin 11 and 12	AC-Coupled Output

**BILL OF MATERIALS**

Item	Part Number	Manufacturer	Description	Qty.
C1, C2 C3, C4, C5	PCC2146CT-ND	Panasonic/Digi-Key <sup>(1)</sup>	0.1 $\mu$ F 10%, 25V X5R, Dielectric Ceramic Capacitor, Size 0402 or 0603	5
C6	PCT3685CT-ND	Panasonic/Digi-Key <sup>(1)</sup>	6.8 $\mu$ F, 20V Tantalum Electrolytic Capacitor, Size C	1
J1	111-0703-001	Johnson Components <sup>(2)</sup>	Black Banana Jack	1
J2	111-0702-001	Johnson Components <sup>(2)</sup>	Red Banana Jack	1
R1, R2	P51.1LCT-ND	Panasonic/Digi-Key <sup>(1)</sup>	50 $\Omega$ 1% Surface Resistor, Size 0402 or 0603	2
R3	04F6884	SMD <sup>(3)</sup>	0–10k $\Omega$ 3269 Series Mult-turn Trimmer Resistor, Size 0402	1
S1, S2 S3, S4, S5	142-0701-851	Johnson Components <sup>(2)</sup>	Jack Assembly End Launch SMA	5
TP1, TP2	TSW-101-07-S-S	Samtec <sup>(4)</sup>	1-Header Through Hole Terminal Strip	2
U1	<b>SY88932LL</b>	Micrel Semiconductor <sup>(5)</sup>	3.3V 3.2Gbps SONET/SDH Laser Driver with 50 $\Omega$ Input Termination	1

**Note 1.** Panasonic tel: 847-468-5624

**Note 2.** Johnson Components tel: 800-247-8256

**Note 3.** SMD tel: 852-2331-2776

**Note 4.** Samtec tel: 1-800-726832-9

**Note 5.** Micrel Semiconductor tel: 408-944-0800

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