DESIGN KIT AVAILABLE

DS3141/DS3142/DS3143/DS3144 Single/Dual/Triple/Quad DS3/E3 Framers

www.maxim-ic.com

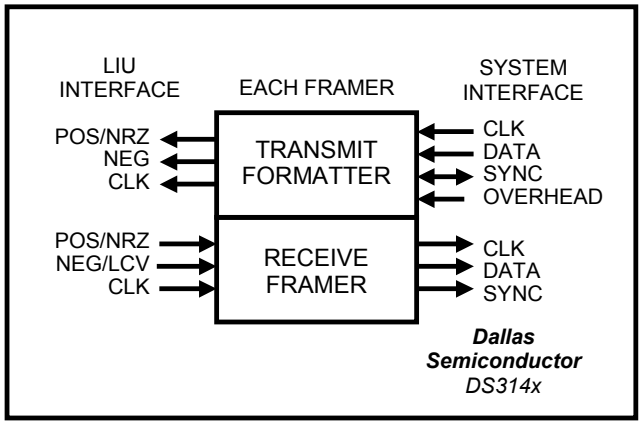
GENERAL DESCRIPTION

The DS3141, DS3142, DS3143, and DS3144 (DS314x) devices include all necessary circuitry to frame and format up to four separate DS3 or E3 channels. Each framer in these devices is independently configurable to support M23 DS3, C-Bit Parity DS3, or G.751 E3. The framers interface to a variety of line interface units (LIUs), microprocessor buses, and other system components without glue logic. Each DS3/E3 framer has its own HDLC controller, FEAC controller, and BERT, as well as full support for error detection and generation, performance monitoring, and loopbacks.

APPLICATIONS

SONET/SDH Muxes
PDH Muxes
Digital Cross-Connect Systems
Access Concentrators
ATM and Frame Relay Equipment
Routers

FUNCTIONAL DIAGRAM



FEATURES

- One/Two/Three/Four Independent DS3/E3 Framers on a Single Die
- Framing and Formatting to M23 DS3, C-Bit Parity DS3, and G.751 E3
- LIU Interface can be Binary (NRZ) or Dual-Rail (POS/NEG)
- B3ZS/HDB3 Encoder and Decoder
- Generate and Detect DS3/E3 Alarms
- Integrated HDLC Controller for Each Channel
- Integrated FEAC Controller for Each Channel
- Integrated Bit Error-Rate Tester (BERT) for Each Channel
- Large Performance-Monitoring Counters
- Line, Diagnostic, and Payload Loopbacks
- Externally Controlled Transmit Overhead Insertion Port
- Support External Timing or Loop-Timing
- Framers can be Powered Down When Not Used
- 8-Bit Processor Port Supports Muxed or Nonmuxed Bus Operation (Intel or Motorola)
- 3.3V Supply with 5V Tolerant I/O
- 144-Pin, 13mm x 13mm CSBGA Package
- IEEE 1149.1 JTAG Support

ORDERING INFORMATION

PART	NO. OF FRAMERS	TEMP RANGE	PIN-PACKAGE
DS3141	1	0°C to +70°C	144 CSBGA
DS3141N	1	-40°C to +85°C	144 CSBGA
DS3142	2	0°C to +70°C	144 CSBGA
DS3142	2	-40°C to +85°C	144 CSBGA
DS3143	3	0°C to +70°C	144 CSBGA
DS3143N	3	-40°C to +85°C	144 CSBGA
DS3144	4	0°C to +70°C	144 CSBGA
DS3144N	4	-40°C to +85°C	144 CSBGA

Pin Configurations appear at end of data sheet.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

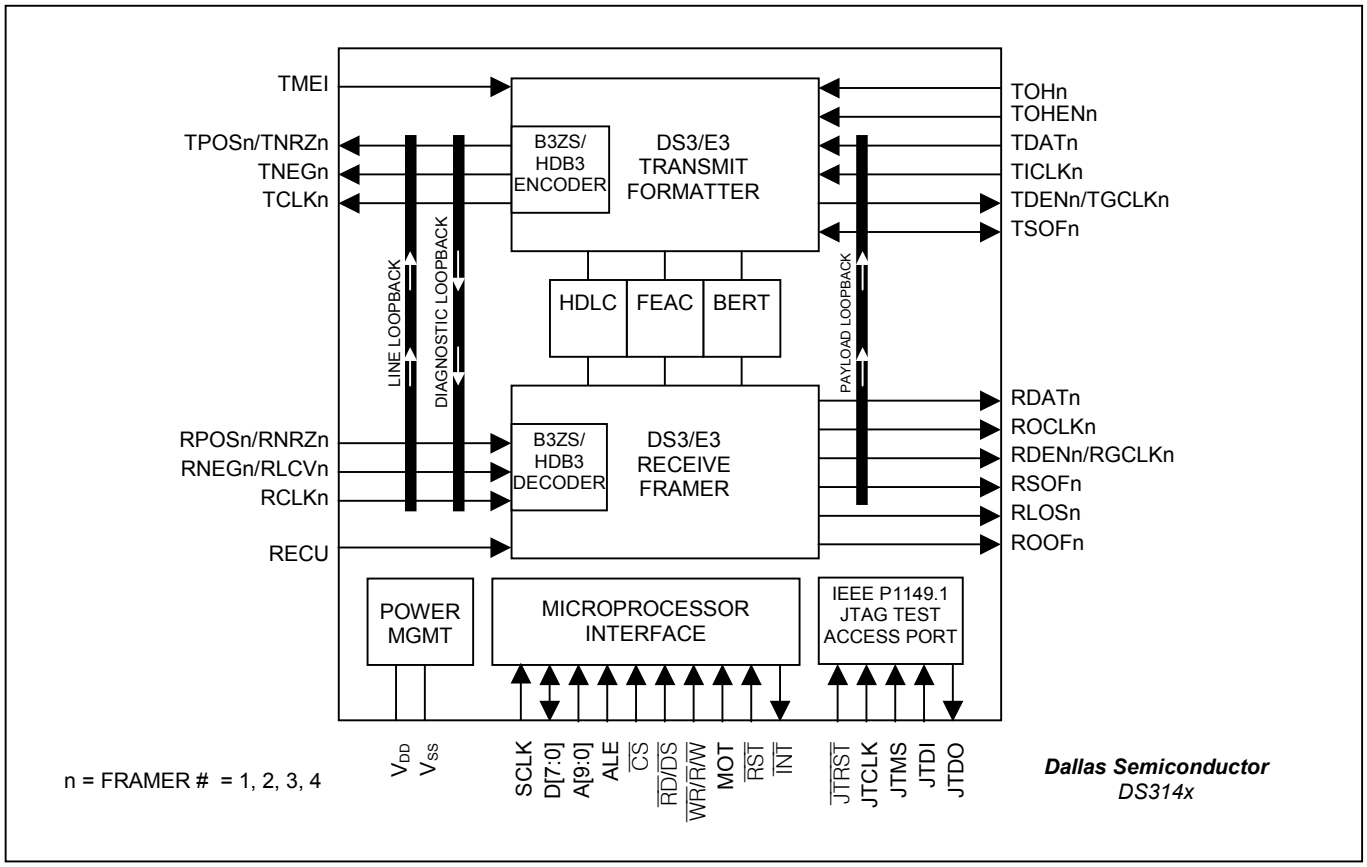
TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

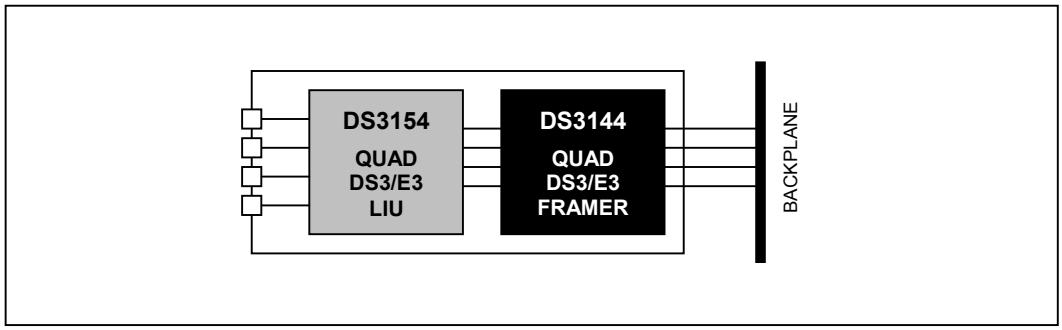
1. BLOCK DIAGRAM

Figure 1-1. Block Diagram



2. APPLICATION EXAMPLE

Figure 2-1. Application Example: 12-Port Unchannelized DS3/E3 Card



3. MAIN FEATURES

General

- LIU Interfaces can be Either Dual-Rail (POS/NEG/CLK) or Binary (DAT/CLK/LCV)
- Support Gapped 52MHz Clock Rates
- Optional B3ZS/HDB3 Encoder and Decoder
- Clock, Data, and Control Signals can be Inverted to Allow a Glueless Interface to Other Devices
- Detection of Loss-of-Transmit Clock and Loss-of-Receive Clock
- Manual or Automatic One-Second Update of Performance Monitoring Counters
- Each Framer can be Put Into Low-Power Standby Mode When Not Being Used

Receive Framer

- Frame Synchronization for M23 DS3, C-Bit Parity DS3, and G.751 E3
- Optional B3ZS/HDB3 Decoding
- Detects RAI, AIS, and DS3 Idle Signal
- Detects and Accumulates Bipolar Violations (BPV), Line-Code Violations (CVs), Excessive Zeros (EXZ), F-Bit Errors, M-Bit Errors, FAS Errors, P-Bit Parity Errors, CP-Bit Parity Errors, and Far-End Block Errors (FEBE)
- Detect Loss-of-Signal (LOS), Out-of-Frame (OOF), Severely Errored Frame Event (SEF), Change-of-Frame Alignment (COFA), Receipt of B3ZS/HDB3 Codewords, and DS3 Application ID Status
- E3 National Bit (Sn) is Forwarded to a Status Register Bit, the HDLC Controller, and the FEAC Controller

Transmit Formatter

- Frame Insertion for M23 DS3, C-Bit Parity DS3, and G.751 E3
- Optional B3ZS/HDB3 Encoding
- Clear-Channel Formatter Pass-Through Mode
- Generate RAI, AIS, and DS3 Idle Signals
- Automatic or Manual FEBE Insertion
- Support Automatic or Manual Insertion of BPVs, CVs, Excessive Zeros, F-Bit Errors, M-Bit Errors, FAS Errors, P-Bit Parity Errors, and CP-Bit Parity Errors
- E3 National Bit (Sn) can be Sourced from a Control Register, the HDLC Controller, or the FEAC Controller
- Any Overhead Bit Position can be Externally Overridden in the Transmit Formatter Using the Transmit Overhead Enable (TOHEN) and the Transmit Overhead Input (TOH). This Feature Enables External Control Over Unused Overhead Bits for Proprietary Signaling Applications.
- Optional Common Transmit Clock-Input Pin

HDLC Controller

- Designed to Handle Multiple LAPD Messages with Minimal Host Processor Intervention
- 256-Byte Receive and Transmit FIFOs are Large Enough to Handle the Three DS3 PMDL Messages (Path ID, Idle Signal ID, and Test Signal ID) that are Sent and Received Once per Second
- Handles All the Normal Layer 2 Tasks Such As Zero Stuffing/Destuffing, CRC and Abort Generation/Checking, Flag Generation/Detection, and Byte Alignment
- Programmable High and Low Watermarks for the Transmit and Receive FIFOs
- Terminates the Path Maintenance Data Link in DS3 C-Bit Parity mode and Optionally the Sn-Bit in E3 Mode

FEAC Controller

- Designed to Handle Multiple FEAC Codewords with Minimal Host Processor Intervention
- Receive FEAC Automatically Validates Incoming Codewords and Stores Them in a 4-Byte FIFO
- Transmit FEAC can be Configured to Send One Codeword, One Codeword Continuously, or Two Different Codewords Back-to-Back to Send DS3 Line Loopback Commands
- Terminates the FEAC Channel in DS3 C-Bit Parity Mode and Optionally the Sn Bit in E3 Mode

BERT

- Generates and Detects Pseudorandom Patterns 2^{15} - 1, 2^{20} - 1 (QRSS), 2^{23} - 1, and 2^{31} - 1 as well as Repetitive Patterns from 1 to 32 Bits in Length
- Supports Pattern Insertion/Extraction in Either Payload Only or Full Bandwidth
- Large 24-Bit Error Counter Allows Testing to Proceed for Long Periods Without Host Processor Intervention
- Errors can be Inserted in the Generated BERT Patterns for Diagnostic Purposes (Single Bit Errors or Specific Bit-Error Rates)

Loopback

- Diagnostic Loopback (Transmit to Receive)
- Line Loopback (Receive to Transmit)
- Payload Loopback

Microprocessor Interface

- Multiplexed or Nonmultiplexed 8-Bit Processor Port
- Intel and Motorola Bus Compatible
- Global Reset-Input Pin
- Global Interrupt-Output Pin

4. STANDARDS COMPLIANCE

Table 4-A. Applicable Telecommunications Standards

SPECIFICATION	TITLE
ANSI	
T1.107–1995	*Digital Hierarchy—Formats Specification*
T1.231–1997	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404–1994	*Network-to-Customer Installation—DS3 Metallic Interface Specification*
ITU–T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces*, 1991
G.751	*Digital Multiplex Equipment Operating at the Third-Order Bit Rate of 34,368kbps and the Fourth-Order Bit Rate of 139,264kbps and Using Positive Justification,* 1993
G.775	*Loss-of-Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria,* November 1994
G.823	*The Control of Jitter and Wander within Digital Networks that are Based on the 2048kbps Hierarchy*, 1993
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above*, October 1992
O.161	*In-Service Code Violation Monitors for Digital Systems*, 1984
IETF	
RFC 2469	*Definition of Managed Objects for the DS3/E3 Interface Type, Network Working Group Request for Comments*, January 1999
TELCORDIA	
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 1, December 1995
GR-820-CORE	*Generic Digital Transmission Surveillance*, Issue 1, November 1994
TR-TSY-000009	*Asynchronous Digital Multiplexes Requirements and Objectives*, Issue 1, May 1986
TR-TSY-000191	*Alarm Indication Signal Requirements and Objectives,* Issue 1, May 1986

5. PIN DESCRIPTION

5.1 Transmit Formatter LIU Interface Pins

NAME	TYPE	FUNCTION
TPOS/ TNRZ	O	Transmit Positive Data Output/Transmit NRZ Data Output. If BIN = 0 in the MC1 register, the LIU interface is in dual-rail (POS/NEG) mode. In this mode, the transmit formatter outputs the serial data stream in alternate mark inversion (AMI) format. TPOS = 1 signals an external LIU to drive a positive pulse on the line, while TNEG = 1 tells the LIU to drive a negative pulse on the line. If BIN = 1, the LIU interface is in binary (NRZ) mode. In this mode, the transmit formatter outputs the serial data stream in binary format on the TNRZ pin. TNRZ = 1 indicates a 1 in the data stream, while TNRZ = 0 indicates a 0. If TCLKI = 0 in the MC5 register, data is clocked out of the formatter on the rising edge of TCLK. If TCLKI = 1, data is clocked out on the falling edge of TCLK. MC5:TPOSH = 1 forces TPOS/TNRZ high. MC5:TPOSI = 1 inverts the polarity of TPOS/TNRZ. Setting both TPOSH = 1 and TPOSI = 1 forces TPOS/TNRZ low.
TNEG	O	Transmit Negative Data Output. If BIN = 0 in the MC1 register, the LIU interface is in dual-rail (POS/NEG) mode. In this mode, the transmit formatter outputs the serial data stream in AMI format. TPOS = 1 signals an external LIU to drive a positive pulse on the line, while TNEG = 1 tells the LIU to drive a negative pulse on the line. If BIN = 1, the LIU interface is in binary (NRZ) mode. In this mode the transmit formatter outputs the serial data stream in binary format on the TNRZ pin, and TNEG is driven low. If TCLKI = 0 in the MC5 register, data is clocked out of the formatter on the rising edge of TCLK. If TCLKI = 1, data is clocked out on the falling edge of TCLK. MC5:TNEGH = 1 forces TNEG high. MC5:TNEGI = 1 inverts the polarity of TNEG. Setting both TNEGH = 1 and TNEGI = 1 forces TNEG low.
TCLK	O	Transmit Clock Output. TCLK is used to clock data out of the transmit formatter on TPOS/TNEG (dual-rail LIU interface mode) or TNRZ (binary LIU interface mode). If TCLKI = 0 in the MC5 register, data is clocked out of the formatter on the rising edge of TCLK. If TCLKI = 1, data is clocked out on the falling edge of TCLK. TCLK is normally a buffered (and optionally inverted) version of TICLK. When either line loopback or payload loopback is active, TCLK is a buffered (and optionally inverted) version of RCLK. When a clock is not present on TICLK and MC1:LOTCMC = 1, TCLK is a buffered (and optionally inverted) version of RCLK.

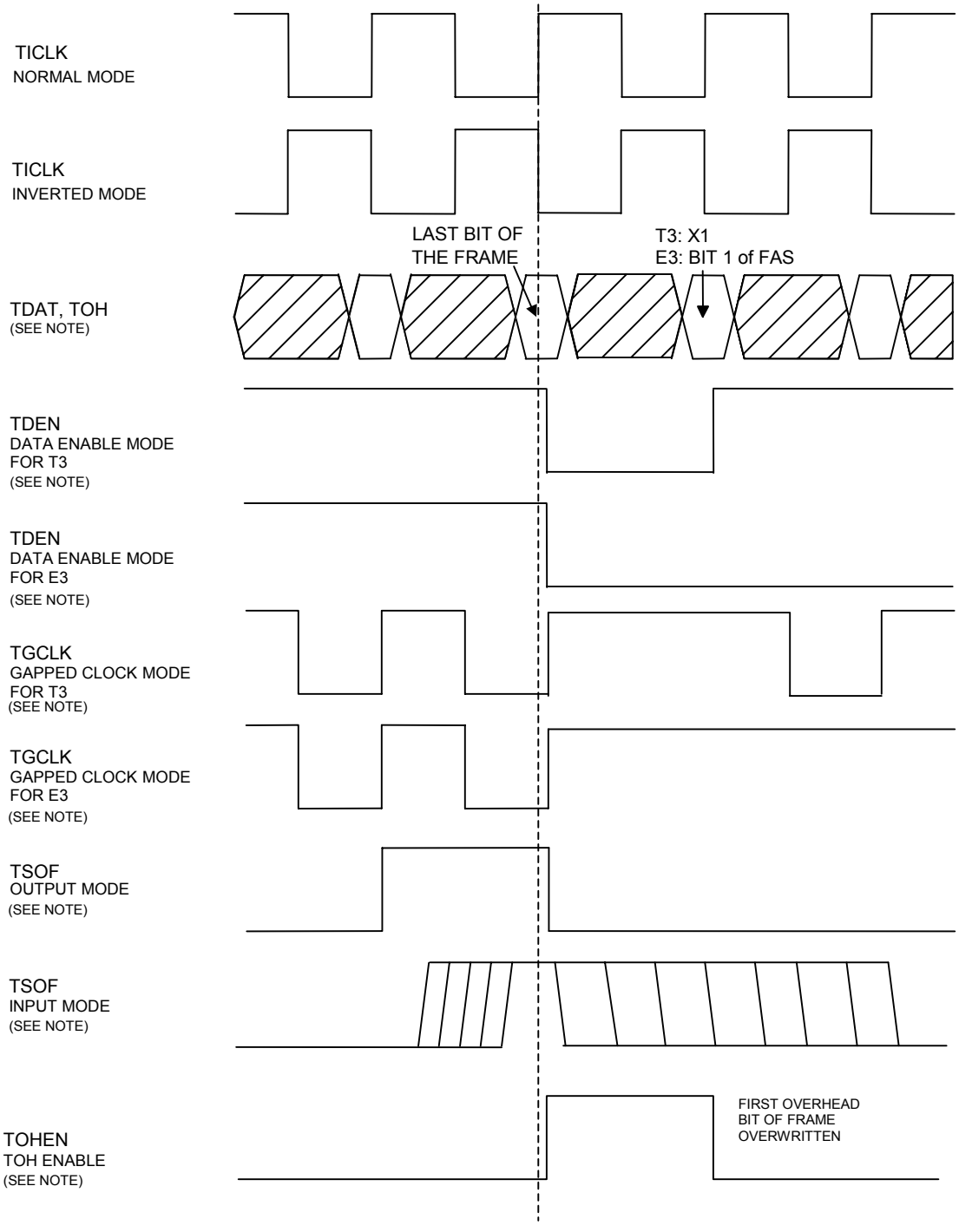
5.2 Receive Framer LIU Interface Pins

NAME	I/O	FUNCTION
RPOS/ RNRZ	I	Receive Positive Data Input/Receive NRZ Data Input. If BIN = 0 in the MC1 register, the LIU interface is in dual-rail (POS/NEG) mode. In this mode, the framer clocks in the serial data stream in AMI format. RPOS = 1 from an external LIU indicates a positive pulse was received on the line; RNEG = 1 from the LIU indicates a negative pulse was received on the line. If BIN = 1, the framer is in binary (NRZ) LIU interface mode. In this mode the framer clocks in the serial data stream in binary format on the RNRZ pin. RNRZ = 1 indicates a 1 in the data stream; RNRZ = 0 indicates a 0 in the data stream. If RCLKI = 0 in the MC5 register, data is clocked into the framer on the rising edge of RCLK. If RCLKI = 1, data is clocked in on the falling edge of RCLK. MC5:RPOSI = 1 inverts the polarity of RPOS/RNRZ.
RNEG/ RLCV	I	Receive Negative Data Input/Receive Line-Code Violation Input. If BIN = 0 in the MC1 register, the LIU interface is in dual-rail (POS/NEG) mode. In this mode, the framer clocks in the serial data stream in AMI format. RPOS = 1 from an external LIU indicates a positive pulse was received on the line, while RNEG = 1 from the LIU indicates a negative pulse was received on the line. If BIN = 1, the framer is in binary (NRZ) LIU interface mode. In this mode the framer clocks in the serial data stream in binary format on the RNRZ pin and line code violations on the RLCV pin. If RCLKI = 0 in the MC5 register, data is clocked into the framer on the rising edge of RCLK. If RCLKI = 1, data is clocked in on the falling edge of RCLK. MC5:RNEGI = 1 inverts the polarity of RNEG/RLCV. In binary LIU interface mode, when MC5:RNEGI = 0, the BPV counter (registers BPVCR1 and BPVCR2) counts RCLK cycles when RLCV = 1. When MC5:RNEGI = 1, the BPV counter counts RCLK cycles when RLCV = 0.
RCLK	I	Receive Clock Input. RCLK is used to clock data into the receive framer on RPOS/RNEG (dual-rail LIU interface mode) or RNRZ (binary LIU interface mode). If RCLKI = 0 in the MC5 register, data is clocked into the framer on the rising edge of RCLK. If RCLKI = 1, data is clocked in on the falling edge of RCLK. RCLK is normally accurate to within ±20ppm when sourced from an LIU, but the framer can also accept a gapped clock up to 52MHz on RCLK, such as those commonly sourced from ICs that map/demap DS3 and E3 to/from SONET/SDH.

5.3 Transmit Formatter System Interface Pins

NAME	TYPE	FUNCTION
TICLK	I	Transmit Input Clock. TICLK samples the TDAT, TDEN/TGCLK, TSOF, TOH, and TOHEN input pins. TICLK accepts a smooth clock or a gapped clock up to 52MHz. When the framer is connected to an LIU without a jitter attenuator, TICLK should be an ungapped, transmission-quality DS3 or E3 clock (±20ppm, low jitter) to meet the frequency accuracy and jitter requirements for transmission. The default active sampling edge of TICLK is the rising edge. To make the negative edge the active sampling edge, set MC3:TICLKI = 1.
TDAT	I	Transmit Data Input. In C-Bit Parity DS3 mode, payload bits are clocked into the transmit formatter on TDAT. In M23 DS3 mode and E3 mode, payload bits, stuff opportunity bits and C bits are clocked in on TDAT. TDAT is sampled on the active sampling edge of TICLK. The default active sampling edge of TICLK is the rising edge. To make the negative edge the active sampling edge, set MC3:TICLKI = 1. TDAT can be internally inverted by setting MC3:TDATI = 1.
TDEN/ TGCLK	O	Transmit Data Enable/Transmit Gapped Clock. The transmit formatter can be configured to either output a data enable (TDEN) or a gapped clock (TGCLK). In data enable mode, TDEN goes active when payload data should be made available on the TDAT input pin and inactive when the formatter is inserting framing overhead. In gapped clock mode, TGCLK acts as a demand clock for the TDAT input, toggling for each payload bit position and not toggling when the formatter is inserting framing overhead. In DS3 mode, overhead data is defined as the M bits, F bits, C bits, X bits, and P bits. In E3 mode, overhead data is defined as the FAS word, RAI bit, and Sn bit (bits 1 to 12). To configure the transmit formatter for data enable mode, set MC3:TDENMS = 0. To configure for gapped clock operation, set MC3:TDENMS = 1. TDEN is normally active high; to make TDEN active low, set MC3:TDENI = 1. TGCLK normally is the same polarity as TICLK; to invert TGCLK, set MC3:TDENI = 1. In the transmit pass-through mode (T3E3CR1:TPT = 1), TDEN/TGCLK continues to mark the payload positions in the original frame established before TPT was activated. This pin can also be made to output a constant transmit clock by setting MC2:TCCLK = 1. This constant clock is useful for certain applications that need to use the TOH and TOHEN pins during payload loopback.
TSOF	O/I	Transmit Start-of-Frame. TSOF indicates the DS3 or E3 frame boundary on the outgoing transmit data stream. When TSOFC = 1 in the MC3 register, TSOF is an output and pulses high for one TICLK cycle during the last bit of each DS3 or E3 frame. When TSOFC = 0, TSOF is an input and is sampled to set the transmit DS3 or E3 frame boundary. See Figure 5-1 for functional timing. Note that the reset default is for TSOF to be an input. Some applications require an external pullup or pulldown resistor on TSOF to keep it from floating during power-up and reset. TSOF is normally active high. Set MC3:TSOFI = 1 to make TSOF active low. If transmit pass-through (TPT) mode is enabled (T3E3CR1:TPT = 1) and TSOF is an output, TSOF continues to mark the original frame position that was established before TPT activation.
TOHEN	I	Transmit Overhead Enable. Together the TOHEN and TOH pins make a simple, general-purpose transmit-overwrite port. This port is usually used to overwrite overhead bit positions (such as unused C bits in C-Bit Parity mode), but payload bits can be overwritten as well. During any clock cycle in which TOHEN is active, the formatter sources the TOH pin rather than the TDAT pin or the internal overhead generation logic. In DS3 mode, parity is not recalculated if any payload bits are overwritten. TOHEN can be internally inverted by setting MC3:TOHENI = 1.
TOH	I	Transmit Overhead Data. Together the TOHEN and TOH pins make a simple, general-purpose transmit-overwrite port. This port is usually used to overwrite overhead bit positions (such as unused C bits in C-Bit Parity mode), but payload bits can be overwritten as well. During any clock cycle in which TOHEN is active, the formatter sources the TOH pin rather than the TDAT pin or the internal overhead generation logic. TOH can be inverted by setting MC3:TOHI = 1.
TMEI	I	Transmit Manual-Error Insert. This pin is used to manually control the insertion of errors in the DS3 or E3 frame structure or the line coding. This pin is enabled when MEIMS = 1 in the T3E3EIC register. A single error is normally inserted on the rising edge of TMEI. The other bits in the T3E3EIC register control which types of errors are inserted. All framers on the device share this pin.

Figure 5-1. Transmit Formatter Timing

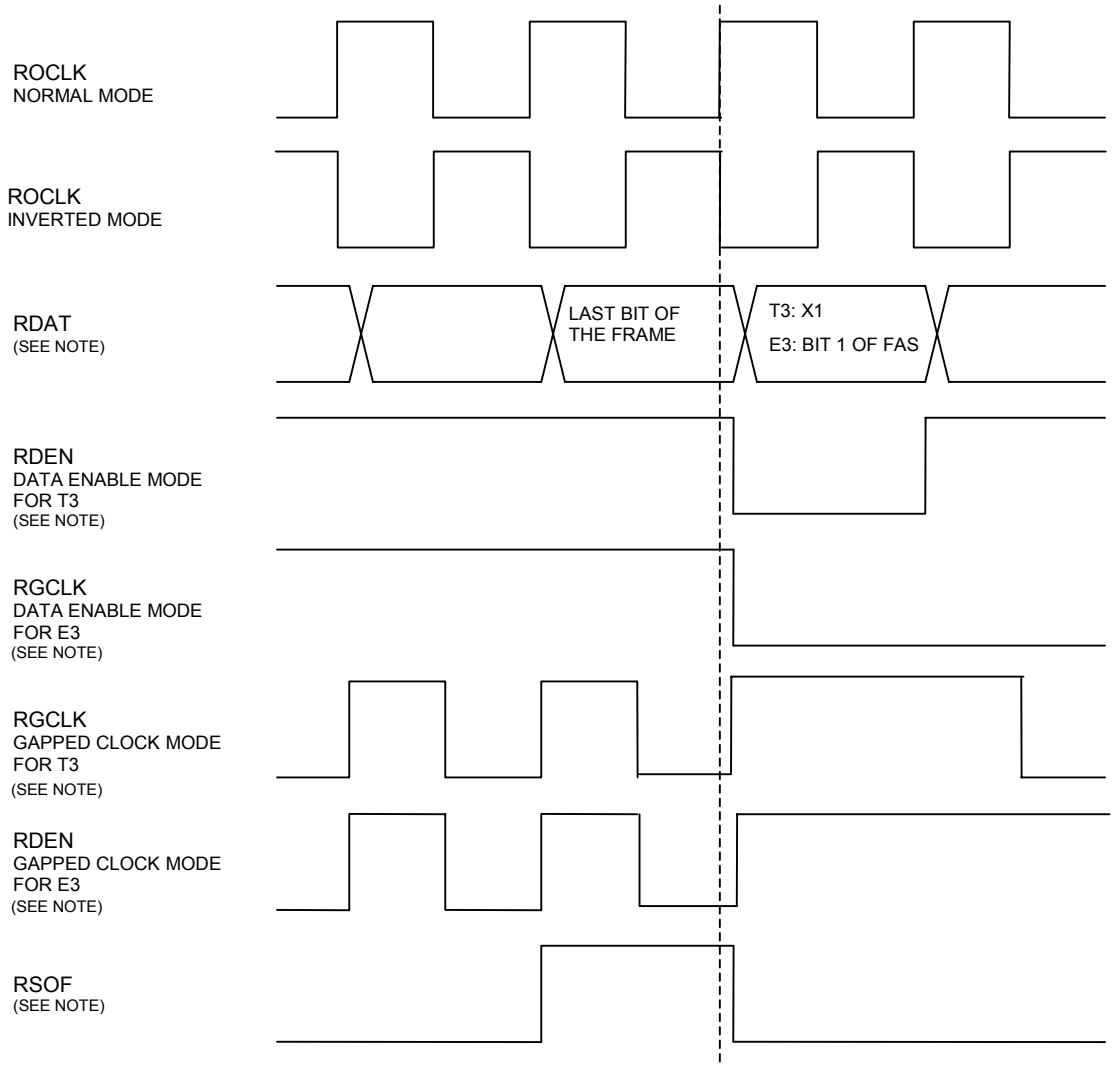


NOTE: TDAT, TDEN, TSOF, TOH, AND TOHN CAN BE INVERTED BY MASTER CONTROL REGISTER 3. THEY ARE SHOWN HERE AS NONINVERTED SIGNALS.

5.4 Receive Framer System Interface Pins

NAME	TYPE	FUNCTION
ROCLK	O	Receive Output Clock. ROCLK is used to clock data out of the receive framer on RDAT. ROCLK is normally a buffered (and optionally inverted) version of RCLK. When diagnostic loopback is active, ROCLK is a buffered (and optionally inverted) version of TICLK. If MC4:ROCLKI = 0, data is clocked out of the framer on the rising edge of ROCLK. If ROCLKI = 1, data is clocked out on the falling edge of ROCLK.
RDAT	O	Receive Data Output. The incoming DS3/E3 data stream is serially clocked out of the receive framer on the RDAT pin. RDAT is normally updated on the rising edge of ROCLK. To output data on the falling edge of ROCLK, set MC4:ROCLKI = 1. To internally invert RDAT, set MC4:RDATI = 1. To force RDAT high, set MC4:RDATH = 1. To force RDAT low, set MC4:RDATI = MC4:RDATH = 1.
RDEN/ RGCLK	O	Receive Data Enable/Receive Gapped Clock. The receive framer can be configured to either output a data enable (RDEN) or a gapped clock (RGCLK). In data enable mode, RDEN goes active when payload data is available on the RDAT output pin and inactive when overhead data is present on the RDAT pin. In gapped clock mode, RGCLK acts as a payload data clock for the RDAT output, toggling for each payload bit position and not toggling for each framing overhead bit position. In DS3 mode, overhead data is defined as the M bits, F bits, C bits, X bits, and P bits. In E3 mode, overhead data is defined as the FAS word, RAI bit, and Sn bit (bits 1 to 12). To configure the receive framer for data enable mode, set MC4:RDENMS = 0. To configure for gapped clock operation, set MC4:RDENMS = 1. RDEN is normally active high; to make RDEN active low, set MC4:RDENI = 1. RGCLK normally is the same polarity as RCLK; to invert RGCLK, set MC4:RDENI = 1.
RSOF	O	Receive Start of Frame. RSOF indicates the DS3 or E3 frame boundary on the incoming receive data stream. RSOF pulses high for one TICLK cycle during the last bit of each DS3 or E3 frameRSOF is normally active high. Set MC4:RSOFI = 1 to make RSOF active low.
RLOS	O	Receive Loss of Signal. RLOS goes high when the receive framer is in a loss-of-signal (LOS) state. It remains high as long as the LOS state persists and returns low when the framer exits the LOS state. See Table 7-E and Table 7-F for details on the set and clear criteria for this pin. LOS status is also available through the LOS status bit in the T3E3SR register.
ROOF	O	Receive Out of Frame. ROOF goes high when the receive framer is in an out-of-frame (OOF) state. It remains high as long as the OOF state persists and returns low when the framer synchronizes. See Table 7-E and Table 7-F for details on the set and clear criteria for this pin. OOF status is also available through the OOF status bit in the T3E3SR register.
RECU	I	Receive Error-Counter Update Strobe. Through the AECU control bit in the MC1 register, the device can be configured to use this asynchronous input to initiate an update of the internal error counters in all the framers on the device. A 0-to-1 transition on the RECU pin causes the device to load the error counter registers with the latest internal error counts. This signal must be returned low before a subsequent update of the error counters can occur. After toggling the RECU pin, the host processor must wait at least 100ns before reading the error counter registers to allow the device time to load the registers. This signal is logically ORed with the MECU control bit in MC1. If this signal is not used, it should be wired low.

Figure 5-2. Receive Framer Timing



NOTE: RDAT, RDEN, AND RSOF CAN BE INVERTED THROUGH MASTER CONTROL REGISTER 4. THEY ARE SHOWN HERE AS NONINVERTED SIGNALS.

5.5 CPU Bus Interface Pins

NAME	I/O	FUNCTION
MOT	I	Motorola Bus Mode Select. This pin controls whether the CPU bus operates in Intel mode or in Motorola mode. 0 = CPU bus is in Intel mode 1 = CPU bus is in Motorola mode
D[7:0]	I/O	CPU Bus Data. The host processor accesses the devices' internal registers through this bus. These pins are outputs during reads and inputs otherwise. D7 is the MSB; D0 is the LSB.
A[9:0]	I	CPU Bus Address. The host processor specifies the address of the internal register to be accessed by this bus. Pins A[9:8] specify the framer to be accessed. In multiplexed bus applications, the A[7:0] pins should be connected to the D[7:0] pins, and A[9:0] must have a valid register address when the ALE pin goes low. A9 is the MSB; A0 is the LSB.
ALE	I	CPU Bus Address Latch Enable. This pin controls the address latch for the A[9:0] inputs. When ALE is high, the latch is transparent. On the falling edge of ALE, the latch samples and holds the A[9:0] inputs. In nonmultiplexed bus applications, ALE should be wired high. In multiplexed bus applications, A[7:0] should be connected to D[7:0], and the falling edge of ALE latches the address.
$\overline{CS}$	I	CPU Bus Chip Select, Active Low. The host processor selects the device for read or write access by driving this pin low.
$\overline{WR}$ (R/$\overline{W}$)	I	CPU Bus Write Enable (CPU Bus Read/Write Select), Active Low. In Intel mode (MOT = 0), $\overline{WR}$ controls write accesses to the device. In Motorola mode (MOT = 1), R/$\overline{W}$ specifies whether a read or a write access is to occur.
$\overline{RD}$ ($\overline{DS}$)	I	CPU Bus Read Enable (CPU Bus Data Strobe), Active Low. In Intel mode (MOT = 0), $\overline{RD}$ controls read accesses to the device. In Motorola mode (MOT = 1), $\overline{DS}$ controls both read and write accesses to the device, while the R/$\overline{W}$ pin specifies the type of access.
$\overline{INT}$	O	CPU Bus Interrupt, Open Drain, Active Low. This pin is driven low by the device if one or more unmasked interrupt sources within the device are active. $\overline{INT}$ remains low until the interrupt is serviced or masked.
SCLK	I	System Clock. An ungapped clock with frequency between 33MHz and 52MHz must be provided to this pin to run certain logic in the CPU bus port. The use of this clock allows the transmit and receive clocks (TICLK and RCLK) to be gapped, if desired, without affecting the CPU bus timing. This pin can be connected to TICLK or RCLK if the signal on one of those pins is an ungapped clock.

5.6 JTAG Interface Pins

NAME	I/O	FUNCTION
JTCLK	I	JTAG IEEE 1149.1 Test Serial Clock. This pin is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, this pin should be wired high.
JTDI	I	JTAG IEEE 1149.1 Test Serial-Data Input (Internal 10kΩ Pullup). Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI should be left unconnected or driven high.
JTDO	O	JTAG IEEE 1149.1 Test Serial-Data Output. Test instructions are clocked out of this pin on the falling edge of JTCLK. If not used, JTDO should be left open-circuited. This pin is in tri-state mode after $\overline{JTRST}$ is activated.
$\overline{JTRST}$	I	JTAG IEEE 1149.1 Test Reset (Active Low, Internal 10kΩ Pullup). This pin is used to asynchronously reset the test access port controller. At power-up, $\overline{JTRST}$ must be driven low and then high. This action sets the device into the boundary scan bypass mode, allowing normal device operation. If boundary scan is not used, this pin should be held low.
JTMS	I	JTAG IEEE 1149.1 Test Mode Select (Internal 10kΩ Pullup). This pin is sampled on the rising edge of JTCLK and is used to place the test port into the various defined IEEE 1149.1 states. If not used, JTMS should be left unconnected or driven high.

5.7 Supply, Test, and Reset Pins

NAME	I/O	FUNCTION
$\overline{RST}$	I	Global Hardware Reset (Active Low). When this pin is driven low, all the framers in the device are reset and all the internal registers are forced to their default values. The device is held in the reset state as long as this pin is low. The clocks (TICLK and RCLK) must be stable and in spec before this pin is driven high. The device registers can be configured for operation after the reset is deactivated.
$\overline{TEST}$	I	Factory Test Enable (Active Low, Internal 10kΩ Pullup). This pin should be left open-circuited.
$\overline{HIZ}$	I	High-Z Control (Active Low, Internal 10kΩ Pullup). When this pin is low and $\overline{JTRST}$ is low, all outputs go to the high-impedance mode. This pin can be left open-circuited by the user.
V_{SS}		Digital Ground Reference. All V_{SS} pins should be wired together.
V_{DD}		Digital Positive Supply. 3.3V (±5%). All V_{DD} pins should be wired together.

6. REGISTERS

The framers are memory-mapped as follows:

Framer 1 (000h to 0FFh)
Framer 2 (100h to 1FFh)
Framer 3 (200h to 2FFh)
Framer 4 (300h to 3FFh)

The DS3141 uses address space 000h–0FFh and does not have address pins A[9:8]. The DS3142 uses address space 000h–1FFh, and does not have address pin A[9]. The DS3143 has three framers and uses address space 000h–2FFh. The DS3143 ignores any writes to 300h–3FFh, and returns 00h for any reads from 300h–3FFh. The DS3144 has four framers and uses address space 000h–3FFh.

Table 6-A shows the framer register map. Bits that are underlined are read-only bits. Bits that are marked "N/A" are undefined. Addresses that are not listed in Table 6–A are undefined. Undefined registers and bits are reserved for future enhancements and must always be written with logic 0 and ignored when read.

The device ID register is mapped into address 00h of every framer on the chip. Similarly, the ISR1 register is mapped into addresses 06h of every framer on the chip. All other registers are unique to each framer, including the reset (RST) register bit in MC1, which only resets the framer it is associated with, not the entire chip.

Table 6-A. Register Map

ADDR [7:0]	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
01h	MC1	LOTCMC	ZCSD	BIN	MECU	AECU	TUA1	DISABLE	RST
02h	MC2	OSTCS	TCCLK	N/A	N/A	N/A	DLB	LLB	PLB
03h	MC3	TDENMS	TSOFC	TOHENI	TOHI	TSOFI	TICLKI	TDATI	TDENI
04h	MC4	RDENMS	ROOFI	RLOSI	RDATH	RSOFI	ROCLKI	RDATI	RDENI
05h	MC5	RNEGI	RPOSI	RCLKI	TNEGH	TPOSH	TNEGI	TPOSI	TCLKI
06h	ISR1	N/A	N/A	N/A	N/A	INT4	INT3	INT2	INT1
08h	MSR	LORC	LOTC	T3E3SR	FEAC	HDLC	BERT	COVF	N/A
09h	MSRL	LORCL	LOTCL	N/A	N/A	N/A	N/A	COVFL	OSTL
0Ah	MSRIE	LORCIE	LOTCIE	T3E3SRIE	FEACIE	HDLCIE	BERTIE	COVFIE	OSTIE
10h	T3E3CR1	E3SNC1	E3SNC0	T3IDLE	TRAI	TAIS	TPT	CBEN	DS3M
11h	T3E3CR2	FRESYNC	N/A	TFEBE	AFEBED	ECC	FECC1	FECC0	E3CVE
12h	T3E3EIC	MEIMS	FBEIC1	FBEIC0	FBEI	T3CPBEI	T3PBEI	EXZI	BPVI
18h	T3E3SR	N/A	N/A	SEF	T3IDLE	RAI	AIS	OOF	LOS
19h	T3E3SRL	COFAL	N/A	SEFL	T3IDLEL	RAIL	AISL	OOFL	LOSL
1Ah	T3E3SRIE	COFAIE	N/A	SEFIE	T3IDLEIE	RAIIE	AISIE	OOFIE	LOSIE
1Bh	T3E3IR	RUA1	T3AIC	E3SN	N/A	EXZL	MBEL	FBEL	ZSCDL
20h	BPVCR1	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
21h	BPVCR2	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
22h	EXZCR1	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
23h	EXZCR2	EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8
24h	FECR1	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
25h	FECR2	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
26h	PCR1	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
27h	PCR2	PE14	PE14	PE13	PE12	PE11	PE10	PE9	PE8
28h	CPCR1	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
29h	CPCR2	CPE14	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8
2Ah	FEBECR1	FEBE7	FEBE6	FEBE5	FEBE4	FEBE3	FEBE2	FEBE1	FEBE0

ADDR [7:0]	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
2Bh	FEBECR2	FEBE15	FEBE14	FEBE13	FEBE12	FEBE11	FEBE10	FEBE9	FEBE8
30h	BCR1	BM1	BM0	BENA	TINV	RINV	RESYNC	TC	LC
31h	BCR2	N/A	PS2	PS1	PS0	RPL3	RPL2	RPL1	RPL0
32h	BCR3	N/A	N/A	N/A	N/A	EIB2	EIB1	EIB0	SBE
33h	BCR4	AWC7	AWC6	AWC5	AWC4	AWC3	AWC2	AWC1	AWC0
38h	BSR	N/A	N/A	RA1	RA0	N/A	BBCO	BECO	SYNC
39h	BSRL	N/A	N/A	RA1L	RA0L	BEDL	BBCOL	BECOL	SYNCL
3Ah	BSRIE	N/A	N/A	N/A	N/A	BEDIE	BBCOIE	BECOIE	SYNCIE
3Ch	BRPR1	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
3Dh	BRPR2	RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
3Eh	BRPR3	RP23	RP22	RP21	RP20	RP19	RP18	RP17	RP16
3Fh	BRPR4	RP31	RP30	RP29	RP28	RP27	RP26	RP25	RP24
40h	BBCR1	BBC7	BBC6	BBC5	BBC4	BBC3	BBC2	BBC1	BBC0
41h	BBCR2	BBC15	BBC14	BBC13	BBC12	BBC11	BBC10	BBC9	BBC8
42h	BBCR3	BBC23	BBC22	BBC21	BBC20	BBC19	BBC18	BBC17	BBC16
43h	BBCR4	BBC31	BBC30	BBC29	BBC28	BBC27	BBC26	BBC25	BBC24
44h	BBECR1	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
45h	BBECR2	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
46h	BBECR3	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
50h	HCR1	RHR	THR	RID	TID	TFS	TZSD	TCRCI	TCRCD
51h	HCR2	N/A	RHWMS2	RHWMS1	RHWMS0	N/A	TLWMS2	TLWMS1	TLWMS0
54h	HSR	N/A	N/A	N/A	N/A	RHWM	TLWM	N/A	N/A
55h	HSRL	ROVRL	RPEL	RPSL	RABTL	RHWML	TLWML	TUDRL	TENDL
56h	HSRIE	ROVRIE	RPEIE	RPSIE	RABTIE	RHWMIE	TLWMIE	TUDRIE	TENDIE
57h	HIR	N/A	N/A	REMPTY	TEMPTY	TFL3	TFL2	TFL1	TFL0
5Ch	RHDLC1	D7	D6	D5	D4	D3	D2	D1	D0
5Dh	RHDLC2	N/A	N/A	N/A	N/A	PS1	PS0	CBYTE	OBYTE
5Eh	THDLC1	D7	D6	D5	D4	D3	D2	D1	D0
5Fh	THDLC2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	TMEND
60h	FCR	N/A	N/A	N/A	N/A	N/A	RFR	TFS1	TFS0
61h	FSR	N/A	N/A	N/A	N/A	RFFE	RFI	RFCD	TFI
62h	FSRL	N/A	N/A	N/A	RFFOL	RFFNL	RFIL	RFCDL	TFIL
63h	FSRIE	N/A	N/A	N/A	RFFOIE	RFFNIE	RFIIE	RFCDIE	TFIIE
64h	TFEACA	N/A	N/A	TFCA5	TFCA4	TFCA3	TFCA2	TFCA1	TFCA0
65h	TFEACB	N/A	N/A	TFCB5	TFCB4	TFCB3	TFCB2	TFCB1	TFCB0
66h	RFEAC	N/A	N/A	RFF5	RFF4	RFF3	RFF2	RFF1	RFF0

Note 1. Bits that are underlined are read-only bits. Bits that are marked “N/A” are unused and undefined.
Note 2: Framer addresses 70h, 71h, and 7Ch–7Fh are factory test registers. During normal operation, these registers should not be written and should be ignored when read.

6.1 Status Register Description

There are two types of bits used to build the status and information registers. The real-time status register bit indicates the state of the corresponding signal at the time it was read. The latched status register bit is set when the corresponding signal changes state (low-to-high, high-to-low, or both, depending on the bit). The latched status bit is cleared when written with logic 1 and is not set again until the corresponding signal changes state again.

The following is example host-processor pseudocode that checks to see if the BERT SYNC status has changed:

```
If ((BSRL and 01h) neq 0) then      // SYNCL bit is set
      BSRL = 01h                          // Clear SYNCL bit only
      If ((BSR and 01h) neq 0) then       // BERT has changed to in sync
            -----
      Else                                // BERT has changed to out of sync
            -----
```

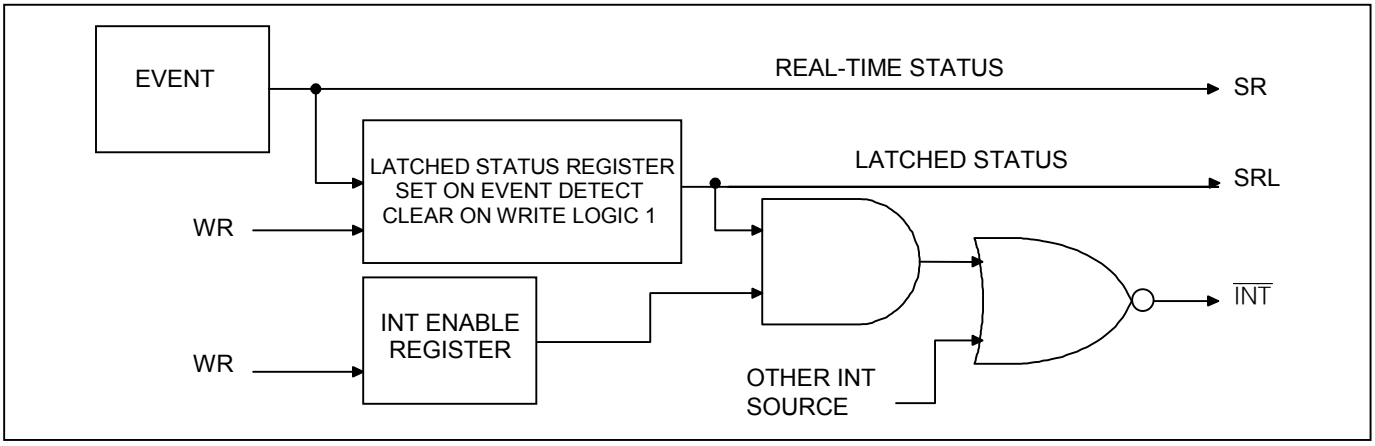
There are four suffixes used for status and information register names: SR for real-time status registers, SRL for latched status registers, SRIE for interrupt-enable registers, and IR for information registers. Latched status bits have the suffix “L” and interrupt-enable bits have the suffix “IE.” The bits in the SR, SRL, and SRIE registers are arranged such that related real-time status, latched status, and interrupt-enable bits are located in the same bit position in neighboring registers. For example, Table 6-B shows that the real-time status bit SYNC, the latched status bit SYNCL, and the interrupt-enable bit SYNCIE are all located in bit 0 of their respective registers (BSR, BSRL, and BSRIE).

When set, most latched status register bits can cause an interrupt on the $\overline{INT}$ pin if the corresponding interrupt-enable register bit is also set. Most latched status register bits have an associated real-time status register bit. Information registers can contain a mix of real-time and latched status bits, none of which can cause an interrupt.

Table 6-B. Status Register Set Example

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BSR	N/A	N/A	RA1	RA0	N/A	BBCO	BECO	SYNC
BSRL	N/A	N/A	RA1L	RA0L	BEDL	BBCOL	BECOL	SYNCL
BSRIE	N/A	N/A	N/A	N/A	BEDIE	BBCOIE	BECOIE	SYNCIE

Figure 6-1. Status Register Interrupt Flow



7. FUNCTIONAL DESCRIPTION

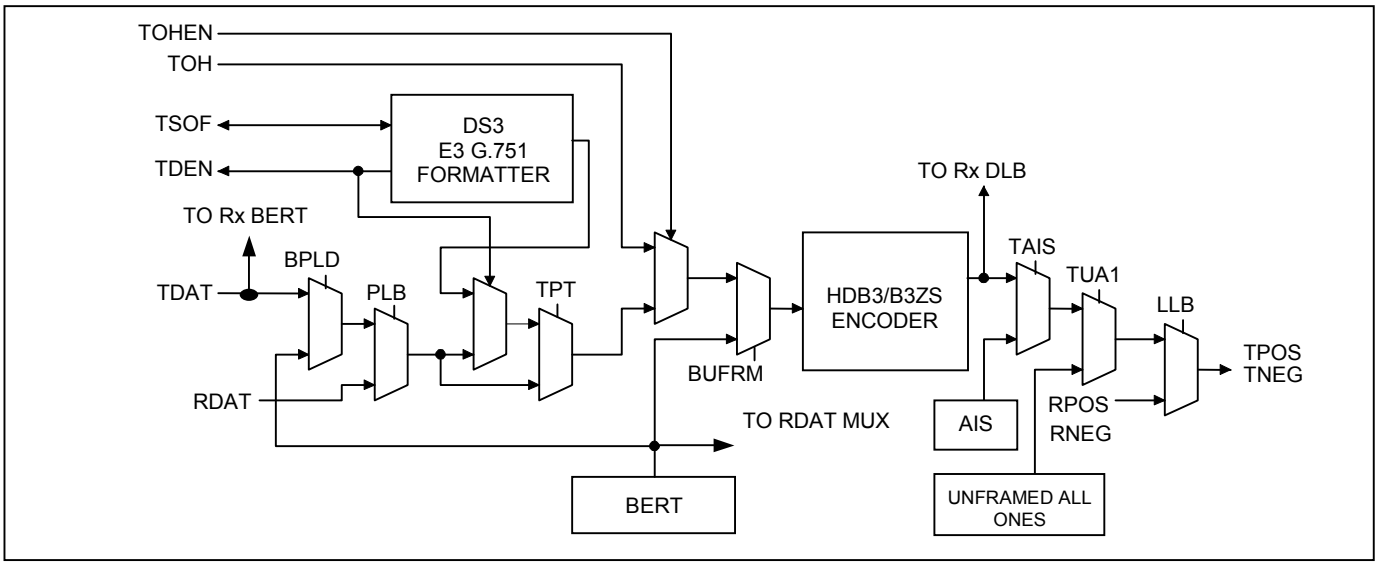
7.1 Pin Inversions and Force High/Low

Many of the input and output pins can be inverted and some output pins can be forced high or low (TPOS, TNEG, and RDAT). The inversion logic occurs at the input and output pads, but the JTAG control is not affected. The output pins that can be forced high can also be forced low by setting both the force high and invert bits for those pins.

7.2 Transmitter Logic

In the normal operating mode, the transmit section adds either DS3 or E3 framing overhead to the payload coming in on the TDAT input pin, then encodes the framed data in either HDB3 (E3 mode) or B3ZS (DS3 mode) and outputs the positive and negative pulse signals on TPOS and TNEG along with the transmit clock on TCLK. In line loopback mode (LLB bit in the MC2 register), TPOS, TNEG, and TCLK are buffered versions of RPOS, RNEG, and RCLK. In payload loopback mode (PLB bit in the MC2 register), payload is sourced from the receiver, framing overhead is added, and TCLK is a buffered version of RCLK. When a transmit alarm-indication signal (TAIS) is generated, an E3 or DS3 AIS signal is generated on TPOS/TNEG independent of the signal being internally generated. This allows the device to be in diagnostic loopback (DLB) internally and simultaneously send AIS to the transmit LIU interface. The TAIS is generated when either the TAIS bit in the T3E3CR1 register is set, or when there is a loss-of-transmit clock and the LOTCMC bit in the MC1 register is set. The same applies to the generation of unframed all ones when the TUA1 bit in the MC1 register is set. The TOHEN pin overwrites any of the data from TDAT, RDAT, the BERT (BPLD in BERT payload mode) or the transmit formatter with data from the TOH pin. The BERT signal in the unframed mode (BUFRM) is not overwritten with the TOH data. The data on TDAT (or RDAT in PLB mode) can be sent without adding internal overhead by setting the TPT (transmit pass-through) bit in the T3E3CR1 register. In transmit pass-through mode, data from TOH can still overwrite data from TDAT or RDAT.

Figure 7-1. Transmit Data Block Diagram

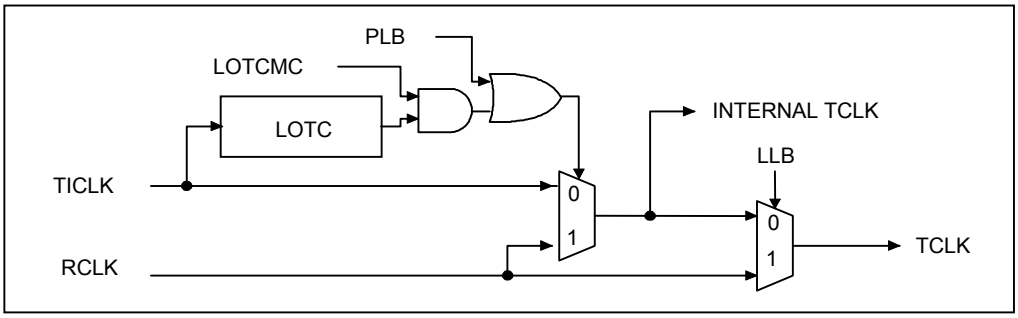


7.2.1 Transmit Clock

The transmit clock on the TICLK pin is monitored for activity, and, if the clock signal is inactive for several SCLK cycles, then the loss-of-transmit clock (LOTC) status is set. The LOTC status is then cleared when the TICLK signal is active for a few cycles.

The internal transmit clock can be sourced from either the TICLK pin or the RCLK pin, depending on LOTC status; the LOTCMC control bit (in the MC1 register); and payload loopback (PLB). Normally, the internal transmit clock is connected to the transmit-input clock (TICLK) pin. When LOTC is detected and the LOTCMC bit is set, the internal transmit clock is connected to the receive clock (RCLK). Also, if payload loopback (PLB) is selected, the internal transmit clock is connected to RCLK. The TCLK output pin is sourced from the internal transmit clock except in line loopback mode (LLB), where TCLK is always sourced from RCLK.

Figure 7-2. Transmit Clock Block Diagram



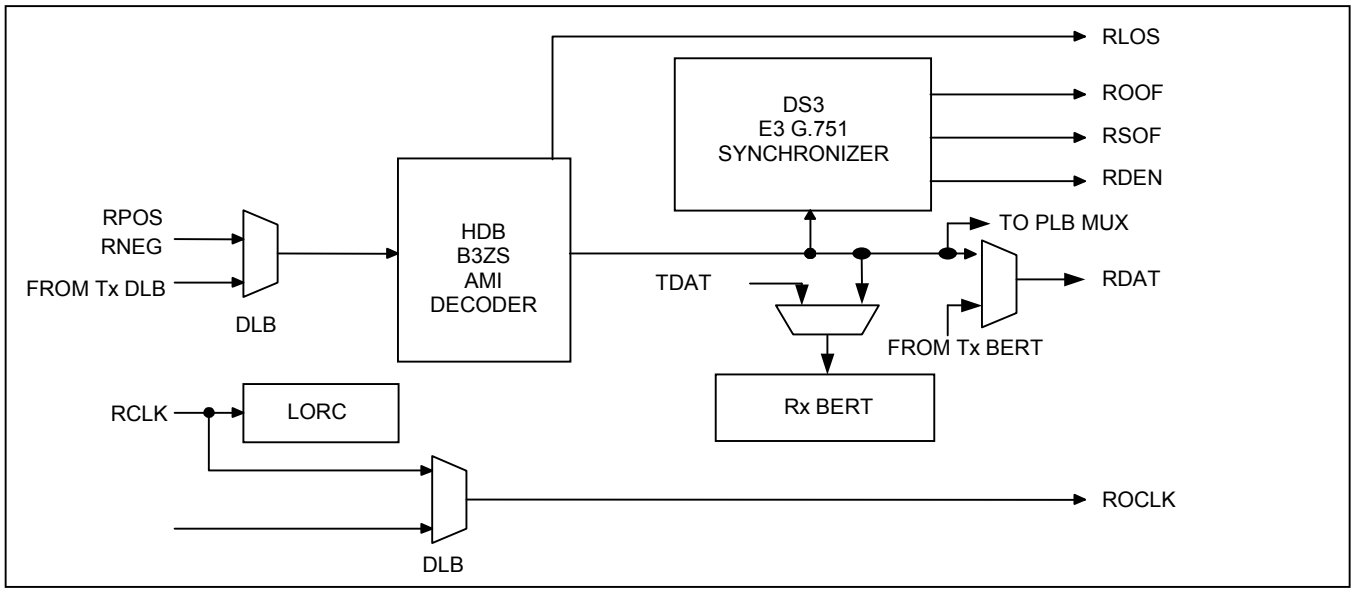
7.2.2 Loss-of-Clock Detection

The LOTC and LORC (loss-of-receive clock) status bits in the MSR register are set when the transmit (TICLK) and receive (RCLK) clocks are stopped, respectively. The clocks are monitored with the system clock (SCLK), which must be running for the loss-of-clock circuits to function properly. The LOTC and LORC status bits are set when TICLK or RCLK have been stopped high or low for between 9 and 21 clock periods (depending on SCLK frequency). The LOTC and LORC status bits are cleared after the device detects a few edges of the monitored clock.

7.3 Receiver Logic

In the normal operating mode, the signals on RPOS and RNEG are decoded as an HDB3 signal in E3 mode or as a B3ZS signal in DS3 mode and output on the RDAT pin. The input signal is monitored for loss-of-signal, bipolar violations, excessive zeroes, AIS, and unframed all ones, and after decoding, is sent to the BERT and synchronizer. When the synchronizer finds the framing pattern in the overhead bits, it clears the out-of-frame indication (ROOF) and aligns the start-of-frame (RSOF) and data-enable (RDEN) signals to the signal on RDAT. If the framing pattern is lost, then ROOF is set and the framing pattern is searched for again. While the framing pattern is being searched for, the RSOF and RDEN signals maintain the alignment with the last known position of the framing pattern. If a framing pattern is found in a new position, the RSOF and RDEN signals align with the new pattern position and the COFAL status bit is set in the T3E3SRL register. After reset, the RSOF and RDEN signals are generated, but have no relationship with any framing pattern until one is found. The signal on the ROOF pin can be monitored using the OOF bit in the T3E3SR register. When the diagnostic loopback mode is enabled using the DLB bit in the MC2 register, RCLK, RPOS, and RNEG are replaced with TICLK, TPOS, and TNEG. This allows the framer and synchronizer logic to be checked in order to isolate a problem in the system. The BERT can monitor either the payload or the entire signal for expected test patterns.

Figure 7-3. Receiver Block Diagram



7.4 Error Insertion

Errors can be created in the transmit overhead and line coding for diagnostic purposes. These errors do not cause any loss of data when created. The T3E3EIC error insertion register contains all the control bits to create errors. The TMEI input pin can also be used to create errors.

7.5 Loopbacks

7.5.1 Line Loopback

The line loopback connects the incoming DS3/E3 data (RCLK, RPOS/RNRZ, and RNEG inputs) directly back to the transmit side (TCLK, TPOS/TNRZ, and TNEG outputs). When this loopback is enabled, the incoming data continues to pass through the receive framer block, but the output data from the transmit formatter is ignored. See Figure 1-1 for a visual description of this loopback. Setting the LLB bit in the MC2 register activates the line loopback.

7.5.2 Diagnostic Loopback

The diagnostic loopback sends the outgoing DS3/E3 data directly back to the receive side. When this loopback is enabled, the incoming receive data at RCLK, RPOS, and RNEG is ignored. See Figure 1-1 for a visual description of this loopback. During diagnostic loopback the device can simultaneously generate AIS at the TCLK, TPOS, and TNEG outputs, while regular traffic is looped back to the receiver. This feature keeps the diagnostic signal that is being looped back from disturbing downstream equipment. Setting the DLB bit in the MC2 register activates the diagnostic loopback.

7.5.3 Payload Loopback

The payload loopback sends the DS3/E3 payload from the receive framer back to the transmit formatter. When this loopback is enabled, the incoming receive data continues to be present on the RDAT pin, but the transmit data on the TDAT pin is ignored. During payload loopback, the TSOF and TDEN signals are realigned to the receive frame, and the signals at TOH and TOHEN are active and can still overwrite any bit position. See Figure 1-1 for a visual description of this loopback. During payload loopback TSOF, TDEN, TOHEN, and TOH are aligned to the ROCLK signal. When PLB and DLB are both set, diagnostic loopback takes precedence. Setting the PLB bit in the MC2 register activates payload loopback.

7.5.4 BERT and Loopback Interaction

Table 7-A describes how the payload bits move through the device with various combinations of BERT modes and loopbacks active. The BERT mode is set in the BM[1:0] bits in the BCR1 register. The BERT is enabled when the BENA bit is set in the BCR1 register. Table 7-B describes how the overhead bits move through the device with various combinations of BERT modes and loopbacks active.

Table 7-A. BERT/Loopback Interaction—Payload Bits

CONFIGURATION BITS				BITS AT PAYLOAD BIT POSITIONS		
DLB	**LLB**	**PLB**	**BM [1:0]**	**From RPOS/RNEG To:**	**From TDAT To:**	**From BERT To:**
0	0	0	0X	BERT and RDAT	Not used	TPOS/TNEG
0	0	0	1X	Not used	BERT and TPOS/TNEG	RDAT
1	0	0	0X	Not used	Not used	TPOS/TNEG, BERT, and RDAT
1	0	0	1X	Not used	BERT and TPOS/TNEG	RDAT
0	1	0	0X	TPOS/TNEG, RDAT, and BERT	Not used	Not used
0	1	0	1X	TPOS/TNEG	BERT	RDAT
0	0	1	00	TPOS/TNEG and RDAT and BERT	Not used	Not used
0	0	1	01	RDAT and BERT	Not used	TPOS/TNEG
0	0	1	1X	TPOS/TNEG	BERT	RDAT

Table 7-B. BERT/Loopback Interaction—Overhead Bits

CONFIGURATION BITS				BITS AT OVERHEAD BIT POSITIONS			
DLB	LLB	PLB	BM [1:0]	From RPOS/RNEG To:	From TDAT To:	From Formatter To:	From BERT To:
0	0	0	00	Framer and RDAT	Not used (Note 1)	TPOS/TNEG	Not generated
0	0	0	01	Framer, RDAT and BERT	Not used	Not used	TPOS, TNEG
0	0	0	10	Framer and RDAT	Not used (Note 1)	TPOS/TNEG	Not generated
0	0	0	11	Framer	BERT (Note 2)	TPOS/TNEG	RDAT
1	0	0	00	Not used	Not used (Note 1)	TPOS/TNEG, Framer, and RDAT	Not generated
1	0	0	01	Not used	Not used	Not used	TPOS/TNEG, Framer, BERT, and RDAT
1	0	0	10	Not used	Not used (Note 1)	TPOS/TNEG, Framer, and RDAT	Not generated
1	0	0	11	Not used	BERT (Note 2)	TPOS/TNEG and Framer	RDAT
0	1	0	00	TPOS/TNEG, Framer, and RDAT	Not used	Not used	Not generated
0	1	0	01	TPOS/TNEG, Framer, RDAT, and BERT	Not used	Not used	Not used
0	1	0	10	TPOS/TNEG, Framer, and RDAT	Not used	Not used	Not generated
0	1	0	11	TPOS/TNEG and Framer	BERT (Note 2)	Not used	RDAT
0	0	1	00	Framer and RDAT	Not used (Note 1)	TPOS/TNEG	Not generated
0	0	1	01	Framer, RDAT, and BERT	Not used	Not used	TPOS/TNEG
0	0	1	10	Framer and RDAT	Not used (Note 1)	TPOS/TNEG	Not generated
0	0	1	11	Framer	BERT (Note 2)	TPOS/TNEG	RDAT

Note 1: In M23 mode or E3 mode, the transmit formatter sources the C bits from the appropriate bit positions of the TDAT data stream.
Note 2: When BM[1:0] = 11, the BERT expects a full-bandwidth (payload plus overhead) pattern to come in on the TDAT pin. In M23 mode or E3 mode with BM[1:0] = 11, the transmit formatter sources the C bits from the appropriate bit positions of the TDAT data stream, even though those bit positions are actually part of the full-bandwidth BERT pattern.

7.6 Common and Line Interface Registers

This section describes the registers responsible for top-level configuration, control, and status of each framer, including resets, clocks, pin controls, and line interface functions.

Table 7-C. Common Line Interface Register Map

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
01h	MC1	LOTCMC	ZCSD	BIN	MECU	AECU	TUA1	DISABLE	RST
02h	MC2	OSTCS	TCCLK	N/A	N/A	N/A	DLB	LLB	PLB
03h	MC3	TDENMS	TSOFC	TOHENI	TOHI	TSOFI	TICLKI	TDATI	TDENI
04h	MC4	RDENMS	ROOFI	RLOSI	RDATH	RSOFI	ROCLKI	RDATI	RDENI
05h	MC5	RNEGI	RPOSI	RCLKI	TNEGH	TPOSH	TNEGI	TPOSI	TCLKI
06h	ISR1	N/A	N/A	N/A	N/A	INT4	INT3	INT2	INT1
08h	MSR	LORC	LOTC	T3E3	FEAC	HDLC	BERT	COVF	N/A
09h	MSRL	LORCL	LOTCL	N/A	N/A	N/A	N/A	COVFL	OSTL
0Ah	MSRIE	LORCIE	LOTCIE	T3E3IE	FEACIE	HDLCIE	BERTIE	COVFIE	OSTIE

Register Name: **ID**
Register Description: **ID Register**
Register Address: **00h**

Bit #	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Default	—	—	—	—	—	—	—	—

This register is a global resource and is mapped into address 00h in every framer in the device.

Bits 0 to 7: Device ID (ID[7:0]). Read-only. Contact the factory for details on the meaning of the ID bits.

Register Name: **MC1**
Register Description: **Master Configuration Register 1**
Register Address: **01h**

Bit #	7	6	5	4	3	2	1	0
Name	LOTCMC	ZCSD	BIN	MECU	AECU	TUA1	DISABLE	RST
Default	0	0	0	0	0	1	0	0

Bit 0: Framer Reset (RST). When this bit is set to logic 1, it forces all the internal registers in the framer (except this RST bit) to their default state. Only the framer associated with this register is reset. RST must be high for a minimum of 100ns and then returned low. This register bit is logically ORed with the $\overline{RST}$ pin.

0 = normal operation
1 = force all internal registers to their default values

Bit 1: Framer Disable (DISABLE). Setting this bit disables the framer by stopping all clocks. This reduces the power the framer requires. After the framer is enabled again by clearing this bit, the RST bit must be toggled to initialize the framer again. Toggling the RST bit when DISABLE = 1 automatically enables the framer again.

0 = enable framer
1 = disable framer

Bit 2: Transmit Unframed All Ones (TUA1). Enables the transmission of an unframed all-ones pattern on TPOS/TNEG or TNRZ. This pattern is sometimes called physical AIS.

0 = disable transmission of unframed all ones
1 = enable transmission of unframed all ones (reset default value)

Bit 3: Automatic Error-Counters Update Defeat (AECU). When this bit is logic 0, the device automatically updates the DS3/E3 performance error counters on an internally created 1-second boundary based on the RCLK or TCLK signal, depending on the OSTCS control bit. The host processor is notified of the update through the setting of the OST status bit in the MSRL register. In this mode, the host processor has a full 1-second period to retrieve the error count information before it is overwritten with the next update. When this bit is set high, the device disables the automatic 1-second update and enables a manual update mode. In the manual update mode, the device relies on either the RECU hardware input signal or the MECU control bit to update the error counters. The RECU hardware input signal and MECU control bit are logically ORed and therefore a 0-to-1 transition on either initiates an error counter update. After either the RECU signal or MECU bit has toggled, the host processor must wait at least 100ns before reading the error counters to allow the device time to complete the update.

0 = enable the automatic update mode and disable the manual update mode
1 = disable the automatic update mode and enable the manual update mode

Bit 4: Manual Error-Counter Update (MECU). A 0-to-1 transition on this bit causes the device to update the performance error counters. This bit is ignored if the AECU control bit is logic 0. This bit must be cleared and set again for a subsequent update. This bit is logically ORed with the RECU input pin.

Bit 5: DS3/E3 POS/NEG Binary Mode Select (BIN). Selects the mode of the LIU interface signals.

0 = dual-rail mode (data on TPOS/TNEG and RPOS/RNEG)
1 = binary NRZ mode (data on TNRZ and RNRZ with line-code violation pulses on RLCV)

Bit 6: Zero Code Suppression Disable (ZCSD). When BIN = 1, zero code suppression is automatically disabled and ZCSD has no effect.

0 = enable the B3ZS/HDB3 encoder and decoder; coding is AMI with zero substitution
1 = disable the B3ZS/HDB3 encoder and decoder; coding is AMI without zero substitution

Bit 7: Loss-of-Transmit Clock Mux Control (LOTCMC). The device can detect if the TICLK fails to transition. If this bit is logic 0, the device takes no action (other than setting the LOTC status bit) when the TICLK fails to transition. If this bit is logic 1, when TICLK fails to transition the device automatically switches the transmitter to the input receive clock (RCLK) and transmits AIS.

0 = do not switch the transmitter to RCLK if TICLK fails to transition
1 = automatically switch the transmitter to RCLK and transmit AIS if TICLK fails to transition

Register Name: **MC2**
Register Description: **Master Configuration Register 2**
Register Address: **02h**

Bit #	7	6	5	4	3	2	1	0
Name	OSTCS	TCCLK	N/A	N/A	N/A	DLB	LLB	PLB
Default	0	0	—	—	—	0	0	0

Bit 0: Payload Loopback Enable (PLB). When payload loopback is enabled, the transmit formatter operates from the receive clock (rather than TICLK) and sources DS3/E3 payload bits from the receive data stream rather than from the TDAT input pin. Receive data is still available on the RDAT output pin during payload loopback. See Figure 1-1 for a visual description of this loopback.

0 = disable payload loopback
1 = enable payload loopback

Bit 1: Line Loopback Enable (LLB). Line loopback connects the TPOS, TNEG, and TCLK output pins to the RPOS, RNEG, and RCLK input pins. When line loopback is enabled, the receive framer continues to process the incoming receive data stream and present it on the RDAT pin; the output of the transmit formatter is ignored. Line loopback and diagnostic loopback can be active at the same time to support simultaneous local and far-end loopbacks. See Figure 1-1 for a visual description of this loopback.

0 = disable line loopback
1 = enable line loopback

Bit 2: Diagnostic Loopback Enable (DLB). When diagnostic loopback is enabled, the receive framer sources data from the transmit formatter rather than the RCLK, RPOS, and RNEG input pins. Transmit data is sourced prior to transmit AIS generation, unframed all-ones generation, TCLK/TPOS/TNEG pin inversion, and TPOS/TNEG force-high logic. This allows the device to transmit AIS or unframed all ones to the far end while locally looping back the actual transmit data stream, which could be test patterns or other traffic that should not be sent to the far end. See Figure 1-1 for a visual description of this loopback.

0 = disable diagnostic loopback
1 = enable diagnostic loopback

Bit 6: Transmit Constant Clock Select (TCCLK). When TCCLK is set to logic 1, the device outputs a constant transmit clock on the TDEN/TGCLK pin instead of a data enable or gapped clock. This bit has precedence over the TDENMS bit in register MC3. The pin can still be inverted by MC3:TDENI.

0 = the function of the TDEN/TGCLK pin is controlled by TDENMS control bit
1 = the TDEN/TGCLK pin is a constant transmit clock output

Bit 7: One-Second Timer Clock Select (OSTCS). This control bit selects the clock source for the internal one-second timer.

0 = use RCLK
1 = use TICLK

Register Name: **MC3**
Register Description: **Master Configuration Register 3**
Register Address: **03h**

Bit #	7	6	5	4	3	2	1	0
Name	TDENMS	TSOFC	TOHENI	TOHI	TSOFI	TICLKI	TDATI	TDENI
Default	0	0	0	0	0	0	0	0

Bit 0: TDEN Invert Enable (TDENI)
0 = do not invert the TDEN/TGCLK signal (normal mode)
1 = invert the TDEN/TGCLK signal (inverted mode)

Bit 1: TDAT Invert Enable (TDATI)
0 = do not invert the TDAT signal (normal mode)
1 = invert the TDAT signal (inverted mode)

Bit 2: TICLK Invert Enable (TICLKI)
0 = do not invert the TICLK signal (normal mode)
1 = invert the TICLK signal (inverted mode)

Bit 3: TSOF Invert Enable (TSOFI)
0 = do not invert the TSOF signal (normal mode)
1 = invert the TSOF signal (inverted mode)

Bit 4: TOH Invert Enable (TOHI)
0 = do not invert the TOH signal (normal mode)
1 = invert the TOH signal (inverted mode)

Bit 5: TOHEN Invert Enable (TOHENI)
0 = do not invert the TOHEN signal (normal mode)
1 = invert the TOHEN signal (inverted mode)

Bit 6: Transmit Start-of-Frame I/O Control (TSOFC). When this bit is logic 1, the TSOF pin is an output and pulses for the last TICLK cycle of each frame. When this bit is 0, the TSOF pin is an input, and the device uses it to determine the frame boundaries. See Figure 5-1 for functional timing information.
0 = TSOF is an input (reset default as input)
1 = TSOF is an output

Bit 7: Transmit Data-Enable Mode Select (TDENMS). When this bit is logic 0, the TDEN/TGCLK output has the TDEN (data enable) function. TDEN asserts during payload bit times and de-asserts during overhead bit times. When this bit is logic 1, TDEN/TGCLK has the TGCLK (gapped clock) function. TGCLK pulses during payload bit times and is suppressed during overhead bit times. The TCCLK control bit in the MC2 register has precedence over this control bit. See Figure 5-1 for functional timing information.
0 = TDEN (data enable) mode
1 = TGCLK (gapped clock) mode

Register Name: **MC4**
Register Description: **Master Configuration Register 4**
Register Address: **04h**

Bit #	7	6	5	4	3	2	1	0
Name	RDENMS	ROOFI	RLOSI	RDATH	RSOFI	ROCLKI	RDATI	RDENI
Default	0	0	0	1	0	0	0	0

Bit 0: RDEN Invert Enable (RDENI)
0 = do not invert the RDEN signal (normal mode)
1 = invert the RDEN signal (inverted mode)

Bit 1: RDAT Invert Enable (RDATI)
0 = do not invert the RDAT signal (normal mode)
1 = invert the RDAT signal (inverted mode)

Bit 2: ROCLK Invert Enable (ROCLKI)
0 = do not invert the ROCLK signal (normal mode)
1 = invert the ROCLK signal (inverted mode)

Bit 3: RSOF Invert Enable (RSOFI)
0 = do not invert the RSOF signal (normal mode)
1 = invert the RSOF signal (inverted mode)

Bit 4: RDAT Force High (RDATH). This bit is set to logic 1 at reset, which puts an all-ones signal on the RDAT pin. This pin should be cleared once the device has framed to a valid signal. The RDAT pin can be forced low by setting both the RDATH and RDATI control bits.
0 = do not force RDAT high (normal mode)
1 = force RDAT high (default reset mode)

Bit 5: RLOS Invert Enable (RLOSI)
0 = do not invert the RLOS signal (normal mode)
1 = invert the RLOS signal (inverted mode)

Bit 6: ROOF Invert Enable (ROOFI)
0 = do not invert the ROOF signal (normal mode)
1 = invert the ROOF signal (inverted mode)

Bit 7: Receive Data-Enable Mode Select (RDENMS). When this bit is logic 0, the RDEN/RGCLK output has the RDEN (data enable) function. RDEN asserts during payload bit times and de-asserts during overhead bit times. When this bit is logic 1, RDEN/RGCLK has the RGCLK (gapped clock) function. RGCLK pulses during payload bit times and is suppressed during overhead bit times. See Figure 5-2 for timing information.
0 = RDEN (data enable) mode
1 = RGCLK (gapped clock) mode

Register Name: **MC5**
Register Description: **Master Configuration Register 5**
Register Address: **05h**

Bit #	7	6	5	4	3	2	1	0
Name	RNEGI	RPOSI	RCLKI	TNEGH	TPOSH	TNEGI	TPOSI	TCLKI
Default	0	0	0	0	0	0	0	0

Bit 0: TCLK Invert Enable (TCLKI)
0 = do not invert the TCLK signal (normal mode)
1 = invert the TCLK signal (inverted mode)

Bit 1: TPOS/TNRZ Invert Enable (TPOSI)
0 = do not invert the TPOS/TNRZ signal (normal mode)
1 = invert the TPOS/TNRZ signal (inverted mode)

Bit 2: TNEG Invert Enable (TNEGI)
0 = do not invert the TNEG signal (normal mode)
1 = invert the TNEG signal (inverted mode)

Bit 3: TPOS/TNRZ Force-High Enable (TPOSH). The TPOS/TNRZ pin can be forced low by setting both the TPOSH and TPOSI control bits.
0 = allow normal transmit data to appear at the TPOS/TNRZ pin (normal mode)
1 = force the TPOS/TNRZ signal high (force high mode, can be inverted)

Bit 4: TNEG Force-High Enable (TNEGH). The TNEG pin can be forced low by setting both the TNEGH and TNEGI control bits.
0 = allow normal transmit data to appear at the TNEG pin (normal mode)
1 = force the TNEG signal high (force high mode, can be inverted)

Bit 5: RCLK Invert Enable (RCLKI)
0 = do not invert the RCLK signal (normal mode)
1 = invert the RCLK signal (inverted mode)

Bit 6: RPOS/RNRZ Invert Enable (RPOSI)
0 = do not invert the RPOS/RNRZ signal (normal mode)
1 = invert the RPOS/RNRZ signal (inverted mode)

Bit 7: RNEG/RLCV Invert Enable (RNEGI)
0 = do not invert the RNEG/RLCV signal (normal mode)
1 = invert the RNEG/RLCV signal (inverted mode)

Register Name: **ISR1**
Register Description: **Interrupt Status Register 1**
Register Address: **06h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	INT4	INT3	INT2	INT1
Default	—	—	—	—	—	—	—	—

This register is a global resource and is mapped into address 06h in every framer in the device. In both interrupt-based and polling-based device servicing strategies, the host processor should read this register first to determine which framers require servicing.

Bit 0: Interrupt 1 (INT1). This bit is set when framer 1 is driving the $\overline{INT}$ pin.

Bit 1: Interrupt 2 (INT2). This bit is set when framer 2 is driving the $\overline{INT}$ pin.

Bit 2: Interrupt 3 (INT3). This bit is set when framer 3 is driving the $\overline{INT}$ pin.

Bit 3: Interrupt 4 (INT4). This bit is set when framer 4 is driving the $\overline{INT}$ pin.

7.6.1 Master Status Register (MSR)

The master status register (MSR) is a special status register that helps the host processor quickly locate changes in device status. Each major block in the framer has a status bit in the MSR. When an alarm or event occurs in one of these blocks, the device can be configured to set the appropriate bit in the MSR. The latched status bits in the MSRL can also cause a hardware interrupt to occur. In both interrupt-based and polling-based device servicing strategies, the host processor should read the ISR1 register to determine which framers need service and then read the MSRL register of each framer that needs service to determine which blocks within the framer need service.

Register Name: **MSR**
Register Description: **Master Status Register**
Register Address: **08h**

Bit #	7	6	5	4	3	2	1	0
Name	LORC	LOTC	T3E3	FEAC	HDLC	BERT	COVF	N/A
Default	—	—	—	—	—	—	—	—

Bit 1: Counter Overflow Event (COVF). This real-time status bit is set to 1 if any of the error counters saturate (the error counters saturate when full). This bit is cleared when the error counters are cleared. The error counters are discussed in Section 7.8.

Bit 2: Change in BERT Status (BERT). This real-time status bit is set when any of the bits in the BSRL register are set and the corresponding bits in the BSRIE interrupt-enable register are set. This bit is cleared when the latched status bits in the BSRL register are cleared or the interrupt-enable bits in the BSRIE register are cleared. The setting of this status bit can cause a hardware interrupt to occur if the BERTIE bit in the MSRIE register is set to 1. The interrupt is cleared when this bit is cleared or the interrupt-enable bit in the MSRIE register is cleared.

Bit 3: Change in HDLC Status (HDLC). This real-time status bit is set when any of the bits in the HSRL register are set and the corresponding bits in the HSRIE interrupt-enable register are set. This bit is cleared when the latched status bits in the HSRL register are cleared or the interrupt-enable bits in the HSRIE register are cleared. The setting of this status bit can cause a hardware interrupt to occur if the HDLCIE bit in the MSRIE register is set to 1. The interrupt is cleared when this bit is cleared or the interrupt-enable bit in the MSRIE register is cleared.

Bit 4: Change in FEAC Status (FEAC). This real-time status bit is set when any of the bits in the FSRL register are set and the corresponding bits in the FSRIE interrupt-enable register are set. This bit is cleared when the latched status bits in the FSRL register are cleared or the interrupt-enable bits in the FSRIE register are cleared. The setting of this status bit can cause a hardware interrupt to occur if the FEACIE bit in the MSRIE register is set to 1. The interrupt is cleared when this bit is cleared or the interrupt-enable bit in the MSRIE register is cleared.

Bit 5: Change in DS3/E3 Framer Status (T3E3). This real-time status bit is set when any of the bits in the T3E3SRL register are set and the corresponding bits in the T3E3SRIE interrupt-enable register are set. This bit is cleared when the latched status bits in the T3E3SRL register are cleared or the interrupt-enable bits in the T3E3SRIE register are cleared. The setting of this status bit can cause a hardware interrupt to occur if the T3E3IE bit in the MSRIE register is set to 1. The interrupt is cleared when this bit is cleared or the interrupt-enable bit in the MSRIE register is cleared.

Bit 6: Loss-of-Transmit Clock Detected (LOTC). This real-time status bit is set when the device detects that the TICLK input pin has not toggled for between 9 and 21 clock periods. This bit is cleared when a clock is detected at the TICLK input. The system clock (SCLK) is used to check for the presence of the TICLK. On reset the LOTC status bit is set for a few clock cycles and then cleared if TICLK is present.

Bit 7: Loss-of-Receive Clock Detected (LORC). This real-time status bit is set when the device detects that the RCLK input pin has not toggled for between 9 and 21 clock periods. This bit is cleared when a clock is detected at the RCLK input. The system clock (SCLK) checks for the presence of the RCLK. On reset the LORC status bit is set for a few clock cycles and then cleared if RCLK is present.

Register Name: **MSRL**
Register Description: **Master Status Register Latched**
Register Address: **09h**

Bit #	7	6	5	4	3	2	1	0
Name	LORCL	LOTCL	N/A	N/A	N/A	N/A	COVFL	OSTL
Default	—	—	—	—	—	—	—	—

Note: *See Figure 7-4 for details on the interrupt logic for the status bits in the MSRL register.*

Bit 0: One-Second Timer Latched (OSTL). This latched status bit is set to 1 on each 1-second boundary, as timed by the device. The device chooses an arbitrary 1-second boundary that is timed from either the RCLK signal or the TICLK signal depending on the setting of the OSTCS bit in MC2. OSTL is cleared when the host processor writes a 1 to it and is not set again until another 1-second boundary has occurred. When OSTL is set, it can cause a hardware interrupt to occur if the OSTIE bit in the MSRIE register is set to 1. The interrupt is cleared when this bit is cleared or the interrupt-enable bit is cleared. This bit can be used to determine when to read the error counters, if the counters are automatically updated by the 1-second timer.

Bit 1: Counter Overflow Event Latched (COVFL). This latched status bit is set to 1 when the COVF status bit in the MSR register goes high. COVFL is cleared when the host processor writes a 1 to it and is not set again until COVF goes high again. When COVFL is set, it can cause a hardware interrupt to occur if the COVFIE bit in the MSRIE register is set to 1. The interrupt is cleared when this bit is cleared or the interrupt-enable bit is cleared. This bit can be used to determine when a counter overflow event occurs.

Bit 6: Loss-of-Transmit Clock Latched (LOTCL). This latched status bit is set to 1 when the LOTC status bit in the MSR register goes high. LOTCL is cleared when the host processor writes a 1 to it and is not set again until LOTC goes high again. When LOTCL is set, it can cause a hardware interrupt to occur if the LOTCIE bit in the MSRIE register is set to 1. The interrupt is cleared when this bit is cleared or the interrupt-enable bit is cleared. This bit can be used to determine when a loss of transmit clock event occurs.

Bit 7: Loss-of-Receive Clock Latched (LORCL). This latched status bit is set to 1 when the LORC status bit in the MSR register goes high. LORCL is cleared when the host processor writes a 1 to it and is not set again until LORC goes high again. When LORCL is set, it can cause a hardware interrupt to occur if the LORCIE bit in the MSRIE register is set to 1. The interrupt is cleared when this bit is cleared or the interrupt-enable bit is cleared. This bit can be used to determine when a loss of receive clock event occurs.

Register Name: **MSRIE**
Register Description: **Master Status Register Interrupt Enable**
Register Address: **0Ah**

Bit #	7	6	5	4	3	2	1	0
Name	LORCIE	LOTCIE	T3E3IE	FEACIE	HDLCIE	BERTIE	COVFIE	OSTIE
Default	0	0	0	0	0	0	0	0

Bit 0: One-Second Timer Interrupt Enable (OSTIE). This bit enables an interrupt if the OSTL bit in the MSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 1: Counter Overflow Event Interrupt Enable (COVFIE). This bit enables an interrupt if the COVFL bit in the MSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 2: Change in BERT Status Interrupt Enable (BERTIE). This bit enables an interrupt if the BERT bit in the MSR register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 3: Change in HDLC Status Interrupt Enable (HDLCIE). This bit enables an interrupt if the HDLC bit in the MSR register is set.
0 = interrupt disabled
1 = interrupt enabled

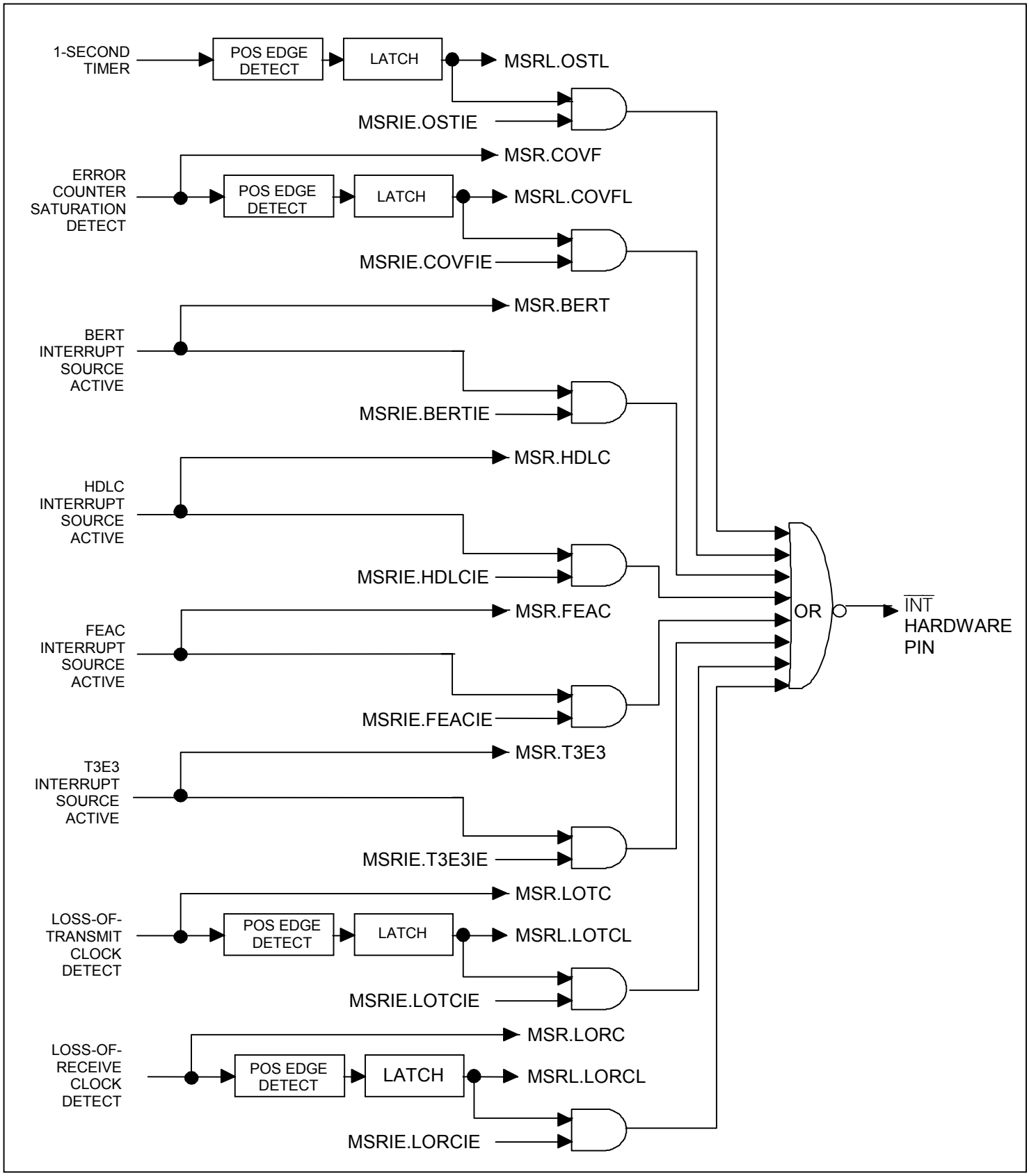
Bit 4: Change in FEAC Status Interrupt Enable (FEACIE). This bit enables an interrupt if the FEAC bit in the MSR register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 5: Change in DS3/E3 Framer Status Interrupt Enable (T3E3IE). This bit enables an interrupt if the T3E3 bit in the MSR register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 6: Loss-of-Transmit Clock Interrupt Enable (LOTCIE). This bit enables an interrupt if the LOTCL bit in the MSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 7: Loss-of-Receive Clock Interrupt Enable (LORCIE). This bit enables an interrupt if the LORCL bit in the MSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Figure 7-4. MSR Status Bit Interrupt Signal Flow



7.7 DS3/E3 Framer

7.7.1 DS3/E3 Framer Register Description

Table 7-D. DS3/E3 Framer Register Map

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
10	T3E3CR1	E3SnC1	E3SnC0	T3IDLE	TRAI	TAIS	TPT	CBEN	DS3M
11	T3E3CR2	FRESYNC	N/A	TFEBE	AFEBED	ECC	FECC1	FECC0	E3CVE
12	T3E3EIC	MEIMS	FBEIC1	FBEIC0	FBEI	T3CPBEI	T3PBEI	EXZI	BPVI
18	T3E3SR	N/A	N/A	SEF	T3IDLE	RAI	AIS	OOF	LOS
19	T3E3SRL	COFAL	N/A	SEFL	T3IDLEL	RAIL	AISL	OOFL	LOSL
1A	T3E3SRIE	COFAIE	N/A	SEFIE	T3IDLEIE	RAIIE	AISIE	OOFIE	LOSIE
1B	T3E3IR	RUA1	T3AIC	E3Sn	N/A	EXZL	MBEL	FBEL	ZSCDL
20	BPVCR1	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
21	BPVCR2	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
22	EXZCR1	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
23	EXZCR2	EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8
24	FECR1	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
25	FECR2	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
26	PCR1	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
27	PCR2	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
28	CPCR1	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
29	CPCR2	CPE15	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8
2A	FEBECR1	FEBE7	FEBE6	FEBE5	FEBE4	FEBE3	FEBE2	FEBE1	FEBE0
2B	FEBECR2	FEBE15	FEBE14	FEBE13	FEBE12	FEBE11	FEBE10	FEBE9	FEBE8

Register Name: **T3E3CR1**
Register Description: **T3/E3 Control Register**
Register Address: **10h**

Bit #	7	6	5	4	3	2	1	0
Name	E3SnC1	E3SnC0	T3IDLE	TRAI	TAIS	TPT	CBEN	DS3M
Default	0	0	0	0	0	0	0	0

Bit 0: DS3 Mode Select (DS3M). Selects DS3 or E3 operation. It must be set immediately after reset to select DS3 mode.

0 = E3 mode
1 = DS3 mode

Bit 1: C-Bit Parity Mode Enable (CBEN). This bit is only active when the framer is in DS3 mode. When this bit is logic 0, C-Bit Parity is defeated and the C bits are sourced from the TDAT input pin.

0 = disable C-Bit Parity mode (also known as the M23 mode)
1 = enable C-Bit Parity mode

Bit 2: DS3/E3 Transmit Pass-Through Enable (TPT). When this bit is set to logic 1, the transmit formatter sources data from the TDAT input on every TCLK cycle and does not insert framing overhead into the transmit data stream. In this mode the TDEN/TGCLK output still marks where the payload bits would be if TPT were not enabled, and the TSOF output still marks the start of a frame. When in this mode, the BERT does not function in payload-only mode; entire-frame mode should be used instead.

0 = configure the formatter to insert framing overhead bits
1 = configure the formatter to pass through TDAT data without inserting framing overhead bits

Bit 3: DS3/E3 Transmit Alarm-Indication Signal (TAIS). When this bit is logic 1 in DS3 mode, the transmitter generates DS3 AIS, which is a properly F-bit and M-bit framed 1010... data pattern with both X bits set to 1, all C bits set to 0, and the proper P bits. When this bit is logic 1 in E3 mode, the transmitter generates an unframed all-ones pattern. When this bit is logic 0, normal data is transmitted.

0 = do not transmit AIS
1 = transmit AIS

Bit 4: DS3/E3 Transmit Remote Alarm Indication (TRAI). When this bit is logic 1 in DS3 mode, both X bits of each DS3 frame are set to logic 0. When this bit is logic 1 in E3 mode, the RAI bit (bit 11 of each E3 frame) is set to logic 1. When this bit is logic 0 in DS3 mode, both X bits are set to logic 1. When this bit is logic 0 in E3 mode, the RAI bit is set to logic 0.

0 = do not transmit RAI
1 = transmit RAI

Bit 5: Transmit DS3 Idle Signal Enable (T3IDLE). When this bit is logic 1 in DS3 mode, the transmitter generates the DS3 idle signal instead of the normal transmit data. The DS3 idle signal is defined as a normally DS3 framed pattern (i.e., with the proper F bits and M bits along with the proper P bits) where the information bit fields are completely filled with a data pattern of 1100..., the C bits in Subframe 3 are set to logic 0, and both X bits are set to logic 1. In C-Bit Parity mode, the PMDL and FEAC channels are still enabled. This bit is ignored in the E3 mode.

0 = do not transmit DS3 idle signal
1 = transmit DS3 idle signal

Bits 6, 7: E3 National Bit Control (E3SnC[1:0]). These bits determine the source of the E3 National bit (Sn). On the receive side, the Sn bit is always routed to the T3E3IR register as well as the HDLC controller and the FEAC controller. These bits are ignored in DS3 mode.

E3SnC1	E3SnC0	SOURCE OF THE E3 NATIONAL BIT (Sn)
0	0	Force the Sn bit to logic 1
0	1	Source the Sn bit from the HDLC controller
1	0	Source the Sn bit from the FEAC controller
1	1	Force the Sn bit to logic 0

Register Name: **T3E3CR2**
Register Description: **DS3/E3 Control Register**
Register Address: **11h**

Bit #	7	6	5	4	3	2	1	0
Name	FRESYNC	N/A	TFEBE	AFEBED	ECC	FECC1	FECC0	E3CVE
Default	0	—	0	0	0	0	0	0

Bit 0: E3 Code Violation Enable (E3CVE). This bit is ignored in the DS3 mode. In E3 mode, this bit is used to configure the bipolar violation count register (BPVCR1) to count either bipolar violations (BPV) or code violations (CV). A BPV is defined as consecutive pulses (or marks) of the same polarity that are not part of an HDB3 codeword. A CV is defined in ITU O.161 as consecutive BPVs of the same polarity.

0 = count BPVs
1 = count CVs

Bits 1, 2: Frame Error-Counting Control (FECC[1:0])

FECC[1:0]	FRAME ERROR-COUNT REGISTER (FECR1) CONFIGURATION
00	DS3 Mode: Count OOF occurrences E3 Mode: Count OOF occurrences
01	DS3 Mode: Count both F-bit and M-bit errors E3 Mode: Count bit errors in the FAS word
10	DS3 Mode: Count only F-bit errors E3 Mode: Count word errors in the FAS word
11	DS3 Mode: Count only M-bit errors E3 Mode: Illegal state

Bit 3: Error-Counting Control (ECC). This bit is used to control whether the framer increments certain error counters during OOF conditions. It only affects the error counters that deal with framing overhead:

Frame Error-Count Register (FECR1) (when it is configured to count frame errors, not OOFs)
DS3 P-Bit Parity Error-Count Register (PCR1)
DS3 CP-Bit Parity Error-Count Register (CPCR1)
DS3 Far-End Block Error-Count Register (FEBECR1)

When this bit is logic 0, these error counters are not allowed to increment during OOF conditions. When this bit is logic 1, these error counters are allowed to increment during OOF conditions.

0 = do not allow the FECR/PCR/CPCR/FEBECR error counters to increment during OOF
1 = allow the FECR/PCR/CPCR/FEBECR error counters to increment during OOF

Bit 4: Automatic FEBE Defeat (AFEBED). This bit is ignored in E3 mode and in M23 DS3 mode. When this bit is low, the framer automatically inserts FEBE codes into the transmit data stream by setting all three C bits in M-subframe 4 to logic 0. A FEBE condition occurs when any received M bits or F bits are in error, or when the received CP bits indicate a parity error or when the receiver is in the OOF condition.

0 = automatically insert FEBE codes in the transmit data stream based on detected errors
1 = use the TFEBE control to determine the state of the FEBE codes

Bit 5: Transmit FEBE Setting (TFEBE). This bit is only active when AFEBED is logic 1. When this bit is logic 0, the formatter forces the FEBE code to 111. When this bit is set logic 1, the formatter forces the FEBE code to 000.

0 = force FEBE to 111 (null state)
1 = force FEBE to 000 (active state)

Bit 7: Force Receive Framer Resynchronization (FRESYNC). A 0-to-1 transition on this bit causes the receive framer to resynchronize. This bit must be cleared and set again for a subsequent resynchronization to occur.

Register Name: **T3E3EIC**
Register Description: **DS3/E3 Error Insert Control Register**
Register Address: **12h**

Bit #	7	6	5	4	3	2	1	0
Name	MEIMS	FBEIC1	FBEIC0	FBEI	T3CPBEI	T3PBEI	EXZI	BPVI
Default	0	0	0	0	0	0	0	0

Bit 0: Bipolar Violation Insert (BPVI). A 0-to-1 transition on this bit causes a single BPV to be inserted into the transmit data stream during the next occurrence of three consecutive 1s. This bit must be cleared and set again for a subsequent BPV to be inserted. Toggling this bit has no effect when the LIU interface is in the binary mode. In the manual error insert mode (MEIMS = 1), errors are inserted on each toggle of the TMEI input signal as long as this bit is logic 1. When this bit is logic 0, no BPVs are inserted.

Bit 1: Excessive Zero Insert (EXZI). A 0-to-1 transition on this bit causes a single EXZ event to be inserted into the transmit data stream. An EXZ event is defined as three or more consecutive 0s in the DS3 mode and four or more consecutive 0s in the E3 mode. After this bit has been toggled from logic 0 to logic 1, the formatter suppresses the next possible B3ZS/HDB3 codeword substitution to create the EXZ event. This bit must be cleared and set again for a subsequent EXZ event to be inserted. Toggling this bit has no effect when the LIU interface is in the binary mode. In the manual error insert mode (MEIMS = 1), errors are inserted on each toggle of the TMEI input signal as long as this bit is logic 1. When this bit is logic 0, no EXZ events are inserted.

Bit 2: DS3 P-Bit Parity Error Insert (T3PBEI). A 0-to-1 transition on this bit causes a single DS3 P-bit parity error event to be inserted into the transmit data stream. A DS3 P-bit parity error is defined as inverting both P bits in a DS3 frame. Once this bit has been toggled from logic 0 to logic 1, the formatter flips both P bits in the next DS3 frame. This bit must be cleared and set again for a subsequent error to be inserted. Toggling this bit has no effect when the framer is operated in the E3 mode. In the manual error insert mode (MEIMS = 1), errors are inserted on each toggle of the TMEI input signal as long as this bit is logic 1. When this bit is logic 0, no P-bit parity errors are inserted.

Bit 3: DS3 C-Bit Parity Error Insert (T3CPBEI). A 0-to-1 transition on this bit causes a single DS3 CP-bit parity error event to be inserted into the transmit data stream. A DS3 CP-bit parity error is defined as inverting the proper polarity of all three CP bits in a DS3 frame. Once this bit has been toggled from logic 0 to logic 1, the framer flips all three CP bits in the next DS3 frame. This bit must be cleared and set again for a subsequent error to be inserted. Toggling this bit has no effect when the framer is not operated in C-Bit Parity mode or when the framer is operated in the E3 mode. In the manual error insert mode (MEIMS = 1), errors are inserted on each toggle of the TMEI input signal as long as this bit is logic 1. When this bit is logic 0, no CP-bit parity errors are inserted.

Bit 4: Frame Bit-Error Insert (FBEI). A 0-to-1 transition on this bit causes the transmit framer to generate framing bit errors. The type of framing bit error to be inserted is controlled by the FBEIC[1:0] bits. Once this bit has been toggled from logic 0 to logic 1, the framer inserts framing bit errors in the next possible frame. This bit must be cleared and set again for a subsequent error to be inserted. In the manual error insert mode (MEIMS = 1), errors are inserted on each toggle of the TMEI input signal as long as this bit is logic 1. When this bit is logic 0, no frame bit errors are inserted.

Bits 5, 6: Frame Bit-Error Insert Control Bits 0 and 1 (FBEIC[1:0])

FBEIC[1:0]	TYPE OF FRAMING BIT ERROR INSERTED
00	**DS3 Mode:** A single F-bit error **E3 Mode:** A single FAS word of 1111**1**10000 is generated instead of the normal FAS word, which is 1111**0**10000 (i.e., only 1 bit inverted)
01	**DS3 Mode:** A single M-bit error **E3 Mode:** A single FAS word of 0000101111 is generated instead of the normal FAS word, which is 1111010000 (i.e., all FAS bits are inverted)
10	**DS3 Mode:** Four consecutive F-bit errors (causes the far end to lose synchronization) **E3 Mode:** Four consecutive FAS words of 1111**1**10000 are generated instead of the normal FAS word, which is 1111**0**10000 (i.e., only 1 bit inverted; causes the far end to lose synchronization)
11	**DS3 Mode:** Three consecutive M-bit errors (causes the far end to lose synchronization) **E3 Mode:** Four consecutive FAS words of 0000101111 are generated instead of the normal FAS word, which is 1111010000 (i.e., all FAS bits are inverted; causes the far end to lose synchronization)

Bit 7: Manual Error-Insert Mode Select (MEIMS). When this bit is logic 0, the framer inserts errors on each 0-to-1 transition of the BPVI, EXZI, T3PBEI, T3CPBEI, or FBEI control bits. When this bit is logic 1, the framer inserts errors on each 0-to-1 transition of the TMEI input signal. The appropriate BPVI, EXZI, T3PBEI, T3CPBEI, or FBEI control bit must be set to 1 for this to occur. If all of the BPVI, EXZI, T3PBEI, T3CPBEI, and FBEI control bits are set to 0, no errors are inserted.

0 = use 0-to-1 transition on the BPVI, EXZI, T3PBEI, T3CPBEI, or FBEI control bits to insert errors
1 = use 0-to-1 transition on the TMEI input signal to insert errors

Register Name: **T3E3SR**
Register Description: **DS3/E3 Status Register**
Register Address: **18h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	SEF	T3IDLE	RAI	AIS	OOF	LOS
Default	—	—	—	—	—	—	—	—

Bit 0: Loss-of-Signal Occurrence (LOS). This real-time status bit is set when the framer detects loss-of-signal and cleared when the LOS condition terminates. The LOS alarm criteria are described in Table 7-Eand Table 7-F.

Note: *The LOS status bit is only valid when the framer is in dual-rail (POS/NEG) interface mode. When the framer is in binary (NRZ) interface mode, LOS status must be sourced from the neighboring LIU. The reason for this is that in binary mode the neighboring LIU performs B3ZS/HDB3 decoding—substituting zeros for B3ZS/HDB3 codewords—before passing the received traffic to the framer. Because this decoded traffic can legitimately have long strings of zeros in it, the framer cannot look for and declare LOS in binary mode. In general, the IC that does the B3ZS/HDB3 decoding must provide the LOS status information.*

Bit 1: Out-of-Frame Occurrence (OOF). This real-time status bit is set when the framer detects an OOF condition and cleared when the OOF condition terminates. The OOF defect criteria are described in Table 7-Eand Table 7-F.

Bit 2: Alarm Indication Signal Detected (AIS). This real-time status bit is set when the framer detects an incoming AIS and cleared when the AIS condition terminates. The AIS alarm criteria are described in Table 7-Eand Table 7-F.

Bit 3: Remote Alarm Indication Detected (RAI). This real-time status bit is set when the framer detects an incoming RAI signal on the X bits or Sa bits and cleared when the RAI condition terminates. The RAI alarm criteria are described in Table 7-Eand Table 7-F. RAI can also be indicated through FEAC codes when the framer is operated in DS3 C-Bit Parity mode, but this bit does not indicate the FEAC alarm code detection.

Bit 4: DS3 Idle-Signal Detected (T3IDLE). This real-time status bit is set when the framer detects an incoming DS3 idle signal and cleared when the idle signal terminates. The DS3 idle signal alarm criteria are described in Table 7-Eand Table 7-F. When the framer is operated in the E3 mode, this status bit should be ignored.

Bit 5: Severely Errored-Frame Detected (SEF). This real-time status bit is set when the frame detects a severely errored frame condition and cleared when the SEF condition clears. The SEF defect criteria are described in Table 7-Eand Table 7-F.

Register Name: **T3E3SRL**
Register Description: **DS3/E3 Status Register Latched**
Register Address: **19h**

Bit #	7	6	5	4	3	2	1	0
Name	COFAL	N/A	SEFL	T3IDLEL	RAIL	AISL	OOFL	LOSL
Default	—	—	—	—	—	—	—	—

Note: *See Figure 7-5 for details on the interrupt logic for the status bits in the T3E3SRL register.*

Bit 0: Loss-of-Signal Occurrence Latched (LOSL). This latched status bit is set to 1 when the LOS status bit in the T3E3SR register changes state (low to high or high to low). LOSL is cleared when the host processor writes a 1 to it. When LOSL is set, it can cause a hardware interrupt to occur if the LOSIE bit in the T3E3SRIE register and the T3E3IE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared. See the note in the LOS status bit description for further information.

Bit 1: Out-of-Frame Occurrence Latched (OOFL). This latched status bit is set to 1 when the OOF status bit in the T3E3SR register changes state (low to high or high to low). OOFL is cleared when the host processor writes a 1 to it. When OOFL is set, it can cause a hardware interrupt to occur if the OOFIE bit in the T3E3SRIE register and the T3E3IE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 2: Alarm Indication Signal Detected Latched (AISL). This latched status bit is set to 1 when the AIS status bit in the T3E3SR register changes state (low to high or high to low). AISL is cleared when the host processor writes a 1 to it. When AISL is set, it can cause a hardware interrupt to occur if the AISIE bit in the T3E3SRIE register and the T3E3IE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 3: Remote Alarm Indication Detected Latched (RAIL). This latched status bit is set to 1 when the RAI status bit in the T3E3SR register changes state (low to high or high to low). RAIL is cleared when the host processor writes a 1 to it. When RAIL is set, it can cause a hardware interrupt to occur if the RAIIE bit in the T3E3SRIE register and the T3E3IE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 4: DS3 Idle-Signal-Detected Latched (T3IDLEL). This latched status bit is set to 1 when the T3IDLE status bit in the T3E3SR register changes state (low to high or high to low). T3IDLEL is cleared when the host processor writes a 1 to it. When T3IDLEL is set, it can cause a hardware interrupt to occur if the T3IDLEIE bit in the T3E3SRIE register and the T3E3IE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 5: Severely Errored Frame Detected Latched (SEFL). This latched status bit is set to 1 when the SEF status bit in the T3E3SR register changes state (low to high or high to low). SEFL is cleared when the host processor writes a 1 to it. When SEFL is set, it can cause a hardware interrupt to occur if the SEFIE bit in the T3E3SRIE register and the T3E3IE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 7: Change-of-Frame Alignment Latched (COFAL). This latched status bit is set to 1 when the DS3/E3 framer has experienced a change of frame alignment (COFA). A COFA occurs when the framer achieves synchronization in a different alignment than it had previously. If the framer has never acquired synchronization before, then this status bit is meaningless. COFAL is cleared when the host processor writes a 1 to it and is not set again until the framer has lost synchronization and reacquired synchronization in a different alignment. When COFAL is set, it can cause a hardware interrupt to occur if the COFAIE bit in the T3E3SRIE register and the T3E3IE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Register Name: **T3E3SRIE**
Register Description: **DS3/E3 Status Register Interrupt Enable**
Register Address: **1Ah**

Bit #	7	6	5	4	3	2	1	0
Name	COFAIE	N/A	SEFIE	T3IDLEIE	RAIIE	AISIE	OOFIE	LOSIE
Default	0	—	0	0	0	0	0	0

Bit 0: Loss-of-Signal Occurrence Interrupt Enable (LOSIE). This bit enables an interrupt if the LOSL bit in the T3E3SRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 1: Out-of-Frame Occurrence Interrupt Enable (OOFIE). This bit enables an interrupt if the OOFL bit in the T3E3SRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 2: Alarm Indication Signal Detected Interrupt Enable (AISIE). This bit enables an interrupt if the AISL bit in the T3E3SRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 3: Remote Alarm Indication Detected Interrupt Enable (RAIIE). This bit enables an interrupt if the RAIL bit in the T3E3SRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 4: DS3 Idle-Signal-Detected Interrupt Enable (T3IDLEIE). This bit enables an interrupt if the T3IDLEL bit in the T3E3SRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 5: Severely Errored Frame Detected-Interrupt Enable (SEFIE). This bit enables an interrupt if the SEFL bit in the T3E3SRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 7: Change-of-Frame Alignment Interrupt Enable (COFAIE). This bit enables an interrupt if the COFAL bit in the T3E3SRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Figure 7-5. T3E3SR Status Bit Interrupt Signal Flow

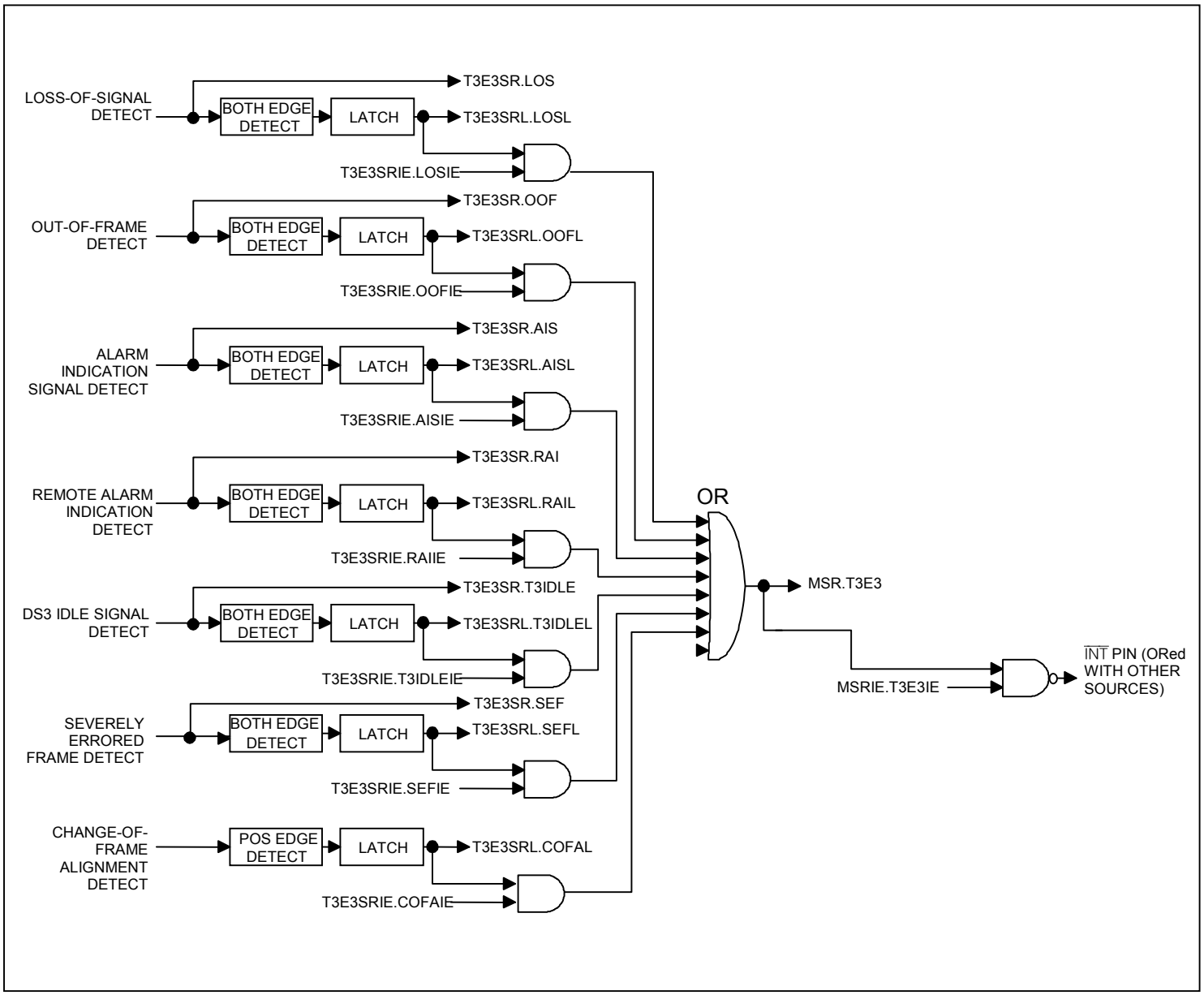


Table 7-E. DS3 Alarm Criteria

ALARM/ CONDITION	FUNCTION	SET CRITERIA	CLEAR CRITERIA
AIS	Alarm Indication Signal. Properly framed 1010... pattern (starting with 1 after each overhead bit), all C bits set to 0	In each 84-bit information field, the properly aligned 1010... pattern is detected with fewer than four bit errors (out of 84 possible) for 1024 consecutive information bit fields (1.95ms) and all C bits are majority decoded to be 0 during this time.	In each 84-bit information field, the properly aligned 1010... pattern is detected with four or more bit errors (out of 84 possible) for 1024 consecutive information bit fields (1.95ms)
RUA1	Unframed All-Ones	Four or fewer 0s in two consecutive 4760-bit frames	Five or more 0s in two consecutive 4760-bit frames
LOS	Loss of Signal	192 consecutive 0s	No EXZ events over a 192-bit window that starts with the first 1 received
OOF	Out of Frame. Too many F bits or M bits in error.	Three or more F bits in error out of 16 consecutive, or two or more M bits in error out of four consecutive	No errors in six consecutive sets of four F bits followed by two consecutive frames with no M bits errors, X bits matching and P bits matching
SEF	Severely Errored Frame	Three or more F bits in error out of 16 consecutive F bits	In sync (OOF = 0) and fewer than three F bits in error out of 16 consecutive F bits
RAI	Remote Alarm Indication (Also referred to as SEF/AIS in Bellcore GR-820.) X1 = X2 = 0 (active) X1 = X2 = 1 (inactive)	X1 = X2 = 0 for four consecutive M-frames (426µs)	X1 = X2 = 1 for four consecutive M-frames (426µs)
T3IDLE	DS3 Idle Signal. Properly framed 1100... pattern (starting with 11 after each overhead bit), the C bits in M-subframe 3 set to 0	In each 84-bit information field, the properly aligned 1100... pattern is detected with fewer than four bit errors (out of 84 possible) for 1024 consecutive information bit fields (1.95ms), and the C bits in M-subframe 3 are majority decoded to be 0 during this time	In each 84-bit information field, the properly aligned 1100... pattern is detected with four or more bit errors (out of 84 possible) for 1024 consecutive information bit fields (1.95ms)

Table 7-F. E3 Alarm Criteria

ALARM/ CONDITION	FUNCTION	SET CRITERIA	CLEAR CRITERIA
AIS	Alarm Indication Signal. Unframed all ones.	Four or fewer 0s in two consecutive 1536-bit frames	Five or more 0s in two consecutive 1536-bit frames
RUA1	Unframed All Ones	Four or fewer 0s in two consecutive 1536-bit frames	Five or more 0s in two consecutive 1536-bit frames
LOS	Loss of Signal	192 consecutive 0s	No EXZ events over a 192-bit window that starts with the first 1 received
SEF	Severely Errored Frame	Same as OOF	Same as OOF
OOF	Out of Frame. Too many FAS errors.	Four consecutive bad FAS	Three consecutive good FAS
RAI	Remote Alarm Indication Inactive: bit 11 of the frame = 0 Active: bit 11 of the frame = 1	Bit 11 = 1 for four consecutive frames (6144 bits, 179µs)	Bit 11 = 0 for four consecutive frames (6144 bits, 179µs)

Register Name: **T3E3IR**
Register Description: **DS3/E3 Information Register**
Register Address: **1Bh**

Bit #	7	6	5	4	3	2	1	0
Name	RUA1	T3AIC	E3Sn	N/A	EXZL	MBEL	FBEL	ZSCDL
Default	—	—	—	—	—	—	—	—

Note: *The status bits in T3E3IR cannot cause a hardware interrupt to occur.*

Bit 0: Zero-Suppression Codeword-Detected Latched (ZSCDL). This latched information bit is set to 1 when the framer detects a B3ZS/HDB3 codeword. ZSCDL is cleared when the host processor writes a 1 to it and is not set again until the framer has detected another B3ZS/HDB3 codeword. This bit has no meaning when the part is configured to operate in binary mode (BIN = 1 in the MC1 register) and should be ignored. This status is still active when the ZCSD control bit is set in the MC1 register.

Bit 1: F-Bit or FAS Error-Detected Latched (FBEL). This latched information bit is set to 1 when the framer detects an error in either the F bits (DS3 mode) or the FAS word (E3 mode). FBEL is cleared when the host processor writes a 1 to it and is not set again until the framer detects another error.

Bit 2: M-Bit Error-Detected Latched (MBEL). This latched information bit is set to 1 when the framer detects an error in the M bits. MBEL is cleared when the host processor writes a 1 to it and is not set again until the framer detects another error in the M bits. This status bit has no meaning in the E3 mode (DS3M = 0 in register MC1) and should be ignored.

Bit 3: Excessive Zeros-Detected Latched (EXZL). This latched information bit is set to 1 when the framer detects a consecutive string of either three or more 0s (DS3 mode) or four or more 0s (E3 mode). EXZL is cleared when the host processor writes a 1 to it and is not set again until the framer detects another excessive zero event. This status is not active when the framer is configured to operate in binary mode (BIN = 1 in register MC1).

Bit 5: E3 National Bit (E3Sn). This real-time status bit reports the incoming E3 National Bit (Sn). E3Sn is loaded at the start of each E3 frame as the Sn bit is decoded.

Bit 6: DS3 Application ID Channel Status (T3AIC). This real-time status bit indicates whether the incoming DS3 data stream is in C-Bit Parity format or M23 format. In the DS3 frame, the first C bit in M-subframe 1 is the application identification channel (AIC). ANSI T1.107 mandates that the AIC must be set to 1 for C-Bit Parity applications and must be toggling between 0 and 1 for M23 application (since it is a stuff control bit). The T3AIC information bit is set to 1 when the framer detects that the AIC is set to 1 for 1020 times or more out of 1024 consecutive M-frames (109ms). T3AIC is cleared when the framer detects that the AIC is set to 1 less than 1020 times out of 1024 consecutive M-frames (109ms). This status bit has no meaning in the E3 mode and should be ignored.

Bit 7: Receive Unframed All Ones (RUA1). This real-time status bit indicates that the framer is receiving an unframed all-ones signal. This status bit is valid in both DS3 and E3 modes and has the same function in both modes. The set and clear criteria for RUA1 are listed in Table 7-E and Table 7-F.

7.8 DS3/E3 Performance Error Counters

There are six internal error counters and six corresponding error count registers in the DS3/E3 framer. All the error counters and count registers are 16 bits in length. The framer can be configured to update the count registers with the latest counter values automatically once a second or manually through either the MECU bit in the MC1 register or the RECU input pin. When the count registers are updated through any of these methods, the internal error counters are reset to 0. All the error counters saturate when full and do not roll over. When any of the error counters are saturated, the COVF bit is set in the MSR register.

Register Name: **BPVCR1**
Register Description: **Bipolar Violation Count Register 1**
Register Address: **20h**

Bit #	7	6	5	4	3	2	1	0
Name	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
Default	0	0	0	0	0	0	0	0

Register Name: **BPVCR2**
Register Description: **Bipolar Violation Count Register 2**
Register Address: **21h**

Bit #	7	6	5	4	3	2	1	0
Name	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
Default	0	0	0	0	0	0	0	0

Bits 0 to 15: Bipolar Violation Count (BPV[15:0]). This count register contains the value of the internal BPV/CV error counter latched during the last error counter update. In DS3 mode, the internal counter counts bipolar violations (BPV). In the E3 mode, the counter can be configured through the E3CVE bit in the T3E3CR2 register to count BPVs or code violations (CVs). A BPV is defined as consecutive pulses (or marks) of the same polarity that are not part of a B3ZS/HDB3 codeword. A CV is defined in ITU O.162 as two consecutive BPVs of the same polarity. When the line interface is in binary mode (BIN = 1 in the MC1 register), the internal counter increments for each RCLK clock cycle that the RLCV pin is active. The RLCV pin is normally active high but can be inverted using the RNEGI bit in the MC5 register. The BPV counter ignores the RLCV pin when the device is in diagnostic loopback (DLB = 1 in register MC2).

Register Name: **EXZCR1**
Register Description: **Excessive Zero Count Register 1**
Register Address: **22h**

Bit #	7	6	5	4	3	2	1	0
Name	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
Default	0	0	0	0	0	0	0	0

Register Name: **EXZCR2**
Register Description: **Excessive Zero Count Register 2**
Register Address: **23h**

Bit #	7	6	5	4	3	2	1	0
Name	EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8
Default	0	0	0	0	0	0	0	0

Bits 0 to 15: Excessive Zero Count (EXZ[15:0]). This count register contains the value of the internal EXZ error counter latched during the last error counter update. The internal counter counts excessive zero occurrences (EXZ). An EXZ occurrence is defined as three or more consecutive 0s in DS3 mode and four or more consecutive 0s in E3 mode. As an example, a string of eight consecutive 0s is a single EXZ occurrence and would only increment this counter once.

Register Name: **FECR1**
Register Description: **Frame Error Count Register 1**
Register Address: **24h**

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	0	0	0	0	0	0	0	0

Register Name: **FECR2**
Register Description: **Frame Error Count Register 2**
Register Address: **25h**

Bit #	7	6	5	4	3	2	1	0
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	0	0	0	0	0	0	0	0

Bits 0 to 15: Frame Error Count (FE[15:0]). This count register contains the value of the internal framer error counter latched during the last error counter update. The internal counter counts either the number of OOF occurrences or the number of framing bit errors received. The type of counting is configured through the FECC[1:0] control bits in the T3E3CR2 register. The possible configurations are shown below.

FECC[1:0]	Frame Error-Count Register (FECR1) Configuration
00	DS3 Mode: Count OOF occurrences E3 Mode: Count OOF occurrences
01	DS3 Mode: Count both F-bit and M-bit errors E3 Mode: Count bit errors in the FAS word
10	DS3 Mode: Count only F-bit errors E3 Mode: Count word errors in the FAS word
11	DS3 Mode: Count only M-bit errors E3 Mode: Illegal state

When the counter is configured to count OOF occurrences, it increments by one each time the framer loses receive synchronization. When the counter is configured to count framing bit errors, the counter can be configured through the ECC control bit in the T3E3CR2 register to either continue counting frame bit errors during an OOF event or not.

Register Name: **PCR1**
Register Description: **P-Bit Parity Error Count Register 1**
Register Address: **26h**

Bit #	7	6	5	4	3	2	1	0
Name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	0	0	0	0	0	0	0	0

Register Name: **PCR2**
Register Description: **P-Bit Parity Error Count Register 2**
Register Address: **27h**

Bit #	7	6	5	4	3	2	1	0
Name	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
Default	0	0	0	0	0	0	0	0

Bits 0 to 15: P-Bit Parity Error Count (PE[15:0]). This count register contains the value of the internal P-bit parity error counter latched during the last error counter update. The internal counter counts the number of DS3 P-bit parity errors. In E3 mode this counter is meaningless and should be ignored. A P-bit parity error is defined as an occurrence when the two P bits in a DS3 frame do not match one another or when the two P bits do not match the parity calculation made on the information bits. Through the ECC control bit in the T3E3CR2 register, the counter can be configured to either continue counting P-bit parity errors during an OOF event or not.

Register Name: **CPCR1**
Register Description: **CP-Bit Parity Error Count Register 1**
Register Address: **28h**

Bit #	7	6	5	4	3	2	1	0
Name	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
Default	0	0	0	0	0	0	0	0

Register Name: **CPCR2**
Register Description: **CP-Bit Parity Error Count Register 2**
Register Address: **29h**

Bit #	7	6	5	4	3	2	1	0
Name	CPE15	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8
Default	0	0	0	0	0	0	0	0

Bits 0 to 15: CP-Bit Parity Error Count (CPE[15:0]). This count register contains the value of the internal CP-bit parity error counter latched during the last error counter update. The internal counter counts the number of DS3 CP-bit parity errors. In E3 mode or M23 DS3 mode this counter is meaningless and should be ignored. A CP-bit parity error is defined as an occurrence when the majority-decoded state of the three CP bits does not match the parity calculation made on the information bits. Through the ECC control bit in the T3E3CR2 register, the counter can be configured to either continue counting CP-bit parity bit errors during an OOF event or not.

Register Name: **FEBECR1**
Register Description: **Far-End Block Error Count Register 1**
Register Address: **2Ah**

Bit #	7	6	5	4	3	2	1	0
Name	FEBE7	FEBE6	FEBE5	FEBE4	FEBE3	FEBE2	FEBE1	FEBE0
Default	0	0	0	0	0	0	0	0

Register Name: **FEBECR2**
Register Description: **Far-End Block Error Count Register 2**
Register Address: **2Bh**

Bit #	7	6	5	4	3	2	1	0
Name	FEBE15	FEBE14	FEBE13	FEBE12	FEBE11	FEBE10	FEBE9	FEBE8
Default	0	0	0	0	0	0	0	0

Bits 0 to 15: Far-End Block Error Count (FEBE[15:0]). This count register contains the value of the internal FEBE counter latched during the last error counter update. The internal counter counts the number of DS3 far-end block errors (FEBE). In E3 mode or M23 DS3 mode this counter is meaningless and should be ignored. A FEBE is defined as an occurrence when the three received FEBE bits do not equal 111. Through the ECC control bit in the T3E3CR2 register, the counter can be configured to either continue counting FEBE occurrences during an OOF event or not.

7.9 BERT

The BERT block can generate and detect the following patterns:

- Maximal-length pseudorandom patterns up to 2^{31} - 1
- A repetitive pattern from 1 to 32 bits in length
- Alternating (16-bit) words that alternate every 1 to 256 words

The BERT receiver has a 24-bit error counter and 32-bit bit counter to allow testing to proceed for long periods without host processor intervention. It can generate interrupts on detecting a bit error, a change in synchronization, or a counter overflow. The BERT can be selected to transmit and receive on the line side or the equipment side. The synchronization algorithm works on a 32-bit block of data, not in a sliding window fashion.

The DS3/E3 formatter can be configured to transmit AIS when the BERT is not being used to test the far end, such as when DLB is active or when BM[1:0] = 1X. When DLB is active, the BERT is used to test the inner workings of the chip, and when BM[1:0] = 1X, the BERT is used to test devices connected on the equipment side (TDAT and RDAT). In either case, BERT patterns are transmitted to the far end on TPOS and TNEG unless the DS3/E3 formatter is configured to transmit AIS by setting T3E3CR1:TAIS = 1.

7.9.1 BERT Register Description

Table 7-G. BERT Register Map

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
30h	BCR1	BM1	BM0	BENA	TINV	RINV	RESYNC	TC	LC
31h	BCR2	N/A	PS2	PS1	PS0	RPL3	RPL2	RPL1	RPL0
32h	BCR3	N/A	N/A	N/A	N/A	EIB2	EIB1	EIB0	SBE
33h	BCR4	AWC7	AWC6	AWC5	AWC4	AWC3	AWC2	AWC1	AWC0
38h	BSR	N/A	N/A	RA1	RA0	N/A	BBCO	BECO	SYNC
39h	BSRL	N/A	N/A	RA1L	RA0L	BEDL	BBCOL	BECOL	SYNCL
3Ah	BSRIE	N/A	N/A	N/A	N/A	BEDIE	BBCOIE	BECOIE	SYNCIE
3Ch	BRPR1	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
3Dh	BRPR2	RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
3Eh	BRPR3	RP23	RP22	RP21	RP20	RP19	RP18	RP17	RP16
3Fh	BRPR4	RP31	RP30	RP29	RP28	RP27	RP26	RP25	RP24
40h	BBCR1	BBC7	BBC6	BBC5	BBC4	BBC3	BBC2	BBC1	BBC0
41h	BBCR2	BBC15	BBC14	BBC13	BBC12	BBC11	BBC10	BBC9	BBC8
42h	BBCR3	BBC23	BBC22	BBC21	BBC20	BBC19	BBC18	BBC17	BBC16
43h	BBCR4	BBC31	BBC30	BBC29	BBC28	BBC27	BBC26	BBC25	BBC24
44h	BBECR1	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
45h	BBECR2	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
46h	BBECR3	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16

Register Name: **BCR1**
Register Description: **BERT Control Register 1**
Register Address: **30h**

Bit #	7	6	5	4	3	2	1	0
Name	BM1	BM0	BENA	TINV	RINV	RESYNC	TC	LC
Default	0	0	0	0	0	0	0	0

Bit 0: Load Bit and Error Counts (LC). A low-to-high transition latches the current bit and error counts into the host-processor-accessible registers BBCR and BBECR and then clears the internal counters. This bit should be toggled from low to high whenever the host processor wishes to begin a new acquisition period. Must be cleared and set again for subsequent loads.

Bit 1: Transmit Pattern Load (TC). A low-to-high transition loads the pattern generator. This bit should be toggled from low to high whenever the host processor loads a new pattern or needs to resynchronize to an existing pattern. Must be cleared and set again for subsequent loads. For pseudorandom patterns, PS[2:0] must be configured before toggling TC. For repetitive patterns, PS[2:0], RPL[3:0], and RP[31:0] must be configured before toggling TC. For alternating word patterns, PS[2:0], AWC[7:0], and RP[31:0] must be configured before toggling TC.

Bit 2: Force Resynchronization (RESYNC). A low-to-high transition forces the receive BERT synchronizer to resynchronize to the incoming data stream. This bit should be toggled from low to high whenever the host processor wishes to acquire synchronization on a new pattern. Must be cleared and set again for a subsequent resynchronization.

Bit 3: Receive Invert Data Enable (RINV)
0 = do not invert the incoming data stream
1 = invert the incoming data stream

Bit 4: Transmit Invert Data Enable (TINV)
0 = do not invert the outgoing data stream
1 = invert the outgoing data stream

Bit 5: BERT Enable (BENA). This bit is used to enable the BERT transmitter, replacing the payload, or the entire DS3/E3 signal (depending on the setting of BM[1:0]). The BERT receiver is always enabled. Configure all BERT control and pattern registers and toggle the TC control bit before setting BENA.
0 = disable BERT transmitter
1 = enable BERT transmitter

Bits 6, 7: BERT Mode (BM[1:0]). These bits select whether the BERT pattern replaces only the DS3/E3 payload or the entire DS3/E3 frame (payload and overhead). These bits also select the BERT transmit direction: line side (TPOS/TNEG and RPOS/RNEG) or equipment side (TDAT and RDAT).

BM[1:0]	DATA	TRANSMIT	RECEIVE
00	Payload	TPOS/TNEG	RPOS/RNEG
01	Entire frame	TPOS/TNEG	RPOS/RNEG
10	Payload	RDAT	TDAT
11	Entire frame	RDAT	TDAT

Register Name: **BCR2**
Register Description: **BERT Control Register 2**
Register Address: **31h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	PS2	PS1	PS0	RPL3	RPL2	RPL1	RPL0
Default	—	0	0	0	0	0	0	0

Bits 0 to 3: Repetitive Pattern Length (RPL[3:0]). RPL3 is the MSB and RPL0 is the LSB of a nibble that describes how long the repetitive pattern is. The valid range is 17 (0000) to 32 (1111). These bits are ignored if the BERT is programmed for a pseudorandom pattern or an alternating word pattern. To create repetitive patterns fewer than 17 bits in length, the user must set the length to an integer multiple of the desired length that is less than or equal to 32. For example, to create a 6-bit pattern, set the length to 18 (0001), 24 (0111), or 30 (1101).

Length	Code	Length	Code	Length	Code	Length	Code
17 bits	0000	18 bits	0001	19 bits	0010	20 bits	0011
21 bits	0100	22 bits	0101	23 bits	0110	24 bits	0111
25 bits	1000	26 bits	1001	27 bits	1010	28 bits	1011
29 bits	1100	30 bits	1101	31 bits	1110	32 bits	1111

Bits 4 to 6: Pattern Select (PS[2:0]). This field specifies the type of pattern to be generated. After configuring these bits, the TC bit in the BCR1 register must be toggled to reconfigure the pattern generator.

PS[2:0]	PATTERN	TAPS	SPECIFICATION	TINV	RINV
000	Repetitive Pattern	—	—	—	—
001	Alternating Word Pattern	—	—	—	—
010	2^{15} - 1	14, 15	ITU O.151 (for DS3)	1	1
011	2^{20} - 1 QRSS	17, 20	T1.403	0	0
100	2^{23} - 1	18, 23	ITU O.151 (for E3)	1	1
101	2^{31} - 1	28, 31	(none)	0	0
110	Invalid	—	—	—	—
111	Invalid	—	—	—	—

Register Name: **BCR3**
Register Description: **BERT Control Register 3**
Register Address: **32h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	EIB2	EIB1	EIB0	SBE
Default	—	—	—	—	0	0	0	0

Bit 0: Single Bit-Error Insert (SBE). A low-to-high transition creates a single bit error. Must be cleared and set again for a subsequent bit error to be inserted.

Bits 1 to 3: Error Insert Bits (EIB[2:0]). Automatically insert bit errors at the prescribed rate into the generated data pattern. Useful for verifying error detection operation.

EIB[2:0]	ERROR RATE INSERTED
000	No errors automatically inserted
001	10^{-1} (1 error per 10 bits)
010	10^{-2} (1 error per 100 bits)
011	10^{-3} (1 error per 1000 bits)
100	10^{-4} (1 error per 10,000 bits)
101	10^{-5} (1 error per 100,000 bits)
110	10^{-6} (1 error per 1,000,000 bits)
111	10^{-7} (1 error per 10,000,000 bits)

Register Name: **BCR4**
Register Description: **BERT Control Register 4**
Register Address: **33h**

Bit #	7	6	5	4	3	2	1	0
Name	AWC7	AWC6	AWC5	AWC4	AWC3	AWC2	AWC1	AWC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7: Alternating Word Count Rate (AWC[7:0]). When the BERT is programmed in the alternating word mode, it transmits the word in register RP[15:0] a number of times equal to AWC[7:0] + 1 and then transmits the word loaded in RP[31:16] the same number of times. The valid count range is from 00h to FFh. These bits are ignored if the BERT is programmed for a pseudorandom pattern or a repetitive pattern.

AWC VALUE	ALTERNATING COUNT ACTION
00h	Send the word in RP[15:0] **1** time followed by the word in RP[31:16] **1** time…
01h	Send the word in RP[15:0] **2** times followed by the word in RP[31:16] **2** times…
02h	Send the word in RP[15:0] **3** times followed by the word in RP[31:16] **3** times…
. . .	. . .
FFh	Send the word in RP[15:0] **256** times followed by the word in RP[31:16] **256** times…

Register Name: **BSR**
Register Description: **BERT Status Register**
Register Address: **38h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	RA1	RA0	N/A	BBCO	BECO	SYNC
Default	—	—	—	—	—	—	—	—

Bit 0: Synchronization Status (SYNC). This real-time status bit is set when the incoming pattern matches for 32 consecutive bit positions. SYNC bit is cleared when six or more bits out of 64 are received in error.

Bit 1: BERT Error-Counter Overflow (BECO). This real-time status bit is set when the 24-bit BERT error counter (BEC) saturates. BECO is cleared when BCR1:LC is toggled to load the error counts.

Bit 2: BERT Bit-Counter Overflow (BBCO). This real-time status bit is set when the 32-bit BERT bit counter (BBC) saturates. BBCO is cleared when BCR1:LC is toggled to load the error counts.

Bit 4: Receive All Zeros (RA0). This real-time status bit is set when 32 consecutive 0s are received. RA0 is cleared when a 1 is received.

Bit 5: Receive All Ones (RA1). This real-time status bit is set when 32 consecutive 1s are received. RA1 is cleared when a 0 is received.

Register Name: **BSRL**
Register Description: **BERT Status Register Latched**
Register Address: **39h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	RA1L	RA0L	BEDL	BBCOL	BECOL	SYNCL
Default	—	—	—	—	—	—	—	—

Note: *See Figure 7-6 for details on the interrupt logic for the status bits in the BSRL register.*

Bit 0: Synchronization Status Latched (SYNCL). This latched status bit is set to 1 when the SYNC status bit in the BSR register changes state (low to high or high to low). To determine if this bit was set because of finding synchronization or losing synchronization, read the SYNC real-time status bit in the BSR register. SYNCL is cleared when the host processor writes a 1 to it and is not set again until SYNC changes state again. When SYNCL is set, it can cause a hardware interrupt to occur if the SYNCIE bit in the BSRIE register and the BERTIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 1: BERT Error-Counter Overflow Latched (BECOL). This latched status bit is set to 1 when the BECO status bit in the BSR register goes high. BECOL is cleared when the host processor writes a one to it and is not set again until BECO goes high again. When BECOL is set, it can cause a hardware interrupt to occur if the BECOIE bit in the BSRIE register and the BERTIE bit in the MSRIE register are both set to a 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 2: BERT Bit-Counter Overflow Latched (BBCOL). This latched status bit is set to 1 when the BBCO status bit in the BSR register goes high. BBCOL is cleared when the host processor writes a 1 to it and is not set again until BBCO goes high again. When BBCOL is set, it can cause a hardware interrupt to occur if the BBCOIE bit in the BSRIE register and the BERTIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 3: Bit Error-Detected Latched (BEDL). This latched status bit is set to 1 when a bit error is detected. The receive BERT must be in synchronization to detect bit errors. BEDL is cleared when the host processor writes a 1 to it. When BEDL is set it can cause a hardware interrupt to occur if the BEDIE bit in the BSRIE register and the BERTIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 4: Receive All-Zeros Latched (RA0L). This latched status bit is set to 1 when the RA0 bit in the BSR register is set. RA0L is cleared when the host processor writes a 1 to it. RA0L cannot cause an interrupt.

Bit 5: Receive All-Ones Latched (RA1L). This latched status bit is set to 1 when the RA1 bit in the BSR register is set. RA1L is cleared when the host processor writes a 1 to it. RA1L cannot cause an interrupt.

Register Name: **BSRIE**
Register Description: **BERT Status Register Interrupt Enable**
Register Address: **3Ah**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	BEDIE	BBCOIE	BECOIE	SYNCIE
Default	—	—	—	—	0	0	0	0

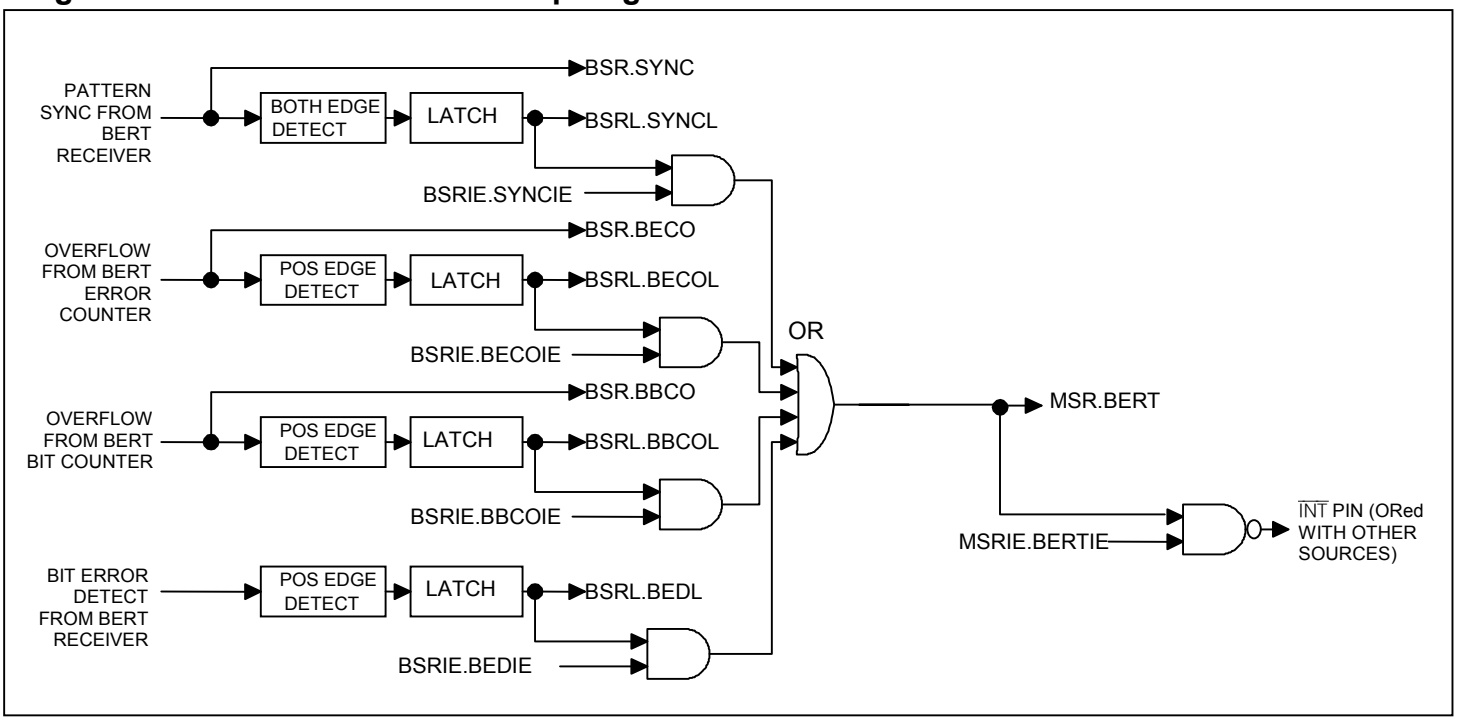
Bit 0: Synchronization Status Interrupt Enable (SYNCIE). This bit enables an interrupt if the SYNCL bit in the BSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 1: BERT Error-Counter Overflow Interrupt Enable (BECOIE). This bit enables an interrupt if the BECOL bit in the BSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 2: BERT Bit-Counter Overflow Interrupt Enable (BBCOIE). This bit enables an interrupt if the BBCOL bit in the BSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 3: Bit Error-Detected Interrupt Enable (BEDIE). This bit enables an interrupt if the BEDL bit in the BSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Figure 7-6. BERT Status Bit Interrupt Signal Flow



Register Name: **BRPR1**
Register Description: **BERT Repetitive Pattern Register 1 (lower byte)**
Register Address: **3Ch**

Bit #	7	6	5	4	3	2	1	0
Name	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
Default	0	0	0	0	0	0	0	0

Register Name: **BRPR2**
Register Description: **BERT Repetitive Pattern Register 2**
Register Address: **3Dh**

Bit #	7	6	5	4	3	2	1	0
Name	RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
Default	0	0	0	0	0	0	0	0

Register Name: **BRPR3**
Register Description: **BERT Repetitive Pattern Register 3**
Register Address: **3Eh**

Bit #	7	6	5	4	3	2	1	0
Name	RP23	RP22	RP21	RP20	RP19	RP18	RP17	RP16
Default	0	0	0	0	0	0	0	0

Register Name: **BRPR4**
Register Description: **BERT Repetitive Pattern Register 4 (upper byte)**
Register Address: **3Fh**

Bit #	7	6	5	4	3	2	1	0
Name	RP31	RP30	RP29	RP28	RP27	RP26	RP25	RP24
Default	0	0	0	0	0	0	0	0

Bits 0 to 31: BERT Repetitive Pattern (RP[31:0]). These registers must be configured for the BERT to properly generate and synchronize to a repetitive pattern or an alternating word pattern. For an alternating word pattern, the first word to be transmitted should be placed into RP[15:0], and the second word should be placed into RP[31:16]. In the first word, RP0 is the LSB and is transmitted first. In the second word, RP16 is the LSB and is transmitted first. For repetitive patterns, RP0 is the LSB and is transmitted first, while the MSB is determined by the repetitive pattern length, RPL[3:0].

An alternating word example: To use the DDS stress pattern “7E,” set BRPR1 = BRPR2 = 00h, BRPR3 = BRPR4 = 7Eh. When AWC[7:0] is set to 49 (decimal), the BERT sends and detects (49 + 1) x 2 = 100 bytes of 00h followed by 100 bytes of 7Eh.

Register Name: **BBCR1**
Register Description: **BERT Bit Counter Register 1 (lower byte)**
Register Address: **40h**

Bit #	7	6	5	4	3	2	1	0
Name	BBC7	BBC6	BBC5	BBC4	BBC3	BBC2	BBC1	BBC0
Default	0	0	0	0	0	0	0	0

Register Name: **BBCR2**
Register Description: **BERT Bit Counter Register 2**
Register Address: **41h**

Bit #	7	6	5	4	3	2	1	0
Name	BBC15	BBC14	BBC13	BBC12	BBC11	BBC10	BBC9	BBC8
Default	0	0	0	0	0	0	0	0

Register Name: **BBCR3**
Register Description: **BERT Bit Counter Register 3**
Register Address: **42h**

Bit #	7	6	5	4	3	2	1	0
Name	BBC23	BBC22	BBC21	BBC20	BBC19	BBC18	BBC17	BBC16
Default	0	0	0	0	0	0	0	0

Register Name: **BBCR4**
Register Description: **BERT Bit Counter Register 4 (upper byte)**
Register Address: **43h**

Bit #	7	6	5	4	3	2	1	0
Name	BBC31	BBC30	BBC29	BBC28	BBC27	BBC26	BBC25	BBC24
Default	0	0	0	0	0	0	0	0

Bits 0 to 31: BERT Bit Counter (BBC[31:0]). The BBCR registers are loaded with the value of the internal BERT bit counter when the LC control bit in the BCR1 register is toggled. This 32-bit counter increments for each data bit received. The bit counter starts counting when the BERT goes into receive synchronization (SYNC = 1) and continues counting even if the BERT loses sync. The bit counter saturates and does not roll over. Upon saturation, the BBCO status bit in the BSR register is set. When the LC bit is toggled, the bit count is loaded into the BBCR registers and the internal bit counter is cleared. If the BERT is in sync when LC is toggled, the bit counter continues to count up from zero. If the BERT is out of sync when LC is toggled, the bit counter is held at zero until the BERT regains sync. The host processor should toggle LC after the BERT has synchronized and then toggle LC again when the error-checking period is complete. If the framer loses synchronization during this period, then the counting results are suspect.

Register Name: **BBECR1**
Register Description: **BERT Bit-Error Counter Register 1 (lower byte)**
Register Address: **44h**

Bit #	7	6	5	4	3	2	1	0
Name	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
Default	0	0	0	0	0	0	0	0

Register Name: **BBECR2**
Register Description: **BERT Bit Error Counter Register 2**
Register Address: **45h**

Bit #	7	6	5	4	3	2	1	0
Name	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
Default	0	0	0	0	0	0	0	0

Register Name: **BBECR3**
Register Description: **BERT Bit Error Counter Register 3 (upper byte)**
Register Address: **46h**

Bit #	7	6	5	4	3	2	1	0
Name	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
Default	0	0	0	0	0	0	0	0

Bits 0 to 23: BERT Bit-Error Counter (BEC[23:0]). The BBECR registers are loaded with the value of the internal BERT error counter when the LC control bit in the BCR1 register is toggled. This 24-bit counter increments for each received data bit that does not match the expected pattern. The error counter starts counting when the BERT goes into receive synchronization (SYNC = 1) and continues counting even if the BERT loses sync. The error counter saturates and does not roll over. Upon saturation, the BECO status bit in the BSR register is set. When the LC bit is toggled, the error count is loaded into the BBECR registers and the internal error counter is cleared. If the BERT is in sync when LC is toggled, the error counter continues to count up from zero. If the BERT is out of sync when LC is toggled, the error counter is held at zero until the BERT regains sync. The host processor should toggle LC after the BERT has synchronized and then toggle LC again when the error-checking period is complete. If the framer loses synchronization during this period, then the counting results are suspect.

7.10 HDLC Controller

Each framer contains an on-board HDLC controller with 256-byte buffers in the transmit and receive paths. When the framer is operated in the DS3 C-Bit Parity mode, the HDLC transmitter and receiver are connected to the three C-bits in M-subframe 5. When the framer is operated in the E3 mode, the user has the option to connect the HDLC transmitter to the Sn bit, while the HDLC receiver is always connected to the Sn bit in the receive data. If the host processor does not wish to use the HDLC controller for the Sn bit, then the status provided by the HDLC controller should be ignored. On the transmit side, the host processor selects the source of the Sn bit through the E3SnC0 and E3SnC1 controls bits in the T3E3CR1 register. The HDLC controller is not used in the DS3 M23 mode.

7.10.1 Receive Operation

On reset, the receive HDLC controller flushes the receive FIFO and begins searching for a new incoming HDLC packet. It then performs a bit-by-bit search for an HDLC packet and when one is detected, it zero destuffs the incoming data stream, automatically byte aligns to it, and places the incoming bytes into the receive FIFO as they are received. The first byte of each packet is marked in the receive FIFO by setting the opening byte (OBYTE) bit. Upon detecting a closing flag, the receive HDLC controller checks the 16-bit CRC to see if the packet is valid or not and then marks the last byte of the packet in the receive FIFO by setting the closing byte (CBYTE) bit. The CRC is not passed to the receive FIFO. When the CBYTE bit is set, the host processor can obtain the status of the incoming packet through the packet status bits (PS0 and PS1). Incoming packets can be separated by as few as one flag or by two flags that share a common zero. If the receive FIFO ever fills beyond capacity, the rest of the incoming packet data is discarded, and the receive FIFO overrun (ROVRL) status bit is set. If such a scenario occurs, then the last packet in the FIFO is suspect and should be discarded. When an overflow occurs, the receive

HDLC controller stops accepting packets until either the FIFO is completely emptied or reset. If the receive HDLC detects an incoming abort (seven or more 1s in a row), it sets the receive abort sequence-detected (RABTL) status bit. If an abort sequence is detected in the middle of an incoming packet, then the receive HDLC controller sets the packet status bits accordingly in the receive FIFO.

The receive HDLC controller has been designed to minimize its real-time host processor support requirements. The 256-byte receive FIFO is deep enough to store the three DS3 packets (path ID, idle signal ID, and test signal ID) that arrive once a second. Thus, in DS3 applications the host processor only needs to read the receive HDLC FIFO once a second to retrieve the three messages. The host processor can be notified when the beginning of a new packet is received (receive packet-start status bit) and when the end of a packet is received (receive packet-end status bit). Also, the host processor can be notified when the FIFO has filled beyond a programmable level called the high watermark. The host processor reads the incoming packet data out of the receive FIFO one byte at a time. When the receive FIFO is empty, the REMPTY bit in the HDLC information register (HIR) is set.

7.10.2 Transmit Operation

On reset, the transmit HDLC controller flushes the transmit FIFO and transmits an abort followed by either 7Eh or FFh (depending on the setting of the TFS control bit) continuously. The transmit HDLC controller then waits until there are at least two bytes in the transmit FIFO before starting to send the packet. The transmit HDLC automatically adds an opening flag of 7Eh to the beginning of the packet and zero stuffs the outgoing data stream. When the transmit HDLC controller detects that the TMEND bit in the transmit FIFO is set, it automatically calculates and appends the 16-bit CRC checksum followed by a closing flag of 7Eh. If the FIFO is empty, the transmit HDLC controller sends either 7Eh or FFh continuously. When new data arrives in the FIFO, the transmit HDLC automatically transmits the opening flag and begins sending the next packet. Between consecutive packets, there are always at least two flags. If the transmit FIFO ever empties when a packet is being sent (i.e., before the TMEND bit is set), then the transmit HDLC controller sets the transmit FIFO underrun (TUDRL) status bit and sends an abort of seven 1s in a row (FEh) followed by continuous transmission of either 7Eh (flags) or FFh (idle). When the FIFO underruns, the transmit HDLC controller should be reset by the host processor.

The transmit HDLC controller has been designed to minimize its real-time host processor support requirements. The 256-byte transmit FIFO is deep enough to store the three DS3 packets (path ID, idle signal ID, and test signal ID) that should be sent once a second. Thus, in DS3 applications the host processor only needs to write the transmit HDLC FIFO once a second to send the three messages. Once the host processor has written an outgoing packet, it can monitor the transmit packet-end (TENDL) status bit to know when the packet has been sent. Also, the host processor can be notified when the FIFO has emptied below a programmable level called the low watermark. The host processor must never overfill the FIFO. To keep this from occurring, the host processor can obtain the real-time depth of the transmit FIFO through the transmit FIFO level bits in the HDLC information register (HIR).

7.10.3 HDLC Register Description

Table 7-H. HDLC Register Map

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
50h	HCR1	RHR	THR	RID	TID	TFS	TZSD	TCRCI	TCRCD
51h	HCR2	N/A	RHWMS2	RHWMS1	RHWMS0	N/A	TLWMS2	TLWMS1	TLWMS0
54h	HSR	N/A	N/A	N/A	N/A	RHWM	TLWM	N/A	N/A
55h	HSRL	ROVRL	RPEL	RPSL	RABTL	RHWML	TLWML	TUDRL	TENDL
56h	HSRIE	ROVRIE	RPEIE	RPSIE	RABTIE	RHWMIE	TLWMIE	TUDRIE	TENDIE
57h	HIR	N/A	N/A	REMPTY	TEMPTY	TFL3	TFL2	TFL1	TFL0
5Ch	RHDLC1	D7	D6	D5	D4	D3	D2	D1	D0
5Dh	RHDLC2	N/A	N/A	N/A	N/A	PS1	PS0	CBYTE	OBYTE
5Eh	THDLC1	D7	D6	D5	D4	D3	D2	D1	D0
5Fh	THDLC2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	TMEND

Register Name: **HCR1**
Register Description: **HDLC Control Register 1**
Register Address: **50h**

Bit #	7	6	5	4	3	2	1	0
Name	RHR	THR	RID	TID	TFS	TZSD	TCRCI	TCRCD
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit CRC Defeat (TCRCD). When this bit is logic 0, the transmit HDLC controller automatically calculates and appends the 16-bit CRC to the outgoing HDLC message. When this bit is logic 1, the transmit HDLC controller does not append the CRC to the outgoing message.
0 = enable CRC generation (normal operation)
1 = disable CRC generation

Bit 1: Transmit CRC Invert (TCRCI). When this bit is logic 0, the transmit HDLC controller generates the CRC normally. When this bit is logic 1, the transmit HDLC controller inverts all 16 bits of the generated CRC. This bit is ignored when CRC generation is disabled (TCRCD = 1). This bit is useful in testing HDLC operation.
0 = do not invert the generated CRC (normal operation)
1 = invert the generated CRC

Bit 2: Transmit Zero Stuffer Defeat (TZSD). When this bit is logic 0, the transmit HDLC controller performs zero stuffing on all data between the opening and closing flags of the HDLC message. When this bit is logic 1, the transmit HDLC controller does not perform zero stuffing.
0 = enable zero stuffing (normal operation)
1 = disable zero stuffing

Bit 3: Transmit Flag/Idle Select (TFS). This control bit determines whether flags or idle bytes are transmitted between packets.
0 = 7Eh (flags)
1 = FFh (idle)

Bit 4: Transmit Invert Data (TID). When this bit is logic 1, the entire transmit HDLC data stream (including flags and CRC checksum) is inverted before being transmitted by the DS3/E3 formatter.
0 = do not invert transmit HDLC data stream (normal operation)
1 = invert transmit HDLC data stream

Bit 5: Receive Invert Data (RID). When this bit is logic 1, the entire receive HDLC data stream (including flags and CRC checksum) is inverted before processing by the receive HDLC controller.
0 = do not invert receive HDLC data stream (normal operation)
1 = invert receive HDLC data stream

Bit 6: Transmit HDLC Reset (THR). A 0-to-1 transition resets the transmit HDLC controller. A reset flushes the transmit FIFO and causes the transmit HDLC controller to transmit one FEh abort sequence (seven 1s in a row) followed by continuous transmission of either 7Eh (flags) or FFh (idle) until the beginning of a new packet (at least two bytes) is written into the transmit HDLC FIFO.

Bit 7: Receive HDLC Reset (RHR). A 0-to-1 transition resets the receive HDLC controller. A reset flushes the current contents of the receive FIFO and causes the receive HDLC controller to begin searching for a new incoming HDLC packet.

Register Name: **HCR2**
Register Description: **HDLC Control Register 2**
Register Address: **51h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	RHWMS2	RHWMS1	RHWMS0	N/A	TLWMS2	TLWMS1	TLWMS0
Default	—	0	0	0	—	0	0	0

Bits 2 to 0: Transmit Low Watermark Select Bits (TLWMS[2:0]). These control bits determine when the HDLC controller should set the TLWM status bit in the HSR register. When the transmit FIFO contains less than the number of bytes specified by these bits, the TLWM status bit is set to logic 1.

TLWMS[2:0]	TRANSMIT LOW WATERMARK (BYTES)
000	16
001	48
010	80
011	112
100	144
101	176
110	208
111	240

Bits 4 to 6: Receive High Watermark Select Bits (RHWMS[2:0]). These control bits determine when the HDLC controller should set the RHWM status bit in the HSR register. When the receive FIFO contains more than the number of bytes specified by these bits, the RHWM status bit is set to logic 1.

RHWMS[2:0]	RECEIVE HIGH WATERMARK (BYTES)
000	16
001	48
010	80
011	112
100	144
101	176
110	208
111	240

Register Name: **HSR**
Register Description: **HDLC Status Register**
Register Address: **54h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	RHWM	TLWM	N/A	N/A
Default	—	—	—	—	—	—	—	—

Bit 2: Transmit FIFO Low Watermark (TLWM). This real-time status bit is set to 1 when the transmit FIFO contains less than the number of bytes configured by TLWMS[2:0] control bits in the HCR2 register. This bit is cleared when the FIFO fills beyond the low watermark.

Bit 3: Receive FIFO High Watermark (RHWM). This real-time status bit is set to 1 when the receive FIFO contains more than the number of bytes configured by the RHWMS[2:0] control bits in the HCR2 register. This bit is cleared when the FIFO empties below the high watermark.

Register Name: **HSRL**
Register Description: **HDLC Status Register Latched**
Register Address: **55h**

Bit #	7	6	5	4	3	2	1	0
Name	ROVRL	RPEL	RPSL	RABTL	RHWML	TLWML	TUDRL	TENDL
Default	—	—	—	—	—	—	—	—

Note: *See Figure 7-7 for details on the interrupt signal flow for the status bits in the HSRL register.*

Bit 0: Transmit Packet-End Latched (TENDL). This latched status bit is set to 1 each time the transmit HDLC controller reads a transmit FIFO byte with the corresponding TMEND bit set or when a FIFO underrun occurs. TENDL is cleared when the host processor writes a 1 to it. When TENDL is set, it can cause a hardware interrupt to occur if the TENDIE bit in the HSRIE register and the HDLCIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 1: Transmit FIFO Underrun Latched (TUDRL). This latched status bit is set to 1 each time the transmit FIFO underruns. TUDRL is cleared when the host processor writes a 1 to it and is not set again until another underrun occurs (i.e., the FIFO has been written to and then allowed to empty again without the TMEND bit set). When TUDRL is set, it can cause a hardware interrupt to occur if the TUDRIE bit in the HSRIE register and the HDLCIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 2: Transmit FIFO Low Watermark Latched (TLWML). This latched status bit is set to 1 when the TLWM status bit in the HSR register goes high. TLWML is cleared when the host processor writes a 1 to it and is not set again until TLWM goes high again. When TLWML is set, it can cause a hardware interrupt to occur if the TLWMIE bit in the HSRIE register and the HDLCIE bit in the MSRIE register are both set to one. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 3: Receive FIFO High Watermark Latched (RHWML). This latched status bit is set to 1 when the RHWM status bit in the HSR register goes high. RHWML is cleared when the host processor writes a one to it and is not set again until RHWM goes high again. When RHWML is set, it can cause a hardware interrupt to occur if the RHWMIE bit in the HSRIE register and the HDLCIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 4: Receive Abort Sequence Detected Latched (RABTL). This latched status bit is set to 1 each time the receive HDLC controller detects an abort sequence (seven or more 1s in a row) during packet reception. If the receive HDLC is not currently receiving a packet, then receiving an abort sequence does not set this status bit. RABTL is cleared when the host processor writes a 1 to it and is not set again until another abort is detected (at least one valid flag must be detected before another abort can be detected). When RABTL is set, it can cause a hardware interrupt to occur if the RABTIE bit in the HSRIE register and the HDLCIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 5: Receive Packet-Start Latched (RPSL). This latched status bit is set to 1 each time the receive HDLC controller detects the start of an HDLC packet. RPSL is cleared when the host processor writes a 1 to it and is not set again until another start of packet is detected. When RPSL is set, it can cause a hardware interrupt to occur if the RPSIE bit in the HSRIE register and the HDLCIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 6: Receive Packet-End Latched (RPEL). This latched status bit is set to 1 each time the HDLC controller detects a closing flag during reception of a packet, regardless of whether the packet is valid (CRC correct) or not (bad CRC, abort sequence detected, packet too small, not an integral number of octets, or an overrun occurred). RPEL is cleared when the host processor writes a 1 to it and is not set again until another message end is detected. When RPEL is set, it can cause a hardware interrupt to occur if the RPEIE bit in the HSRIE register and the HDLCIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 7: Receive FIFO Overrun Latched (ROVRL). This latched status bit is set to 1 each time the receive FIFO overruns. ROVRL is cleared when the host processor writes a 1 to it and is not set again until another overrun occurs (i.e., the FIFO has been read from and then allowed to fill up again). When ROVRL is set, it can cause a hardware interrupt to occur if the ROVRIE bit in the HSRIE register and the HDLCIE bit in the MSRIE register are both set to 1. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Register Name: **HSRIE**
Register Description: **HDLC Status Register Interrupt Enable**
Register Address: **56h**

Bit #	7	6	5	4	3	2	1	0
Name	ROVRIE	RPEIE	RPSIE	RABTIE	RHWMIE	TLWMIE	TUDRIE	TENDIE
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Packet-End Interrupt Enable (TENDIE). This bit enables an interrupt if the TENDL bit in the HSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 1: Transmit FIFO Underrun Interrupt Enable (TUDRIE). This bit enables an interrupt if the TUDRL bit in the HSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 2: Transmit FIFO Low Watermark Interrupt Enable (TLWMIE). This bit enables an interrupt if the TLWML bit in the HSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 3: Receive FIFO High Watermark Interrupt Enable (RHWMIE). This bit enables an interrupt if the RHWML bit in the HSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

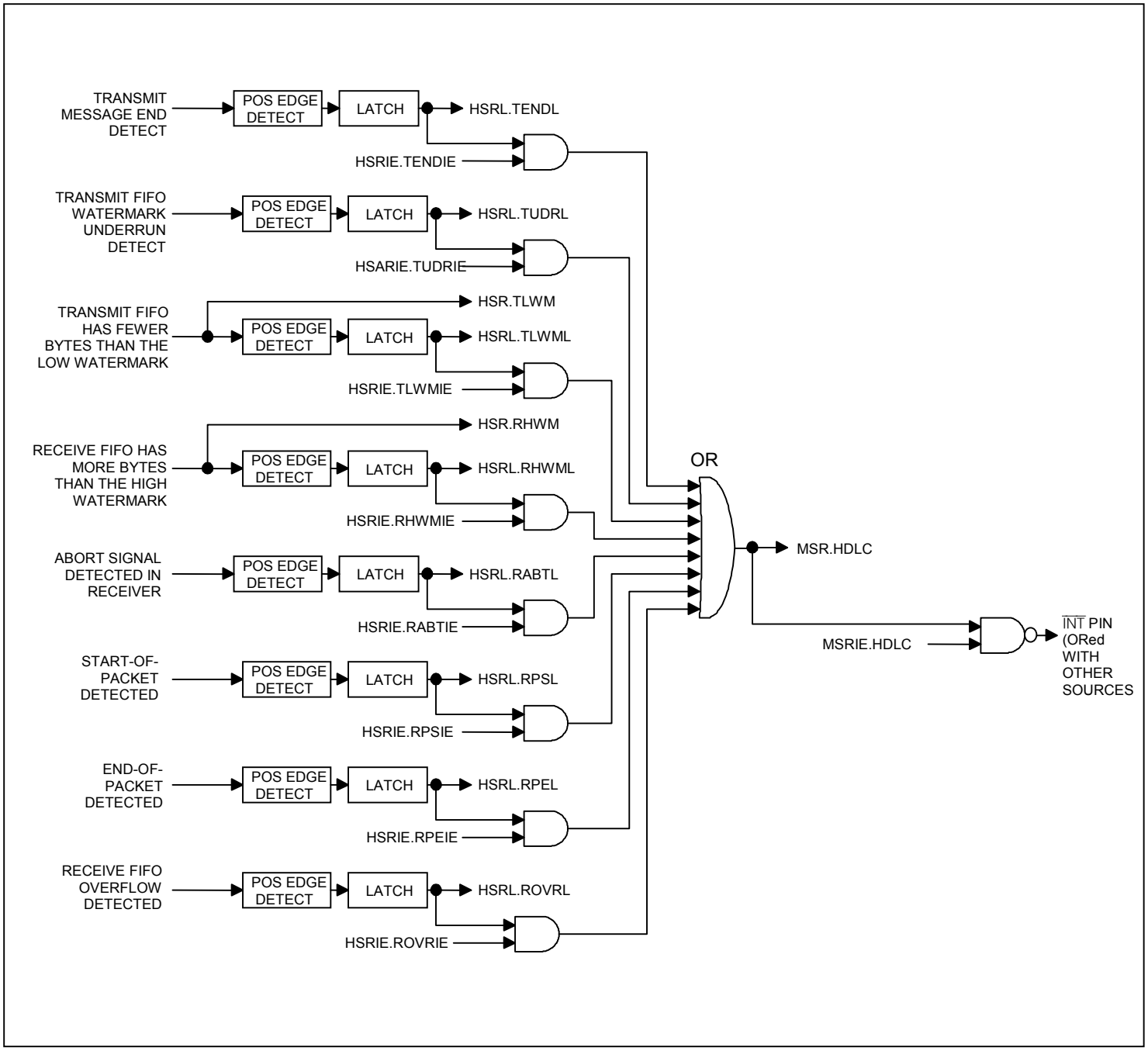
Bit 4: Receive Abort Sequence Detected Interrupt Enable (RABTIE). This bit enables an interrupt if the RABTL bit in the HSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 5: Receive Packet-Start Interrupt Enable (RPSIE). This bit enables an interrupt if the RPSL bit in the HSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 6: Receive Packet-End Interrupt Enable (RPEIE). This bit enables an interrupt if the RPEL bit in the HSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 7: Receive FIFO Overrun-Interrupt Enable (ROVRIE). This bit enables an interrupt if the ROVRL bit in the HSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Figure 7-7. HDLC Status Bit Interrupt Signal Flow



Register Name: **HIR**
Register Description: **HDLC Information Register**
Register Address: **57h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	REMPTY	TEMPTY	TFL3	TFL2	TFL1	TFL0
Default	—	—	—	—	—	—	—	—

Note: *Bits in this information register cannot cause an interrupt to occur.*

Bits 0 to 3: Transmit FIFO Level (TFL[3:0]). These real-time status bits indicate the current depth of the transmit FIFO in 16-byte increments.

TFL3	TFL2	TFL1	TFL0	TRANSMIT FIFO LEVEL (BYTES)
0	0	0	0	Empty to 15
0	0	0	1	16 to 31
0	0	1	0	32 to 47
0	0	1	1	48 to 63
0	1	0	0	64 to 79
0	1	0	1	80 to 95
0	1	1	0	96 to 111
0	1	1	1	112 to 127
1	0	0	0	128 to 143
1	0	0	1	144 to 159
1	0	1	0	160 to 175
1	0	1	1	176 to 191
1	1	0	0	192 to 207
1	1	0	1	208 to 223
1	1	1	0	224 to 239
1	1	1	1	240 to 256

Bit 4: Transmit FIFO Empty (TEMPTY). This real-time status bit is set when the transmit FIFO is empty and cleared when the transmit FIFO contains one or more bytes.

Bit 5: Receive FIFO Empty (REMPTY). This real-time status bit is set when the receive FIFO is empty and cleared when the receive FIFO contains one or more bytes.

Register Name: **RHDLC1**
Register Description: **Receive HDLC FIFO Data**
Register Address: **5Ch**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default	—	—	—	—	—	—	—	—

Note: *After the RHDLC2 register is read, the receive FIFO read pointer advances and both the RHDLC1 and RHDLC2 registers are updated with the next data/status from the receive FIFO. The host processor should read RHDLC1 first to retrieve the FIFO data and then immediately read RHDLC2 to retrieve the associated FIFO status bits.*

Bits 0 to 7: Receive FIFO Data (D[7:0]). These bits contain the next byte of receive FIFO data. D0 is the LSB and is the first bit received by the framer, while D7 is the MSB and is the last bit received. Reading this register does not cause the receive FIFO read pointer to advance.

Register Name: **RHDLC2**
Register Description: **Receive HDLC FIFO Status**
Register Address: **5Dh**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	PS1	PS0	CBYTE	OBYTE
Default	—	—	—	—	—	—	—	—

Bit 0: Opening Byte Indicator (OBYTE). This bit is set to 1 when the RHDLC1 register contains the first byte of an HDLC packet.

Bit 1: Closing Byte Indicator (CBYTE). This bit is set to 1 when the RHDLC1 register contains the last byte of an HDLC packet, whether the packet is valid or not. The host processor can check the PS[1:0] bits to determine packet validity.

Bits 2, 3: Packet Status (PS[1:0]). These bits are only valid when the CBYTE bit is set to 1. These bits indicate the validity of the incoming packet and the cause of the problem if the packet was received in error.

PS[1:0]	PACKET STATUS	REASON FOR INVALID RECEPTION OF THE PACKET
00	Valid	—
01	Invalid	Corrupt CRC
10	Invalid	Incoming packet was either too short (less than 4 bytes including the CRC) or did not contain an integral number of octets
11	Invalid	Abort sequence detected

Packets fewer than four bytes long (including the FCS) are invalid and the data that appears in the FIFO in such instances is meaningless. If only one byte is received between flags, then both the CBYTE and OBYTE bits are set. If two bytes are received, then OBYTE is set for the first byte received and CBYTE is set for the second byte received. If three bytes are received, then OBYTE is set for the first byte received and CBYTE is set for the third byte received. In all of these cases, the packet status is reported as PS[1:0] = 10, and the data in the FIFO should be ignored.

Register Name: **THDLC1**
Register Description: **Transmit HDLC FIFO Data**
Register Address: **5Eh**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

Note 1: *The host processor should always write to THDLC1 first followed by THDLC2. Writing to THDLC2 latches the data from both THDLC1 and THDLC2 into the transmit FIFO.*
Note 2: *THDLC1 and THDLC2 are write-only registers. Data read from these registers is undefined.*
Note 3: *The transmit FIFO can be filled to a maximum capacity of 256 bytes. When the transmit FIFO is full, it does not latch additional data.*

Bits 0 to 7: Transmit FIFO Data (D[7:0]). Data for the transmit FIFO is written to these bits. D0 is the LSB and is transmitted first, while D7 is the MSB and is transmitted last.

Register Name: **THDLC2**
Register Description: **Transmit HDLC FIFO Status**
Register Address: **5Fh**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	N/A	N/A	N/A	TMEND
Default	—	—	—	—	—	—	—	0

Bit 0: Transmit Message End (TMEND). This bit is used to delineate packets in the transmit FIFO. It should be set to 1 when the last byte of a message is written to the THDLC1 register. When set to 1, TMEND indicates that the message is complete and that the HDLC controller should calculate and append the CRC checksum (FCS) and at least two flags (7Eh). This bit should be set to 0 for all other data written to the FIFO. All outgoing HDLC messages must be at least two bytes long.

7.11 FEAC Controller

The DS3 C-Bit Parity far-end alarm and control (FEAC) channel carries repeating 16-bit codewords of the form 0xxxxxx011111111 (rightmost bit transmitted first), where x can be 0 or 1. These codewords are used to send alarm or status information from the far end to the near end, and send loopback commands to the far end.

Each DS314x framer contains an on-board FEAC controller. When the framer is in DS3 C-Bit Parity mode, the FEAC controller sources and sinks the FEAC channel (the third C-bit in M-subframe 1). When the framer is in E3 mode, the FEAC receiver is always connected to the E3 national bit (Sn, bit 12 of the E3 frame). If the host processor does not wish to use the FEAC controller for processing the E3 national bit, then it should ignore the status provided by the FEAC receiver. The FEAC transmitter can be provisioned to source the E3 national bit by setting T3E3CR1:E3SnC[1:0] = 10. The FEAC controller is not used in DS3 M23 framing mode.

The FEAC transmitter can be configured to transmit one codeword 10 times, one codeword continuously, or one codeword 10 times followed by another codeword 10 times. This last option is useful for sending loopback commands where the loopback activate/deactivate command must be followed by the code for line to be looped back. FEAC codewords are transmitted at least 10 times. When the FEAC transmitter is not sending codewords, it enters the idle state where it transmits all ones on the FEAC channel and sets the transmit FEAC idle bit (FSR:TFI) to 1.

The FEAC receiver does a bit-by-bit search for a data pattern matching the form of a FEAC codeword. When a codeword is found, the receiver validates the codeword by checking to see that the same codeword is found in three consecutive opportunities. After a codeword is validated, the receiver sets the receive FEAC codeword-detect status bit (FSR:RFCD) and writes the codeword into the receive FEAC FIFO for the host processor to read. The host processor can use the RFCD or receive FEAC FIFO empty (RFFE) status bits to know when to read the receive FEAC FIFO. The receive FEAC FIFO is four codewords deep. If the FIFO is full when the FEAC receiver attempts to write a new codeword, the new codeword is discarded and the receive FEAC FIFO Overflow status bit (RFFOL) is set. The FEAC receiver clears the RFCD status bit when the valid codeword is no longer present on the FEAC channel (i.e., when a different codeword is received twice in a row).

7.11.1 FEAC Register Description

Table 7-I. FEAC Register Map

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
60h	FCR	N/A	N/A	N/A	N/A	N/A	RFR	TFS1	TFS0
61h	FSR	N/A	N/A	N/A	N/A	RFFE	RFI	RFCD	TFI
62h	FSRL	N/A	N/A	N/A	RFFOL	RFFNL	RFIL	RFCDL	TFIL
63h	FSRIE	N/A	N/A	N/A	RFFOIE	RFFNIE	RFIIE	RFCDIE	TFIIE
64h	TFEACA	N/A	N/A	TFCA5	TFCA4	TFCA3	TFCA2	TFCA1	TFCA0
65h	TFEACB	N/A	N/A	TFCB5	TFCB4	TFCB3	TFCB2	TFCB1	TFCB0
66h	RFEAC	N/A	N/A	RFF5	RFF4	RFF3	RFF2	RFF1	RFF0

Register Name: **FCR**
Register Description: **FEAC Control Register**
Register Address: **60h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	N/A	RFR	TFS1	TFS0
Default	—	—	—	—	—	0	0	0

Bits 0, 1: Transmit FEAC Codeword Select Bits 0 and 1 (TFS[1:0]). These two bits control which of the two available codewords are to be generated. Both TFS0 and TFS1 are edge-triggered; a change from 00 to any other value starts the desired FEAC transmission. Actions 01 and 10 continue to completion even if TFS is subsequently written with 00. Action 11 transmits at least 10 codewords before being terminated by TFS = 00. To initiate a new action, the host must select the idle state (TFS = 00) before selecting the new action.

TFS[1:0]	ACTION
00	Idle state; do not generate a FEAC codeword (send all ones)
01	Send codeword A 10 times followed by all ones
10	Send codeword A 10 times followed codeword B 10 times followed by all ones
11	Send codeword A continuously (sent at least 10 times)

Bit 2: Receive FEAC Reset (RFR). A 0-to-1 transition resets the FEAC receiver and flushes the receive FEAC FIFO. This bit must be cleared before generating a subsequent reset.

Register Name: **FSR**
Register Description: **FEAC Status Register**
Register Address: **61h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	RFFE	RFI	RFCD	TFI
Default	—	—	—	—	—	—	—	—

Bit 0: Transmit FEAC Idle (TFI). This real-time status bit is set when the FEAC transmitter is sending the all-ones idle code. It is cleared when the FEAC transmitter is sending a FEAC codeword.

Bit 1: Receive FEAC Codeword Detected (RFCD). This real-time status bit is set each time the FEAC receiver has detected and validated a new FEAC codeword. It is cleared when the validated codeword is no longer present on the FEAC channel.

Bit 2: Receive FEAC Idle (RFI). This real-time status bit is set when the FEAC controller has detected 16 consecutive 1s. It is cleared when the FEAC receiver has detected and validated a new FEAC codeword.

Bit 3: Receive FEAC FIFO Empty (RFFE). This real-time status bit is set when the receive FEAC FIFO is empty, and thus RFF[5:0] contains no valid information. It is cleared when the receive FIFO contains one or more codewords.

Register Name: **FSRL**
Register Description: **FEAC Status Register Latched**
Register Address: **62h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	RFFOL	RFFNL	RFIL	RFCDL	TFIL
Default	—	—	—	—	—	—	—	—

Note: *See Figure 7-8 for details on the interrupt logic for the status bits in the BSRL register.*

Bit 0: Transmit FEAC Idle Latched (TFIL). This latched status bit is set to 1 when the TFI status bit in the FSR register goes high. TFIL is cleared when the host processor writes a 1 to it and is not set again until TFI goes high again. When TFIL is set, it can cause a hardware interrupt to occur if the TFIIE bit in the FSRIE register and the FEACIE bit in the MSRIE register are both set. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared. This bit can be used to determine when the FEAC codeword transmission has finished, and thus a new codeword can be transmitted.

Bit 1: Receive FEAC Codeword Detected Latched (RFCDL). This latched status bit is set to 1 when the RFCD status bit in the FSR register goes high. RFCDL is cleared when the host processor writes a one to it and is not set again until RFCD goes high again. When RFCDL is set, it can cause a hardware interrupt to occur if the RFCDIE bit in the FSRIE register and the FEACIE bit in the MSRIE register are both set. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Bit 2: Receive FEAC Idle Latched (RFIL). This latched status bit is set to 1 when the RFI status bit in the FSR register goes high. RFIL is cleared when the host processor writes a 1 to it and is not set again until RFI goes high again. When RFIL is set, it can cause a hardware interrupt to occur if the RFIIE bit in the FSRIE register and the FEACIE bit in the MSRIE register are both set. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared. This bit can be used to determine when the FEAC receiver has stopped receiving codewords, which can mark the end of an alarm situation.

Bit 3: Receive FEAC FIFO Not-Empty Latched (RFFNL). This latched status bit is set to 1 when the RFFE bit in the FSR register goes low. RFFNL is cleared when the host processor writes a 1 to it and is not set again until the RFFE bit goes low again. When RFFNL is set, it can cause a hardware interrupt to occur if the RFFNIE bit in the FSRIE register and the FEACIE bit in the MSRIE register are both set. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared. This bit can be used to determine when to read FEAC codeword(s) from the FIFO.

Bit 4: Receive FEAC FIFO Overflow Latched (RFFOL). This latched status bit is set to 1 when the receive FEAC controller has attempted to write to an already full receive FEAC FIFO and the current incoming FEAC codeword is lost. RFFOL is cleared when the host processor writes a 1 to it and is not set again until another FIFO overflow occurs (i.e., the receive FEAC FIFO has been read and then fills beyond capacity). When RFFOL is set, it can cause a hardware interrupt to occur if the RFFOIE bit in the FSRIE register and the FEACIE bit in the MSRIE register are both set. The interrupt is cleared when this bit is cleared or one or both of the interrupt-enable bits are cleared.

Register Name: **FSRIE**
Register Description: **FEAC Status Register Interrupt Enable**
Register Address: **63h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	RFFOIE	RFFNIE	RFIIE	RFCDIE	TFIIE
Default	—	—	—	0	0	0	0	0

Bit 0: Transmit FEAC Idle Interrupt Enable (TFIIE). This bit enables an interrupt if the TFIL bit in the FSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

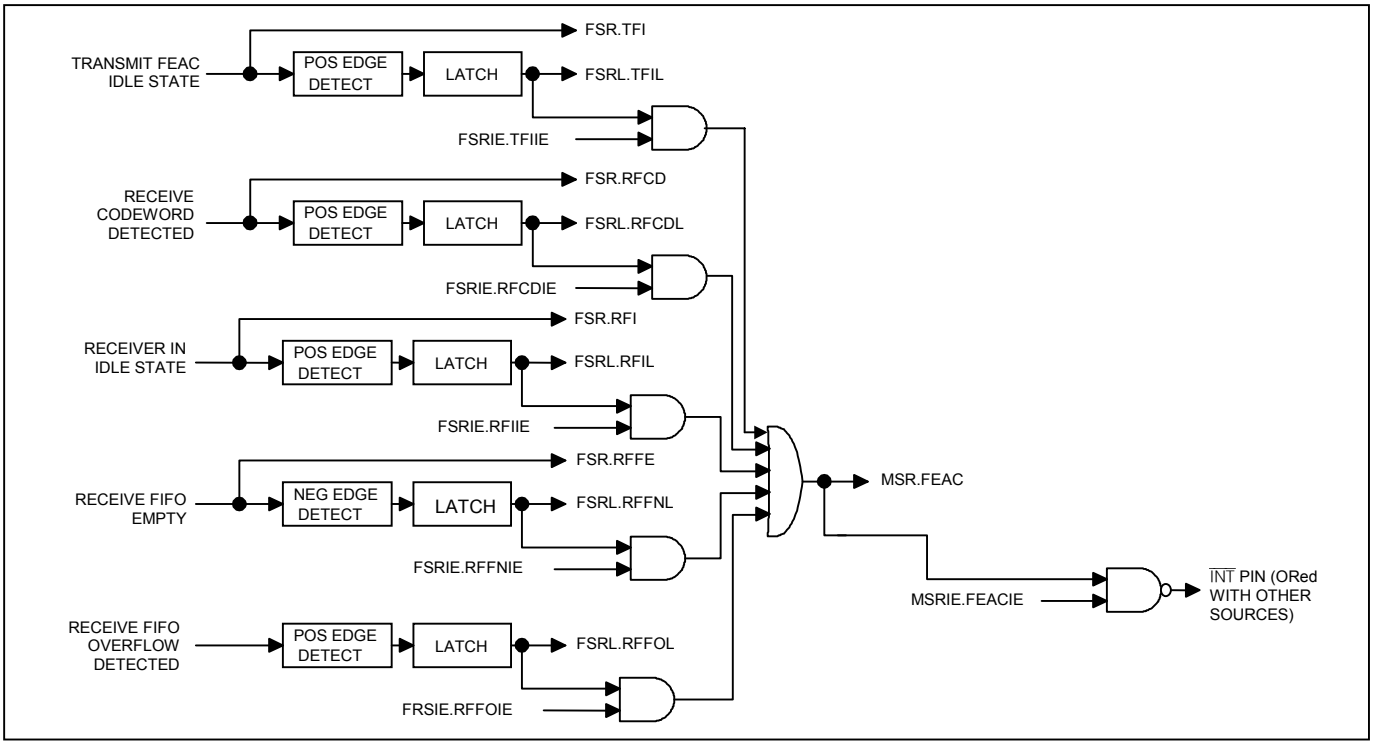
Bit 1: Receive FEAC Codeword Detected Interrupt Enable (RFCDIE). This bit enables an interrupt if the RFCDL bit in the FSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 2: Receive FEAC Idle Interrupt Enable (RFIIE). This bit enables an interrupt if the RFIL bit in the FSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 3: Receive FEAC FIFO Not-Empty Interrupt Enable (RFFNIE). This bit enables an interrupt if the RFFNL bit in the FSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 4: Receive FEAC FIFO Overflow Interrupt Enable (RFFOIE). This bit enables an interrupt if the RFFOL bit in the FSRL register is set.
0 = interrupt disabled
1 = interrupt enabled

Figure 7-8. FEAC Status Bit Interrupt Signal Flow



Register Name: **TFEACA**
Register Description: **Transmit FEAC A**
Register Address: **64h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	TFCA5	TFCA4	TFCA3	TFCA2	TFCA1	TFCA0
Default	—	—	0	0	0	0	0	0

Bits 0 to 5: Transmit FEAC Codeword A Data (TFCA[5:0]). The FEAC codeword is of the form …0xxxxxx011111111… where the rightmost bit is transmitted first. TFCA[5:0] are the middle six bits of the second byte of the FEAC codeword (i.e., the six "x" bits). The transmit FEAC controller can generate two different codewords. These six bits specify what is to be transmitted for codeword A. TFCA0 is the LSB and is transmitted first; TFCA5 is the MSB and is transmitted last. The TFS[1:0] control bits determine if this codeword is to be transmitted. These bits should only be changed when the transmit FEAC controller is in the idle state (TFS[1:0] = 00).

Register Name: **TFEACB**
Register Description: **Transmit FEAC B**
Register Address: **65h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	TFCB5	TFCB4	TFCB3	TFCB2	TFCB1	TFCB0
Default	—	—	0	0	0	0	0	0

Bits 0 to 5: Transmit FEAC Codeword B Data (TFCB[5:0]). The FEAC codeword is of the form …0xxxxxx011111111… where the rightmost bit is transmitted first. TFCB[5:0] are the middle six bits of the second byte of the FEAC codeword (i.e., the six "x" bits). The transmit FEAC controller can generate two different codewords. These six bits specify what is to be transmitted for codeword B. TFCB0 is the LSB and is transmitted first; TFCB5 is the MSB and is transmitted last. The TFS[1:0] control bits determine if this codeword is to be transmitted. These bits should only be changed when the transmit FEAC controller is in the idle state (TFS[1:0] = 00).

Register Name: **RFEAC**
Register Description: **Receive FEAC**
Register Address: **66h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	RFF5	RFF4	RFF3	RFF2	RFF1	RFF0
Default	—	—	—	—	—	—	—	—

Bits 0 to 5: Receive FEAC FIFO Data (RFF[5:0]). Data from the receive FEAC FIFO can be read from these bits. The FEAC codeword is of the form …0xxxxxx011111111… where the rightmost bit is received first. These six bits are the debounced and integrated middle six bits of the second byte of the FEAC codeword (i.e., the six "x" bits). RFF0 is the LSB and is received first; RFF5 is the MSB and is received last.

8. OPERATION DETAILS

8.1 Reset

The DS314x devices must be reset by activating the $\overline{\text{JTRST}}$ and $\overline{\text{RST}}$ pins after the power supply has settled and the input clocks have stabilized to their normal operating conditions. The $\overline{\text{JTRST}}$ pin can be permanently wired low if desired. After reset, all read/write control register bits are reset to 0 except for RDATH and TUA1, which are set to 1. The reset states of the device pins are as follows:

- E3 mode is enabled.
- The LIU interface is in dual-rail (POS/NEG) mode with HDB3 encoding and decoding enabled.
- TPOS and TNEG transmit an unframed all-ones signal (E3 AIS) on the transmit LIU interface.
- RDAT is forced to a logic 1 level to present an unframed all-ones signal (E3 AIS) on the receive system interface.
- TCLK is a noninverted, delayed version of TICLK.
- ROCLK is a noninverted, delayed version or RCLK.
- TSOF is an active-high input pin.
- RSOF, RLOS, and ROOF are active high.
- TDEN/TGCLK is in the TDEN (data enable) mode and is active high.
- RDEN/RGCLK is in the RDEN (data enable) mode and is active high.
- JTDO is tri-stated.

8.2 DS3 and E3 Mode Configuration

In all modes, the TUA1 bit in the MC1 register and RDATH bit in the MC4 register must be cleared. These bits are set to 1 at reset to generate an unframed all-ones (E3 AIS) signal on both the transmit LIU interface (TPOS/TNEG) and the receive system interface (RDAT).

E3 Mode

Default framer operation after reset is E3 mode. To begin operation in E3 mode after reset, clear the TUA1 bit in the MC1 register and clear the RDATH bit in the MC4 register. A 34.368MHz clock must be applied to the TICLK pin.

DS3 M23 Mode

To change framer operation after reset to DS3 M23 mode, set the DS3M bit to 1 in the T3E3CR1 register, clear the TUA1 bit in the MC1 register, and clear the RDATH bit in the MC4 register. A 44.736MHz clock must be applied to the TICLK pin.

DS3 C-Bit Parity Mode

To change framer operation after reset to DS3 C-Bit Parity mode, set the DS3M and CBEN bits to 1 in the T3E3CR1 register, clear the TUA1 bit in the MC1 register, and clear the RDATH bit in the MC4 register. A 44.736MHz clock must be applied to the TICLK pin.

8.3 LIU and System Interface Configuration

LIU Interface

After reset the default LIU interface format is dual-rail (POS/NEG) with B3ZS/HDB3 encoding and decoding enabled. To change framer operation after reset to binary (NRZ) format with B3ZS/HDB3 encoding and decoding disabled (disabled in the framer but should be enabled in the LIU), set the BIN bit to 1 in the MC1 register.

System Interface

After reset the TDEN/TGCLK and RDEN/RGCLK pins default to data enable behavior (TDEN, RDEN) and the TSOF pin defaults to being an input. If gapped clock behavior is desired, set the TDENMS bit tin the MC3 register and/or the RDENMS bit in the MC4 register. To configure TSOF as an output pin, set the TSOFC bit to 1 in the MC3 register.

8.4 Loopback Modes

The loopback modes are selected by setting the LLB, DLB, and/or PLB bits in the MC2 register. See Figure 1-1 for a visual description of these loopbacks. At reset, none of the loopback modes are activated. PLB and DLB may not be active at the same time. If LLB and PLB are both active at the same time, then TPOS/TNRZ, TNEG, and TCLK are sourced from RPOS/RNRZ, RNEG/RLCV, and RCLK while the internal workings of the framer are in PLB mode.

The line loopback (LLB) mode is used to send the received signal back toward the network. TAIS and TUA1 are not available during line loopback, but the TPOS/TRNZ and TNEG pins can be forced high and low using the TPOSH, TPOSI, TNEGH, and TNEGI bits in the MC5 register.

The diagnostic loopback (DLB) mode is used to send the transmitted signal back toward the system through the receive framer. When the framer is in diagnostic loopback, it can simultaneously transmit AIS to the far end if the TAIS bit is set in the T3E3CR1 register. The framer supports simultaneous line loopback and diagnostic loopback.

The payload loopback (PLB) mode is used to send the received payload back toward the network with new overhead inserted. When the framer is in payload loopback, the internal transmit clock is connected to the internal receive clock, internal transmit data is sourced from internal receive data, and TICLK and TDAT are ignored. The TDEN and TSOF signals are aligned with the RDEN and RSOF signals, and TOH and TOHEN are still enabled. The TSOF, TDEN, TOH, and TOHEN signals are timed relative to ROCLK rather than TICLK.

8.5 Transmit Overhead Insertion

The transmit signal can be overwritten at any bit location using the TOH and TOHEN signals. The TSOF signal marks the start of the transmit frame and is used to determine which bits to overwrite. To overwrite a specific bit in the DS3 or E3 frame, count the required number of TICLK cycles after the TSOF frame pulse. When the proper TICLK cycle is reached, assert the TOHEN pin to replace normal transmit data (overhead or payload) with the value on the TOH pin. One application for the TOH and TOHEN pins is to use some of the unused C bits in DS3 C-Bit Parity mode for a proprietary communications channel.

During payload loopback, the transmit side is timed from ROCLK rather than TICLK. If the system needs to support transmit overhead insertion (TOH) during payload loopback (PLB), then TOH and TOHEN must also be timed with respect to ROCLK. One way to access ROCLK is to set the TCCLK bit in the MC2 register to convert the TDEN/TGCLK output pin into a constant clock, which is based on ROCLK during payload loopback. TOH and TOHEN can then be timed with respect to the constant clock on the TDEN/TGCLK pin.

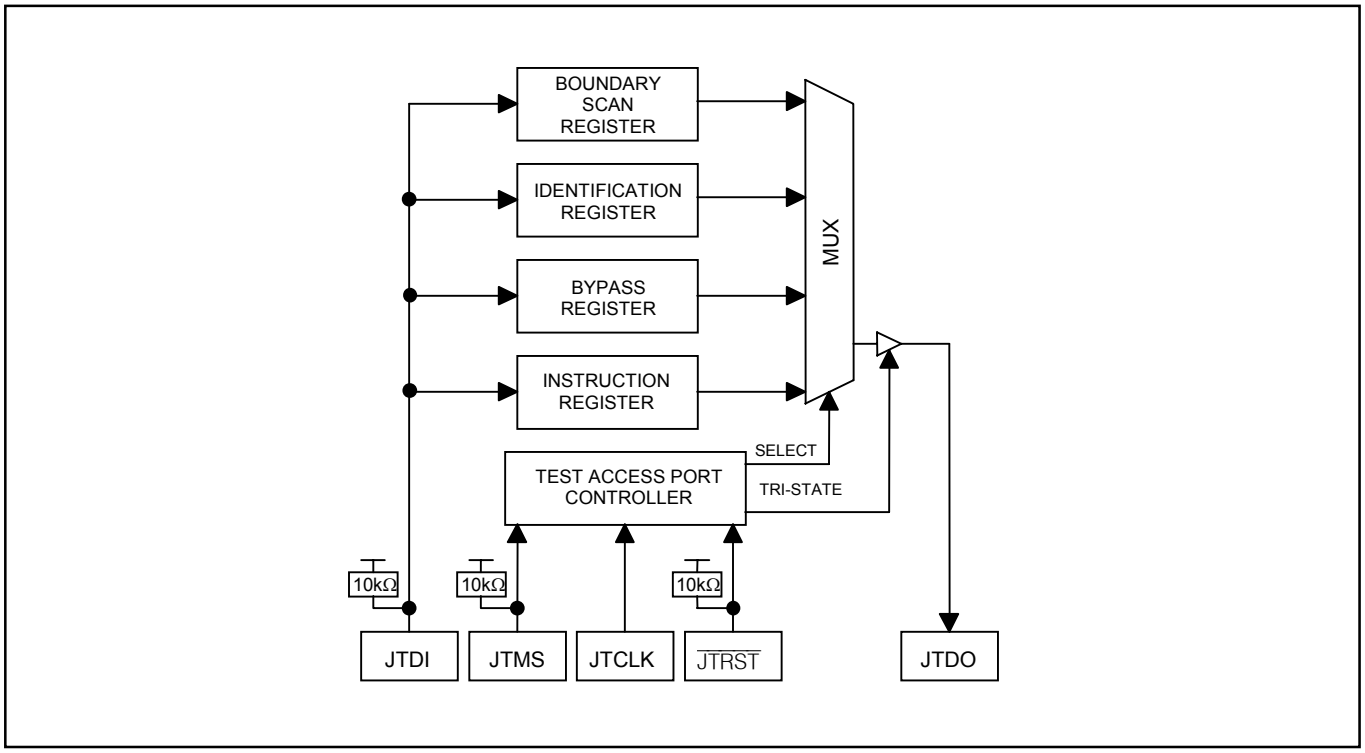
9. JTAG INFORMATION

The DS3141, DS3142, and DS3143, and DS3144 support the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. See the JTAG block diagram in Figure 9-1. The device contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port (TAP) and Boundary Scan Architecture:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

The Test Access Port has the necessary interface pins, namely JTCLK, JTDI, JTDO, and JTMS, and the optional $\overline{\text{JTRST}}$ input. Details on these pins can be found in Section 5.6. Refer to IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994 for details about the Boundary Scan Architecture and the Test Access Port.

Figure 9-1. JTAG Block Diagram



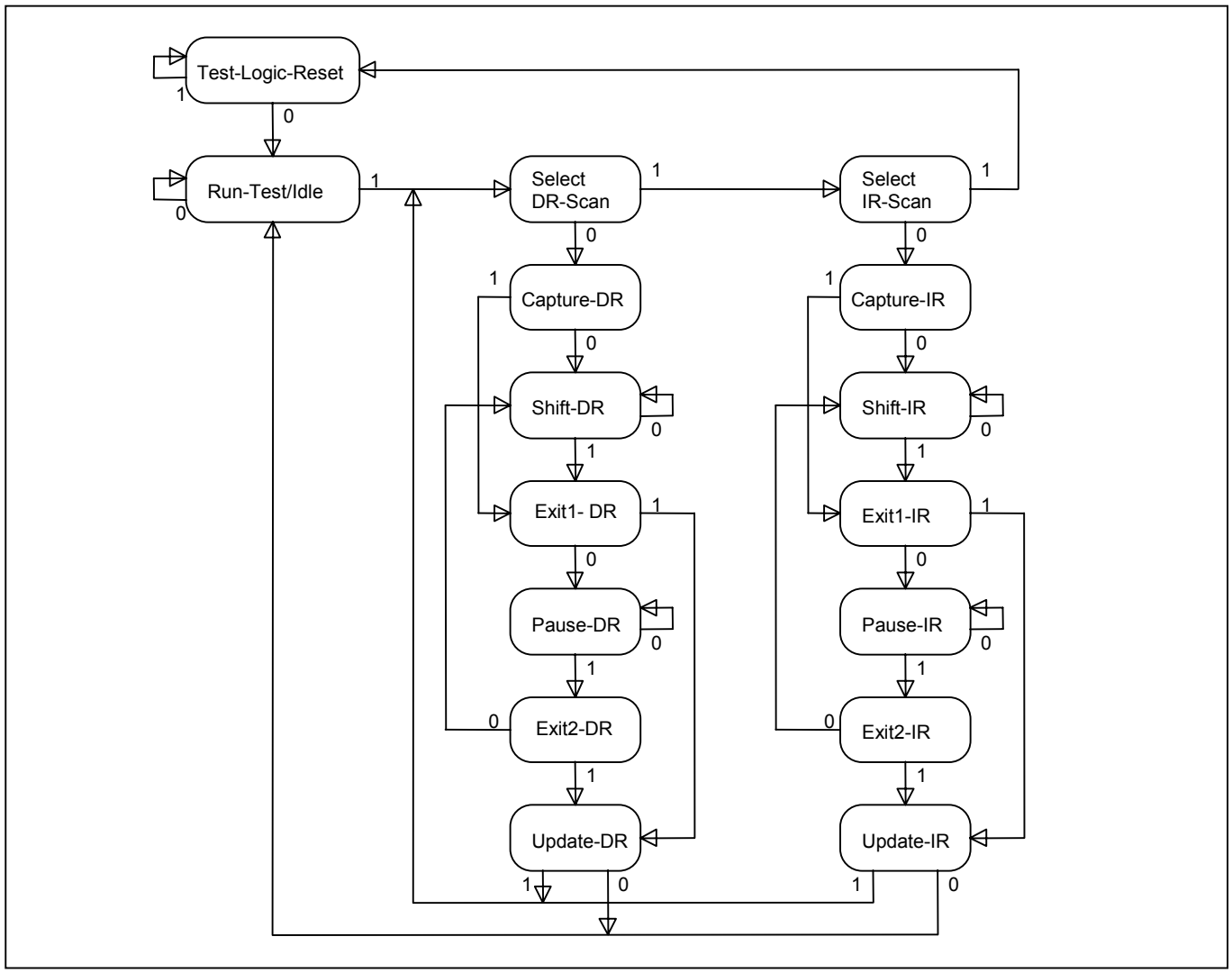
9.1 JTAG TAP Controller State Machine

This section covers the operation of the TAP controller state machine. See Figure 9-2 for details on each of the states described below. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK.

Test-Logic-Reset. When $\overline{\text{JTRST}}$ is changed from low to high, the TAP controller starts in the Test-Logic-Reset state, and the instruction register is loaded with the IDCODE instruction. All system logic and I/O pads on the device operate normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The instruction register and test register remain idle.

Figure 9-2. JTAG TAP Controller State Machine



Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data can be parallel loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

Shift-DR. The test data register selected by the current instruction is connected between JTDI and JTDO and shifts data one stage toward its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and all test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state while moving data one stage through the instruction shift register.

Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR. Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

9.2 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 9-A shows the instructions supported by the device and their respective operational binary codes.

Table 9-A. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD. SAMPLE/PRELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE/PRELOAD also allows the device to shift data into the boundary scan register through JTDI using the Shift-DR state.

EXTEST. EXTEST allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled by the Update-IR state, the parallel outputs of all digital output pins are driven. The boundary scan register is connected between JTDI and JTDO. The Capture-DR samples all digital inputs into the boundary scan register.

BYPASS. When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the 1-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

IDCODE. When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code is loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially through JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output.

HIGHZ. All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

CLAMP. All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

Table 9-B. JTAG ID Code

DEVICE	REVISION	DEVICE CODE	MANUFACTURER'S CODE	REQUIRED
DS3141	Consult factory	0000000000010001	00010100001	1
DS3142	Consult factory	0000000000010010	00010100001	1
DS3143	Consult factory	0000000000010011	00010100001	1
DS3144	Consult factory	0000000000010100	00010100001	1

9.3 JTAG Scan Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the design and is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register

The bypass register is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions that provides a short path between JTDI and JTDO.

Identification Register

The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device ID code always has a 1 in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes, followed by 16 bits for the device and 4 bits for the version.

Boundary Scan Register

The boundary scan register contains a shift register path and a latched parallel output for all control cells and digital I/O cells.

10. DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Input, Bidirectional or Open Drain Output Lead with Respect to V_{SS}	-0.3V to +5.5V
Supply Voltage Range (V_{DD}) with Respect to V_{SS}	-0.3V to +3.63V
Ambient Operating Temperature Range	-40°C to +85°C
Junction Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature Range	See IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

Note: *The typical values listed in the following tables are not production tested.*

Table 10-A. Recommended DC Operating Conditions

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}		2.4		5.5	V
Logic 0	V_{IL}		-0.3		+0.8	V
Supply	V_{DD}		3.135		3.465	V

Table 10-B. DC Electrical Characteristics

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (V_{DD} = 3.465V) (Notes 1, 2)	I_{DD}	DS3141		80	90	mA
		DS3142		155	170	
		DS3143		225	250	
		DS3144		290	320	
Power-Down Current (All DISABLE Bits Set)	I_{DDD}	DS3144 (Notes 1, 2)			100	mA
Lead Capacitance	C_{IO}			7.0		pF
Input Leakage	I_{IL}		-10		+10	µA
Input Leakage (Inputs Pins with Internal Pullup Resistors)	I_{ILP}		-300		+10	µA
Output Leakage (when High-Z)	I_{LO}		-10		+10	µA
Output Voltage (I_{OH} = -4.0mA)	V_{OH}		2.4			V
Output Voltage (I_{OL} = +4.0mA)	V_{OL}				0.4	V

Note 1: DS3 mode (DS3M = 1); TICLK, RCLK, and SCLK toggling at 44.736MHz.
Note 2: All outputs loaded with rated capacitance; all inputs at V_{DD} or V_{SS}; inputs with pullups connected to V_{DD}.

11. AC TIMING CHARACTERISTICS

All AC timing characteristics are specified with a 50pF capacitive load on the D[7:0] and $\overline{INT}$ pins, and a 25pF capacitive load on all other output pins, $V_{IH} = V_{DD}$ and $V_{IL} = V_{SS}$. The voltage threshold for all timing measurements is $V_{DD}/2$.

11.1 System Interface Timing

Table 11-A. Data Path Timing

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (Figure 11-1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Clock Period	t1	(Note 1)	29.0	29.1		ns
		(Note 2)	22.0	22.4		
		(Note 3)	19.0	19.3		
CLK Clock Duty Cycle	t2/t1		40	50	60	%
CLK in to DIN Setup Time	t3	(Note 4)	3.0			ns
CLK in to DIN Hold Time	t4	(Note 4)	1.0			ns
CLK in to DOUT Delay	t5	(Note 5)	2.0		12	ns
CLK out to DOUT Delay	t6	(Notes 6, 7)	2.0		7.0	ns
CLK in to CLK OUT Delay	t7	(Note 8)			10	ns
Asynchronous Input High, Low Time	t8, t9	(Note 9)	200			ns
Asynchronous Input Period	t10	(Note 9)	1000			ns

Note 1: E3 mode, nongapped 34.368MHz clock.
Note 2: DS3 mode, nongapped 44.736MHz clock.
Note 3: DS3 mode, gapped 51.84MHz clock.
Note 4: TICLK input to TDAT, TOH, TOHEN, and TSOF inputs; RCLK input to RPOS and RNEG inputs.
Note 5: TICLK input to TDEN (data-enable mode) and TSOF outputs.
Note 6: ROCLK output to RDAT, RDEN (data-enable mode) and RSOF outputs; TCLK output to TPOS and TNEG outputs.
Note 7: RGCLK (gapped clock mode) output to RDAT and RSOF outputs; TDEN/TGCLK (gapped or constant clock mode) output to TSOF output.
Note 8: TICLK input to TDEN/TGCLK (gapped clock or constant clock mode) outputs; RCLK input to ROCLK output.
Note 9: TMEI, RECU, and $\overline{RST}$ inputs.

Table 11-B. Line Loopback Timing

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (Figure 11-2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Skew on RPOS to TPOS Path with Respect to RCLK to TCLK Path	t2 - t1		0		3.0	ns
Skew on RNEG to TNEG path with Respect to RCLK to TCLK Path	t2 - t1		0		3.0	ns

Figure 11-1. Data Path Timing Diagram

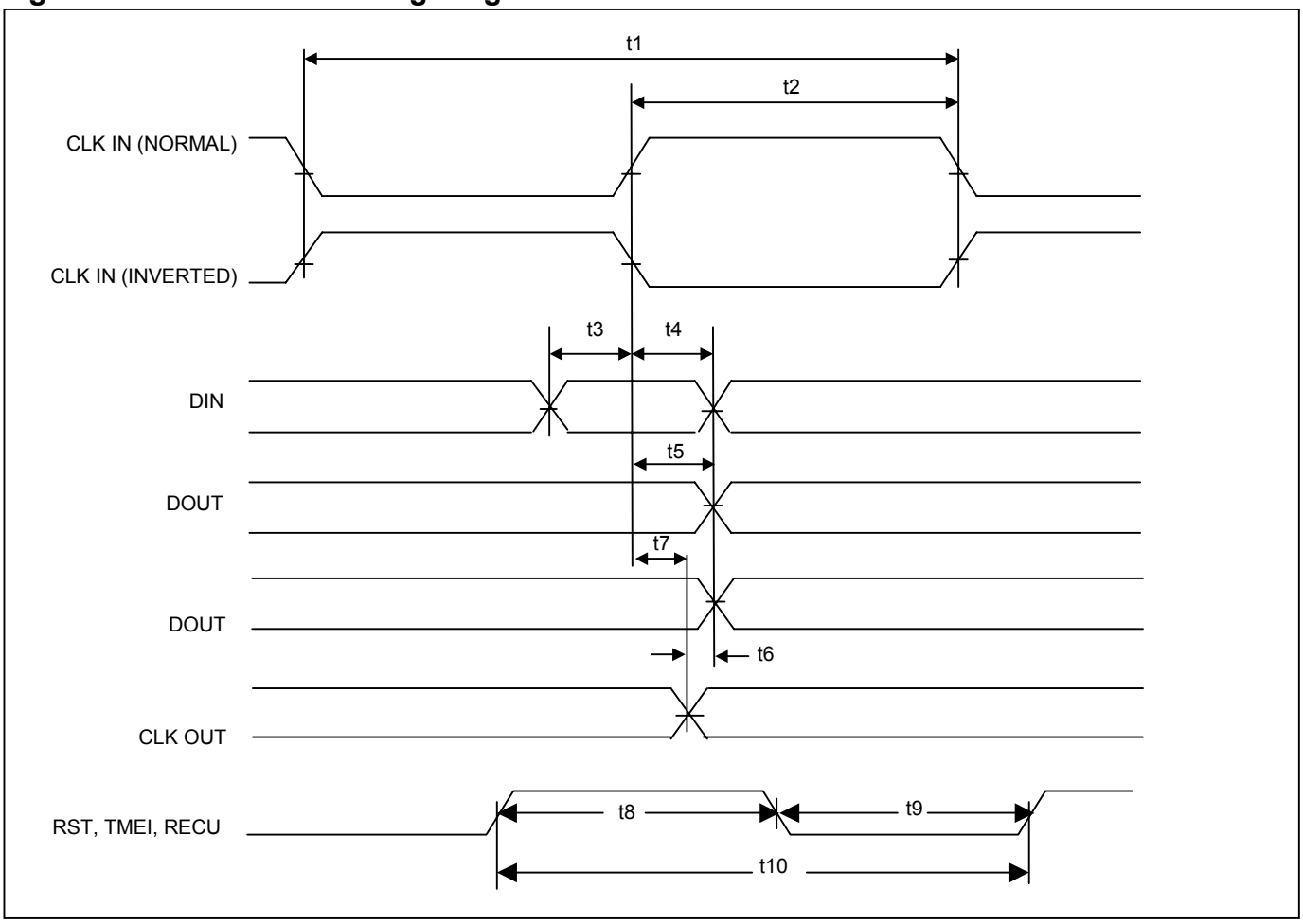
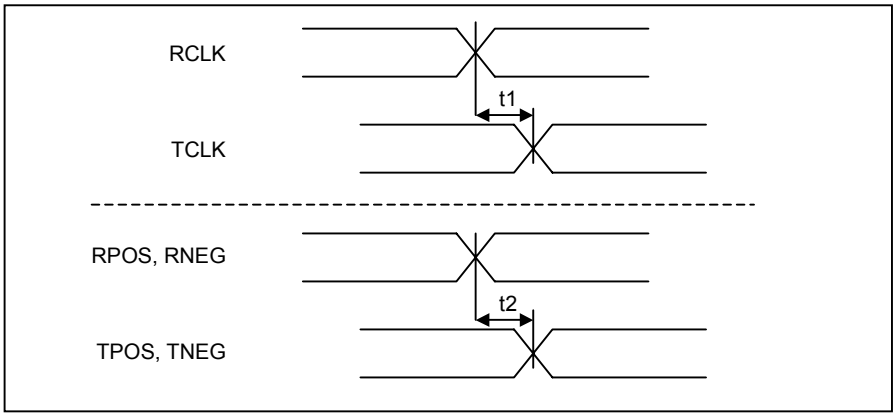


Figure 11-2. Line Loopback Timing Diagram



11.2 Microprocessor Interface Timing

Table 11-C. Microprocessor Interface Timing

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (Figure 11-3, Figure 11-4, and Figure 11-5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for A[9:0] Valid to $\overline{CS}$ Active	t1		0			ns
Setup Time for $\overline{CS}$ Active to $\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Active	t2		0			ns
Delay Time from $\overline{RD}$ or $\overline{DS}$ Active to D[7:0] Valid	t3				65	ns
Hold Time from $\overline{RD}$ or $\overline{WR}$ or $\overline{DS}$ Inactive to $\overline{CS}$ Inactive	t4		0			ns
Hold Time from $\overline{CS}$ or $\overline{RD}$ or $\overline{DS}$ Inactive to D[7:0] Tri-State	t5		5.0		20	ns
Wait Time from $\overline{WR}$ or $\overline{DS}$ Active to Latch D[7:0]	t6		65			ns
D[7:0] Setup Time to $\overline{WR}$ or $\overline{DS}$ Inactive	t7		10			ns
D[7:0] Hold Time from $\overline{WR}$ or $\overline{DS}$ Inactive	t8		2.0			ns
A[9:0] Hold from $\overline{WR}$ or $\overline{RD}$ or $\overline{DS}$ Inactive	t9		5.0			ns
$\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Inactive Time	t10		75			ns
Muxed Address Valid to ALE Falling	t11	(Note 10)	10			ns
Muxed Address Hold Time	t12	(Note 10)	10			ns
ALE Pulse Width	t13	(Note 10)	30			ns
Setup Time for ALE High or Muxed Address Valid to $\overline{CS}$ Active	t14	(Note 10)	0			ns
SCLK Period	t15		19		31	ns
SCLK High and Low Time	t16		7.0			ns
SCLK Duty Cycle (High/Low)	t16/t15		40		60	%

Note 10: In nonmultiplexed bus applications (Figure 11-4), ALE should be connected high. In multiplexed bus applications (Figure 11-5), A[7:0] are normally connected to D[7:0] externally, and the falling edge of ALE latches the address.

Note 11: Whenever $\overline{CS}$ = 0 and $\overline{RD}$ = 0 in Intel mode or $\overline{CS}$ = 0 and R/$\overline{WR}$ = 1 and $\overline{DS}$ = 0 in Motorola mode, the bidirectional data bus D[7:0] is driven as an output.

Figure 11-3. SCLK Clock Timing

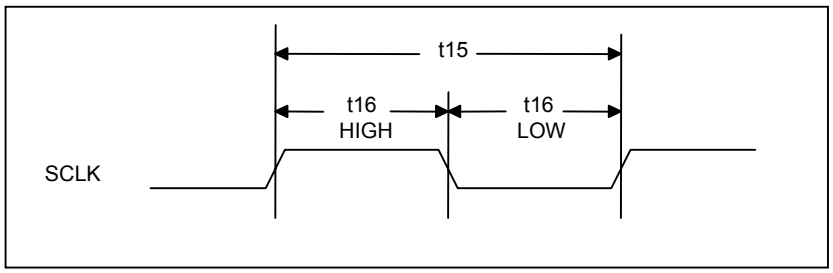


Figure 11-4. Microprocessor Interface Timing Diagram (Nonmultiplexed)

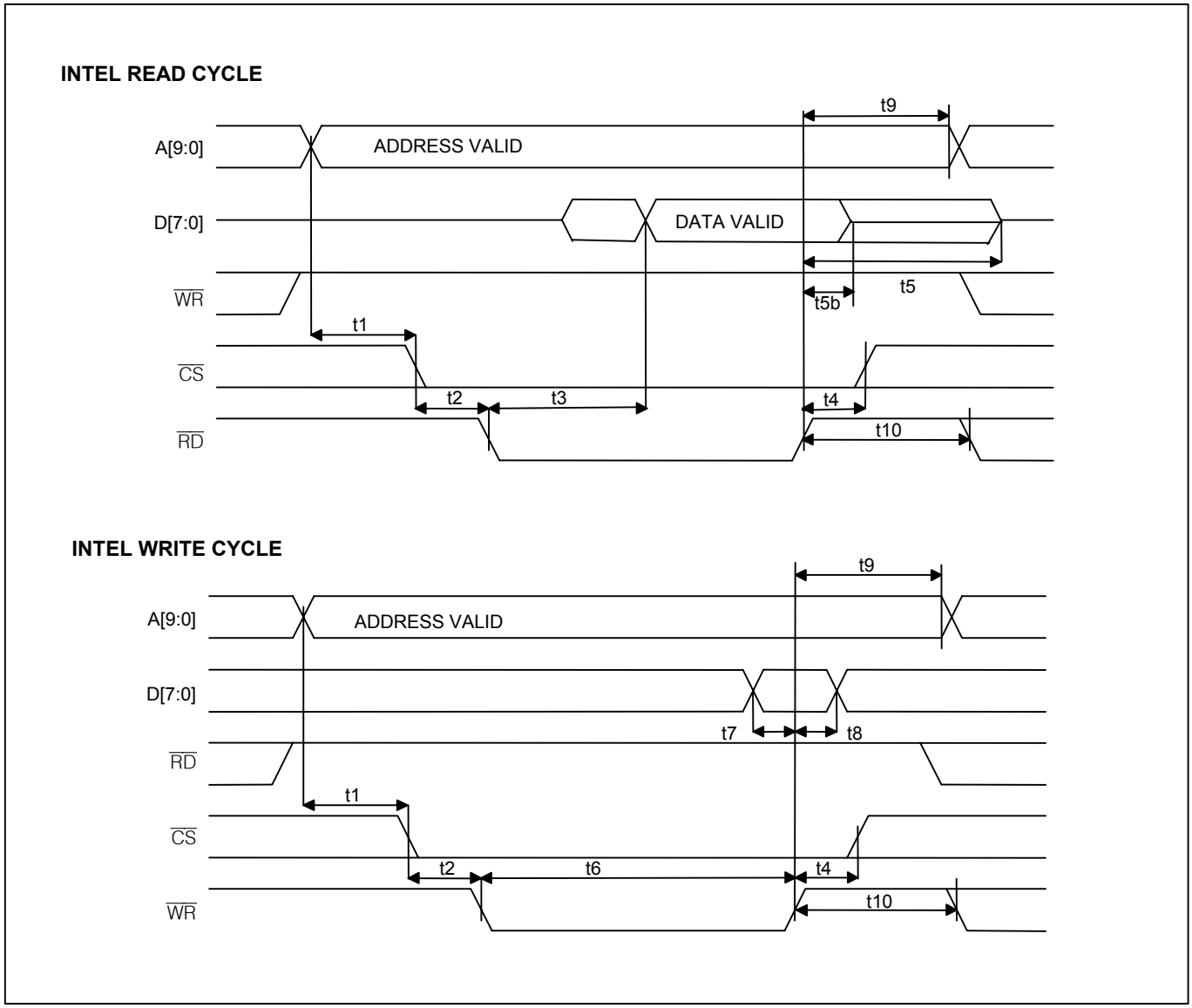


Figure 11-4. Microprocessor Interface Timing Diagram (Nonmultiplexed) (continued)

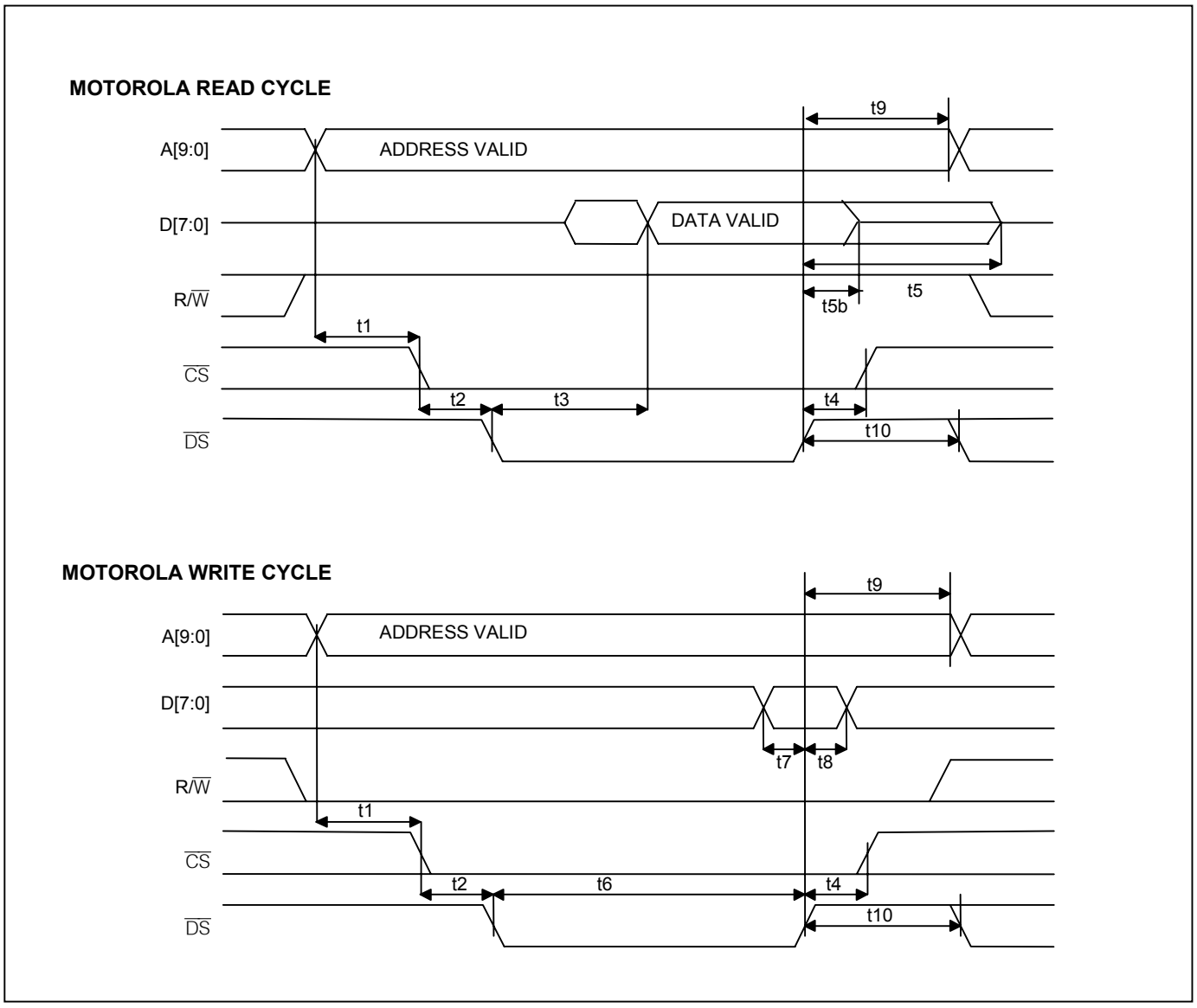
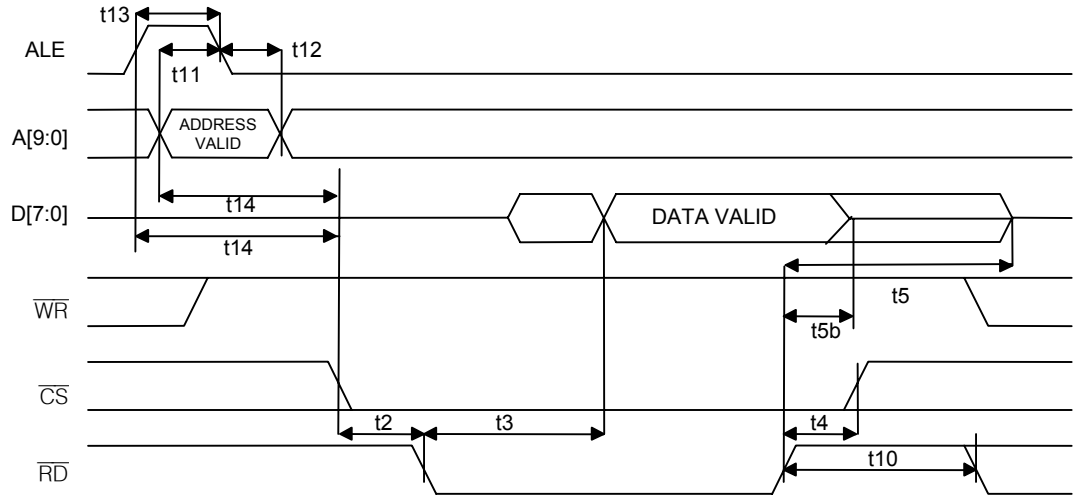


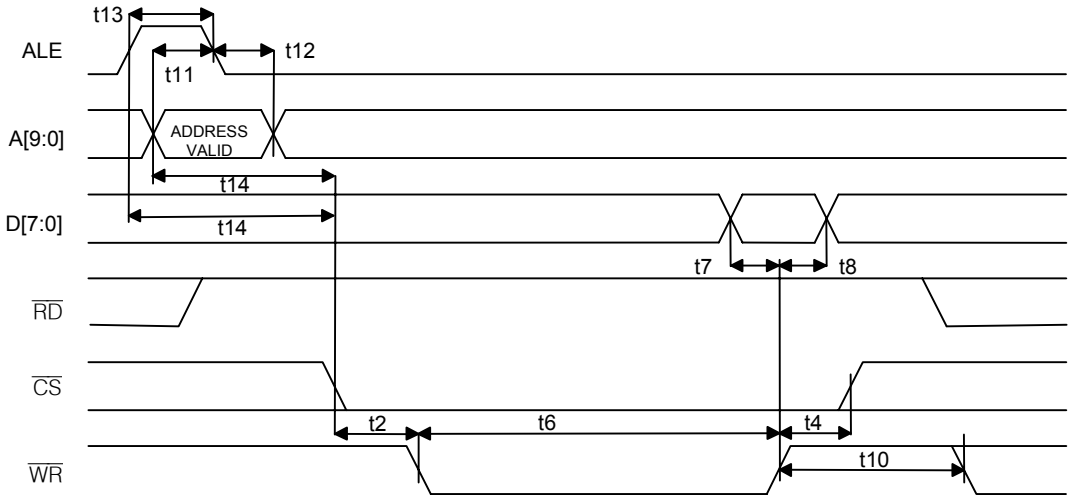
Figure 11-5. Microprocessor Interface Timing Diagram (Multiplexed)

INTEL READ CYCLE



NOTE: t14 STARTS ON THE OCCURRENCE OF EITHER THE RISING EDGE OF ALE OR A VALID ADDRESS, WHICHEVER OCCURS LAST.

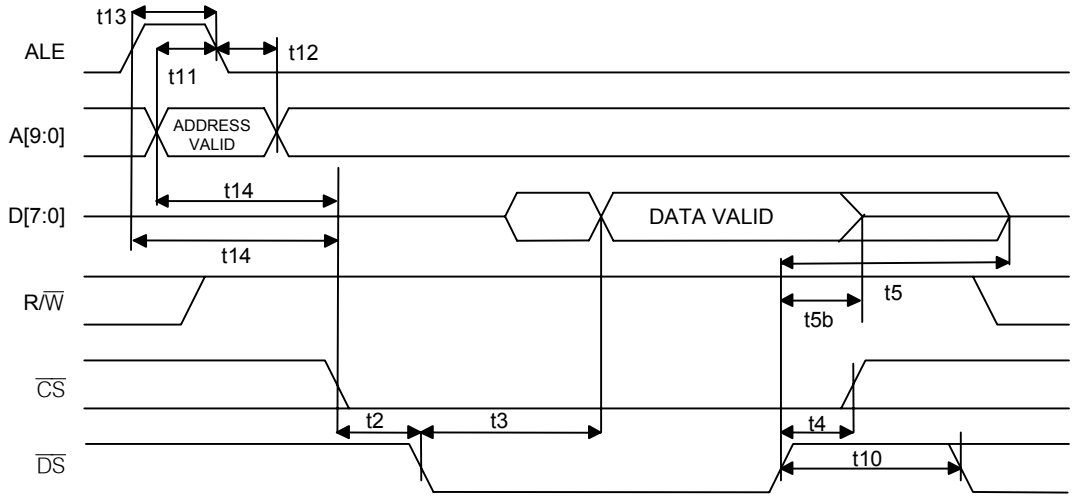
INTEL WRITE CYCLE



NOTE: t14 STARTS ON THE OCCURRENCE OF EITHER THE RISING EDGE OF ALE OR A VALID ADDRESS, WHICHEVER OCCURS LAST.

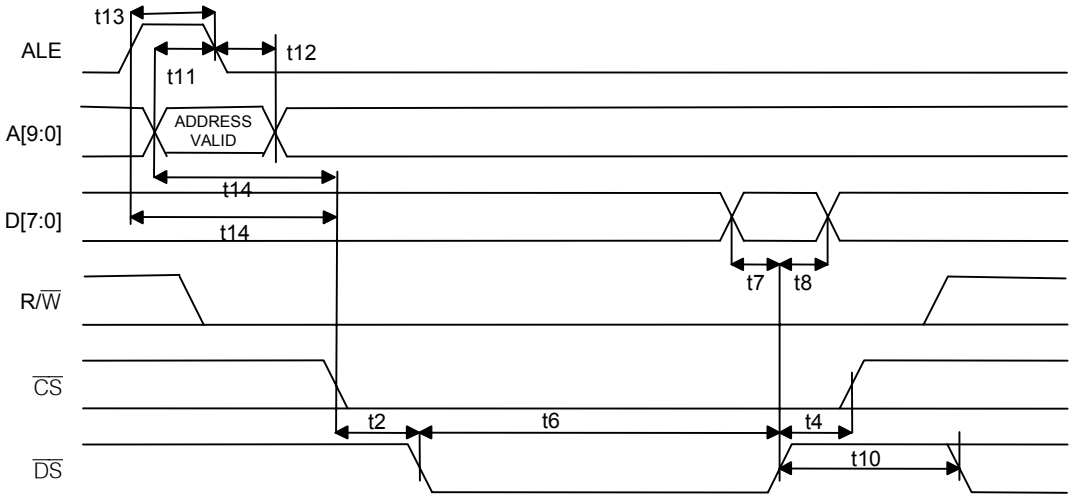
Figure 11-5. Microprocessor Interface Timing Diagram (Multiplexed) (continued)

MOTOROLA READ CYCLE



NOTE: t14 STARTS ON THE OCCURRENCE OF EITHER THE RISING EDGE OF ALE OR A VALID ADDRESS, WHICHEVER OCCURS LAST.

MOTOROLA WRITE CYCLE



NOTE: t14 STARTS ON THE OCCURRENCE OF EITHER THE RISING EDGE OF ALE OR A VALID ADDRESS, WHICHEVER OCCURS LAST.

11.3 JTAG Interface Timing

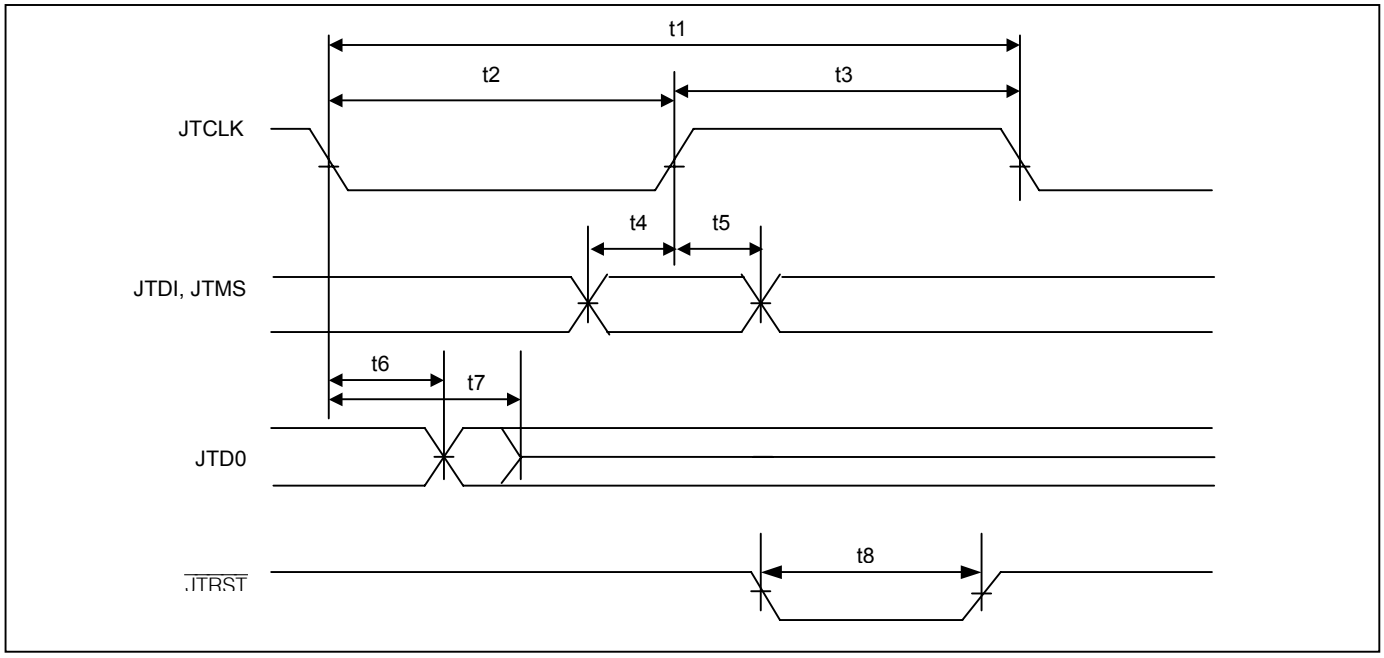
Table 11-D. JTAG Interface Timing

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (Figure 11-6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1			1000		ns
JTCLK Clock High/Low Time	t2/t3	(Note 12)	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4		50			ns
JTCLK to JTDI, JTMS Hold Time	t5		50			ns
JTCLK to JTDO Delay	t6		2		50	ns
JTCLK to JTDO High-Z Delay	t7		2		50	ns
$\overline{\text{JTRST}}$ Width Low Time	t8		100			ns

Note 12: Clock can be stopped high or low.

Figure 11-6. JTAG Interface Timing Diagram



12. PIN ASSIGNMENTS

Table 12-A lists pin assignments sorted by signal name. The DS3141 has only framer 1. The DS3142 has only framers 1 and 2. The DS3143 has only framers 1, 2, and 3. DS3144 has four framers. Figure 12-1, Figure 12-2, and Figure 12-3 show the pinouts for the three devices.

Table 12-A. Pin Assignments (Sorted by Signal Name)

NAME	PIN			
	FRAMER 1	FRAMER 2	FRAMER 3	FRAMER 4
A0	E3			
A1	G3			
A2	J3			
A3	K5			
A4	K7			
A5	K9			
A6	H10			
A7	F10			
A8	E10			
A9	D10			
ALE	C7			
$\overline{CS}$	C6			
D0	D3			
D1	F3			
D2	H3			
D3	K4			
D4	K6			
D5	K8			
D6	J10			
D7	G10			
$\overline{HIZ}$	J8			
JTCLK	E4			
JTDI	H4			
JTDO	J4			
JTMS	D5			
$\overline{JTRST}$	D4			
RCLK	C1	K12	A10	M3
$\overline{RD}$	C4			
RDAT	D1	J12	A9	M4
RDEN	D2	J11	B9	L4
RECU	J9			
RLOS	A2	M11	B12	L1
RNEG	A1	M12	A12	M1
ROCLK	E1	H12	A8	M5
ROOF	B2	L11	B11	L2
RPOS	B1	L12	A11	M2
RSOF	C2	K11	B10	L3
$\overline{RST}$	D8			
SCLK	D9			
TCLK	A5	M8	E12	H1
TDAT	A6	M7	F12	G1
TDEN	B6	L7	F11	G2
$\overline{TEST}$	J5			
TICLK	A7	M6	G12	F1
TMEI	H9			
TNEG	A4	M9	D12	J1
TOH	B7	L6	G11	F2
TOHEN	B8	L5	H11	E2
TPOS	B4	L9	D11	J2
TSOF	B5	L8	E11	H2
V_{DD}	D6, E5, E6, F4–F6, G7–G9, H7, H8, J7			
V_{SS}	D7, E7, E8, F7–F9, G4–G6, H5, H6, J6			
$\overline{WR}$	C5			

Figure 12-1. DS3141 Pin Configuration

A1 RNEG1	A2 RLOS1	A3 N.C.	A4 TNEG1	A5 TCLK1	A6 TDAT1	A7 TICLK1	A8 N.C.	A9 N.C.	A10 N.C.	A11 N.C.	A12 N.C.
B1 RPOS1	B2 ROOF1	B3 N.C.	B4 TPOS1	B5 TSOF1	B6 TDEN1	B7 TOH1	B8 TOHEN1	B9 N.C.	B10 N.C.	B11 N.C.	B12 N.C.
C1 RCLK1	C2 RSOF1	C3 N.C.	C4 $\overline{RD}$	C5 $\overline{WR}$	C6 $\overline{CS}$	C7 ALE	C8 MOT	C9 $\overline{NT}$	C10 N.C.	C11 N.C.	C12 N.C.
D1 RDAT1	D2 RDEN1	D3 D0	D4 $\overline{JTRST}$	D5 JTMS	D6 V_{DD}	D7 V_{SS}	D8 $\overline{RST}$	D9 SCLK	D10 N.C.	D11 N.C.	D12 N.C.
E1 ROCLK1	E2 N.C.	E3 A0	E4 JTCLK	E5 V_{DD}	E6 V_{DD}	E7 V_{SS}	E8 V_{SS}	E9 N.C.	E10 N.C.	E11 N.C.	E12 N.C.
F1 N.C.	F2 N.C.	F3 D1	F4 V_{DD}	F5 V_{DD}	F6 VDD	F7 V_{SS}	F8 V_{SS}	F9 V_{SS}	F10 A7	F11 N.C.	F12 N.C.
G1 N.C.	G2 N.C.	G3 A1	G4 V_{SS}	G5 V_{SS}	G6 V_{SS}	G7 V_{DD}	G8 V_{DD}	G9 V_{DD}	G10 D7	G11 N.C.	G12 N.C.
H1 N.C.	H2 N.C.	H3 D2	H4 JTDI	H5 V_{SS}	H6 V_{SS}	H7 V_{DD}	H8 V_{DD}	H9 TMEI	H10 A6	H11 N.C.	H12 N.C.
J1 N.C.	J2 N.C.	J3 A2	J4 JTDO	J5 $\overline{TEST}$	J6 V_{SS}	J7 V_{DD}	J8 $\overline{HIZ}$	J9 RECU	J10 D6	J11 N.C.	J12 N.C.
K1 N.C.	K2 N.C.	K3 N.C.	K4 D3	K5 A3	K6 D4	K7 A4	K8 D5	K9 A5	K10 N.C.	K11 N.C.	K12 N.C.
L1 N.C.	L2 N.C.	L3 N.C.	L4 N.C.	L5 N.C.	L6 N.C.	L7 N.C.	L8 N.C.	L9 N.C.	L10 N.C.	L11 N.C.	L12 N.C.
M1 N.C.	M2 N.C.	M3 N.C.	M4 N.C.	M5 N.C.	M6 N.C.	M7 N.C.	M8 N.C.	M9 N.C.	M10 N.C.	M11 N.C.	M12 N.C.

- Framer Pins
- Microprocessor Interface Pins
- JTAG and Debug Pins
- V_{DD}
- V_{SS}

Figure 12-2. DS3142 Pin Configuration

A1 RNEG1	A2 RLOS1	A3 N.C.	A4 TNEG1	A5 TCLK1	A6 TDAT1	A7 TICLK1	A8 N.C.	A9 N.C.	A10 N.C.	A11 N.C.	A12 N.C.
B1 RPOS1	B2 ROOF1	B3 N.C.	B4 TPOS1	B5 TSOF1	B6 TDEN1	B7 TOH1	B8 TOHEN1	B9 N.C.	B10 N.C.	B11 N.C.	B12 N.C.
C1 RCLK1	C2 RSOF1	C3 N.C.	C4 $\overline{RD}$	C5 $\overline{WR}$	C6 $\overline{CS}$	C7 ALE	C8 MOT	C9 $\overline{INT}$	C10 N.C.	C11 N.C.	C12 N.C.
D1 RDAT1	D2 RDEN1	D3 D0	D4 $\overline{JTRST}$	D5 JTMS	D6 V_{DD}	D7 V_{SS}	D8 $\overline{RST}$	D9 SCLK	D10 N.C.	D11 N.C.	D12 N.C.
E1 ROCLK1	E2 N.C.	E3 A0	E4 JTCLK	E5 V_{DD}	E6 V_{DD}	E7 V_{SS}	E8 V_{SS}	E9 N.C.	E10 A8	E11 N.C.	E12 N.C.
F1 N.C.	F2 N.C.	F3 D1	F4 V_{DD}	F5 V_{DD}	F6 V_{DD}	F7 V_{SS}	F8 V_{SS}	F9 V_{SS}	F10 A7	F11 N.C.	F12 N.C.
G1 N.C.	G2 N.C.	G3 A1	G4 V_{SS}	G5 V_{SS}	G6 V_{SS}	G7 V_{DD}	G8 V_{DD}	G9 V_{DD}	G10 D7	G11 N.C.	G12 N.C.
H1 N.C.	H2 N.C.	H3 D2	H4 JTDI	H5 V_{SS}	H6 VSS	H7 V_{DD}	H8 V_{DD}	H9 TMEI	H10 A6	H11 N.C.	H12 ROCLK2
J1 N.C.	J2 N.C.	J3 A2	J4 JTDO	J5 $\overline{TEST}$	J6 V_{SS}	J7 V_{DD}	J8 $\overline{HIZ}$	J9 RECU	J10 D6	J11 RDEN2	J12 RDAT2
K1 N.C.	K2 N.C.	K3 N.C.	K4 D3	K5 A3	K6 D4	K7 A4	K8 D5	K9 A5	K10 N.C.	K11 RSOF2	K12 RCLK2
L1 N.C.	L2 N.C.	L3 N.C.	L4 N.C.	L5 TOHEN2	L6 TOH2	L7 TDEN2	L8 TSOF2	L9 TPOS2	L10 N.C.	L11 ROOF2	L12 RPOS2
M1 N.C.	M2 N.C.	M3 N.C.	M4 N.C.	M5 N.C.	M6 TICLK2	M7 TDAT2	M8 TCLK2	M9 TNEG2	M10 N.C.	M11 RLOS2	M12 RNEG2

- Framer Pins
- Microprocessor Interface Pins
- JTAG and Debug Pins
- V_{DD}
- V_{SS}

Figure 12-3. DS3143 Pin Configuration

A1 RNEG1	A2 RLOS1	A3 N.C.	A4 TNEG1	A5 TCLK1	A6 TDAT1	A7 TICLK1	A8 ROCLK3	A9 RDAT3	A10 RCLK3	A11 RPOS3	A12 RNEG3
B1 RPOS1	B2 ROOF1	B3 N.C.	B4 TPOS1	B5 TSOF1	B6 TDEN1	B7 TOH1	B8 TOHEN1	B9 RDEN3	B10 RSOF3	B11 ROOF3	B12 RLOS3
C1 RCLK1	C2 RSOF1	C3 N.C.	C4 $\overline{RD}$	C5 $\overline{WR}$	C6 $\overline{CS}$	C7 ALE	C8 MOT	C9 $\overline{INT}$	C10 N.C.	C11 N.C.	C12 N.C.
D1 RDAT1	D2 RDEN1	D3 D0	D4 $\overline{JTRST}$	D5 JTMS	D6 V_{DD}	D7 V_{SS}	D8 $\overline{RST}$	D9 SCLK	D10 A9	D11 TPOS3	D12 TNEG3
E1 ROCLK1	E2 N.C.	E3 A0	E4 JTCLK	E5 V_{DD}	E6 V_{DD}	E7 V_{SS}	E8 V_{SS}	E9 N.C.	E10 A8	E11 TSOF3	E12 TCLK3
F1 N.C.	F2 N.C.	F3 D1	F4 V_{DD}	F5 V_{DD}	F6 V_{DD}	F7 V_{SS}	F8 V_{SS}	F9 V_{SS}	F10 A7	F11 TDEN3	F12 TDAT3
G1 N.C.	G2 N.C.	G3 A1	G4 V_{SS}	G5 V_{SS}	G6 V_{SS}	G7 V_{DD}	G8 V_{DD}	G9 V_{DD}	G10 D7	G11 TOH3	G12 TICLK3
H1 N.C.	H2 N.C.	H3 D2	H4 JTDI	H5 V_{SS}	H6 V_{SS}	H7 V_{DD}	H8 V_{DD}	H9 TMEI	H10 A6	H11 TOHEN3	H12 ROCLK2
J1 N.C.	J2 N.C.	J3 A2	J4 JTDO	J5 $\overline{TEST}$	J6 V_{SS}	J7 V_{DD}	J8 $\overline{HIZ}$	J9 RECU	J10 D6	J11 RDEN2	J12 RDAT2
K1 N.C.	K2 N.C.	K3 N.C.	K4 D3	K5 A3	K6 D4	K7 A4	K8 D5	K9 A5	K10 N.C.	K11 RSOF2	K12 RCLK2
L1 N.C.	L2 N.C.	L3 N.C.	L4 N.C.	L5 TOHEN2	L6 TOH2	L7 TDEN2	L8 TSOF2	L9 TPOS2	L10 N.C.	L11 ROOF2	L12 RPOS2
M1 N.C.	M2 N.C.	M3 N.C.	M4 N.C.	M5 N.C.	M6 TICLK2	M7 TDAT2	M8 TCLK2	M9 TNEG2	M10 N.C.	M11 RLOS2	M12 RNEG2

- Framer Pins
- Microprocessor Interface Pins
- JTAG and Debug Pins
- V_{DD}
- V_{SS}

Figure 12-4. DS3144 Pin Configuration

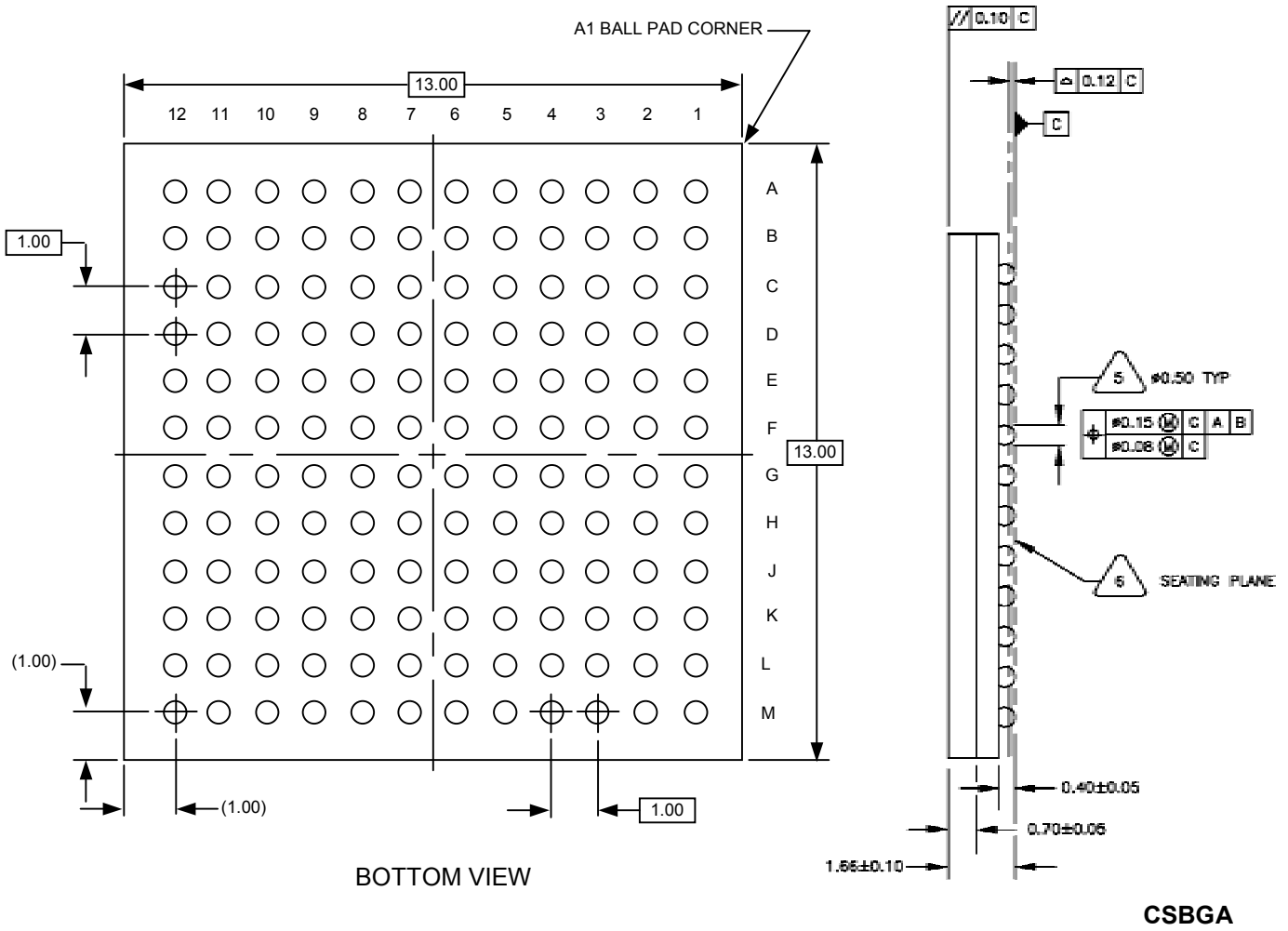
A1 RNEG1	A2 RLOS1	A3 N.C.	A4 TNEG1	A5 TCLK1	A6 TDAT1	A7 TICLK1	A8 ROCLK3	A9 RDAT3	A10 RCLK3	A11 RPOS3	A12 RNEG3
B1 RPOS1	B2 ROOF1	B3 N.C.	B4 TPOS1	B5 TSOF1	B6 TDEN1	B7 TOH1	B8 TOHEN1	B9 RDEN3	B10 RSOF3	B11 ROOF3	B12 RLOS3
C1 RCLK1	C2 RSOF1	C3 N.C.	C4 $\overline{RD}$	C5 $\overline{WR}$	C6 $\overline{CS}$	C7 ALE	C8 MOT	C9 $\overline{INT}$	C10 N.C.	C11 N.C.	C12 N.C.
D1 RDAT1	D2 RDEN1	D3 D0	D4 $\overline{JTRST}$	D5 JTMS	D6 V_{DD}	D7 V_{SS}	D8 $\overline{RST}$	D9 SCLK	D10 A9	D11 TPOS3	D12 TNEG3
E1 ROCLK1	E2 TOHEN4	E3 A0	E4 JTCLK	E5 V_{DD}	E6 V_{DD}	E7 V_{SS}	E8 V_{SS}	E9 N.C.	E10 A8	E11 TSOF3	E12 TCLK3
F1 TICLK4	F2 TOH4	F3 D1	F4 V_{DD}	F5 V_{DD}	F6 V_{DD}	F7 V_{SS}	F8 V_{SS}	F9 V_{SS}	F10 A7	F11 TDEN3	F12 TDAT3
G1 TDAT4	G2 TDEN4	G3 A1	G4 V_{SS}	G5 V_{SS}	G6 V_{SS}	G7 V_{DD}	G8 V_{DD}	G9 V_{DD}	G10 D7	G11 TOH3	G12 TICLK3
H1 TCLK4	H2 TSOF4	H3 D2	H4 JTDI	H5 V_{SS}	H6 V_{SS}	H7 V_{DD}	H8 V_{DD}	H9 TMEI	H10 A6	H11 TOHEN3	H12 ROCLK2
J1 TNEG4	J2 TPOS4	J3 A2	J4 JTDO	J5 $\overline{TEST}$	J6 V_{SS}	J7 V_{DD}	J8 $\overline{HIZ}$	J9 RECU	J10 D6	J11 RDEN2	J12 RDAT2
K1 N.C.	K2 N.C.	K3 N.C.	K4 D3	K5 A3	K6 D4	K7 A4	K8 D5	K9 A5	K10 N.C.	K11 RSOF2	K12 RCLK2
L1 RLOS4	L2 ROOF4	L3 RSOF4	L4 RDEN4	L5 TOHEN2	L6 TOH2	L7 TDEN2	L8 TSOF2	L9 TPOS2	L10 N.C.	L11 ROOF2	L12 RPOS2
M1 RNEG4	M2 RPOS4	M3 RCLK4	M4 RDAT4	M5 ROCLK4	M6 TICLK2	M7 TDAT2	M8 TCLK2	M9 TNEG2	M10 N.C.	M11 RLOS2	M12 RNEG2

- Framer Pins
- Microprocessor Interface Pins
- JTAG and Debug Pins
- V_{DD}
- V_{SS}

13. PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

Note: *All dimensions in millimeters.*



CSBGA

14. THERMAL INFORMATION

Table 14-A. Thermal Properties, Natural Convection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient Temperature		(Note 1)	-40.0		+85.0	°C
Junction Temperature			-40.0		+125	°C
Theta-JA (θ_{JA}), Still Air		(Note 2)		22.4		°C/W
Psi-JB				9.20		°C/W
Psi-JT				1.60		°C/W

Note 1: The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.
Note 2: Theta-JA (θ_{JA}) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

Table 14-B. Theta-JA (θ_{JA}) vs. Airflow

FORCED AIR (m/s)	THETA-JA (θ_{JA})
0	22.4°C/W
1	19.0°C/W
2.5	17.2°C/W

15. REVISION HISTORY

REVISION	DESCRIPTION
102102	DS3144 new product release.
012003	DS3141/DS3142/DS3143 new product releases.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600