



Single/Dual, Ultra-Fast, Low-Power Precision TTL Comparators

MAX912/MAX913

General Description

The MAX913 single and MAX912 dual, high-speed, low-power comparators have differential inputs and complementary TTL outputs. Fast propagation delay (10ns, typ), extremely low supply current, and a wide common-mode input range that includes the negative rail make the MAX912/MAX913 ideal for low-power, high-speed, single +5V (or ±5V) applications such as V/F converters or switching regulators.

The MAX912/MAX913 outputs remain stable through the linear region. This feature eliminates output instability common to high-speed comparators when driven with a slow-moving input signal.

The MAX912/MAX913 can be powered from a single +5V supply or a ±5V split supply. The MAX913 is an improved plug-in replacement for the LT1016. It provides significantly wider input voltage range and equivalent speed at a fraction of the power. The MAX912 dual comparator has equal performance to the MAX913 and includes independent latch controls.

Applications

- Zero-Crossing Detectors
- Ethernet Line Receivers
- Switching Regulators
- High-Speed Sampling Circuits
- High-Speed Triggers
- Extended Range V/F Converters
- Fast Pulse Width/Height Discriminators

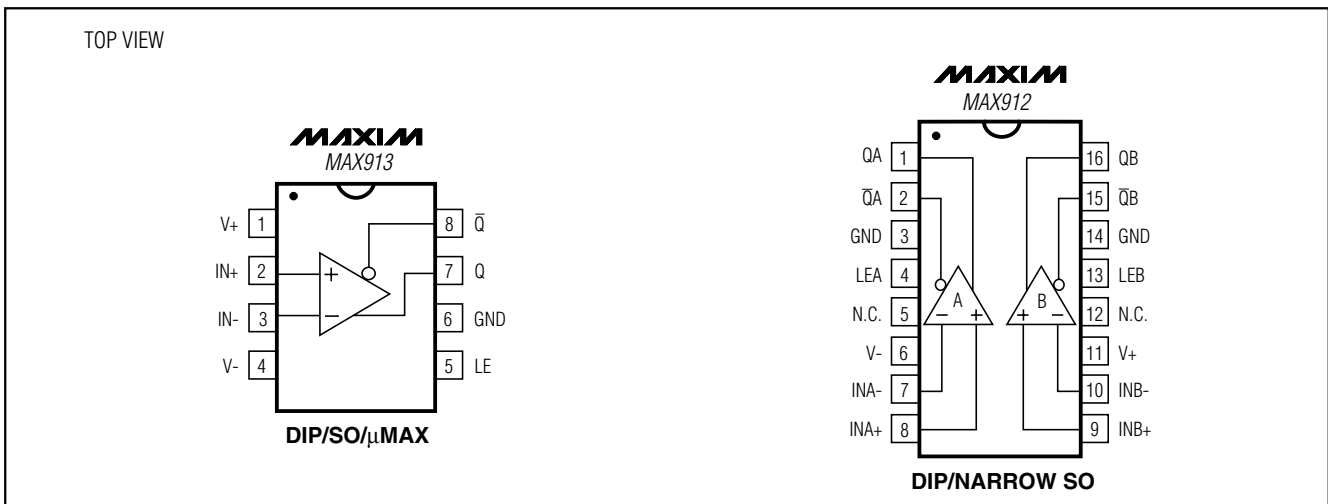
Features

- ◆ Ultra Fast (10ns)
- ◆ Single +5V or Dual ±5V Supply Operation
- ◆ Input Range Extends Below Negative Supply
- ◆ Low Power: 6mA (+5V) Per Comparator
- ◆ No Minimum Input Signal Slew-Rate Requirement
- ◆ No Power-Supply Current Spiking
- ◆ Stable in the Linear Region
- ◆ Inputs Can Exceed Either Supply
- ◆ Low Offset Voltage: 0.8mV
- ◆ Now Available in a Small μMAX Package

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------|----------------|----------------|
| MAX912CPE | 0°C to +70°C | 16 Plastic DIP |
| MAX912CSE | 0°C to +70°C | 16 Narrow SO |
| MAX912EPE | -40°C to +85°C | 16 Plastic DIP |
| MAX912ESE | -40°C to +85°C | 16 Narrow SO |
| MAX913CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX913CSA | 0°C to +70°C | 8 SO |
| MAX913EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX913ESA | -40°C to +85°C | 8 SO |
| MAX913EUA | -40°C to +85°C | 8 μMAX |

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|-------------------|---|-----------------|
| Positive Supply Voltage | +7V | 8-Pin SO (derate 5.88mW/°C above +70°C)..... | 471mW |
| Negative Supply Voltage | -7V | 8-Pin μ MAX (derate 4.5mW/°C above +70°C) | 362mW |
| V+ to V- | +13V | 16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) | 842mW |
| Differential Input Voltage | +15V | 16-Pin Narrow SO (derate 8.70mW/°C above +70°C) | 696mW |
| Input Voltage (Referred to V-) | -0.3V to +14V | Operating Temperature Ranges: | |
| Latch Pin Voltage | Equal to Supplies | MAX91_C_ | 0°C to +70°C |
| Continuous Output Current..... | ± 20 mA | MAX91_E_ | -40°C to +85°C |
| Continuous Power Dissipation (T _A = +70°C) | | Storage Temperature Range | -65°C to +150°C |
| 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... | 727mW | Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V+ = +5V, V- = -5V, V_Q = 1.4V, V_{LE} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|-------------------|--|---|------|------|------|------------|
| Input Offset Voltage (Note 2) | V _{OS} | R _S \leq 100 Ω | T _A = +25°C | 0.1 | 2 | 3 | mV |
| | | | T _A = T _{MIN} TO T _{MAX} | | | | |
| Offset Drift | TCV _{OS} | | | 2 | | | μ V/°C |
| Input Offset Current (Note 2) | I _{OS} | T _A = +25°C | | 0.3 | 0.5 | 1 | μ A |
| | | T _A = T _{MIN} TO T _{MAX} | | | | | |
| Input Bias Current | I _B | T _A = +25°C | | 2 | 5 | 8 | μ A |
| | | C, E temperature ranges | | | | | |
| Input Voltage Range | V _{CM} | C, E temperature ranges | | -5.2 | +3.5 | +3.5 | V |
| | | Single +5V | C, E temperature ranges | -0.2 | | | |
| Common-Mode Rejection Ratio | CMRR | -5.0V \leq V _{CM} \leq +3.5V | | 80 | 110 | | dB |
| Power-Supply Rejection Ratio | PSRR | Positive supply; 4.5V \leq V+ \leq 5.5V | | 60 | 85 | | dB |
| | | Negative supply; -2V \geq V- \geq -7V | | 80 | 100 | | |
| Small-Signal Voltage Gain | A _V | 1V \leq V _Q \leq 2V, T _A = +25°C | | 1500 | 3500 | | V/V |
| Output Voltage | V _{OH} | V+ \geq 4.5V | I _{OUT} = 1mA | 2.7 | 3.4 | 0.5 | V |
| | | | I _{OUT} = 10mA | 2.4 | 3.0 | | |
| | V _{OL} | I _{SINK} = 4mA | | 0.3 | | | |
| | | T _A = +25°C, I _{SINK} = 10mA | | 0.4 | | | |
| Positive Supply Current Per Comparator (Note 3) | I+ | C, E temperature ranges | | 6 | 10 | | mA |
| Negative Supply Current Per Comparator (Note 3) | I- | | | 1 | 2 | | mA |
| Latch-Pin High Input Voltage | V _{IH} | | | 2.0 | | | V |
| Latch-Pin Low Input Voltage | V _{IL} | | | | 0.8 | | V |
| Latch-Pin Current | I _{IL} | V _{LE} = 0V | | -1 | -20 | | μ A |

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ELECTRICAL CHARACTERISTICS (continued)

$V_+ = +5V$, $V_- = -5V$, $V_Q = 1.4V$, $V_{LE} = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$. (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|-----------------------|--|------------------------------|--------|-----|-----|-------|
| Propagation Delay (Note 4) | t_{PD+} , t_{PD-} | $\Delta V_{IN} = 100mV$, $V_{OD} = 5mV$ | $T_A = +25^\circ C$ | | 10 | 14 | ns |
| | | | $T_A = T_{MIN}$ TO T_{MAX} | | | 16 | |
| | | $\Delta V_{IN} = 100mV$, $V_{OD} = 20mV$ | $T_A = +25^\circ C$ | | 9 | 12 | |
| | | | $T_A = T_{MIN}$ TO T_{MAX} | | | 15 | |
| Differential Propagation Delay (Note 4) | Δt_{PD} | $\Delta V_{IN} = 100mV$, $V_{OD} = 5mV$ | $T_A = +25^\circ C$ | MAX913 | 2 | 4 | ns |
| | | | | MAX912 | 3 | 5 | |
| Channel-to-Channel Propagation Delay (Note 4) | | $\Delta V_{IN} = 100mV$, $V_{OD} = 5mV$ (MAX912 only) | $T_A = +25^\circ C$ | | 500 | | ps |
| Latch Setup Time (Note 5) | t_{SU} | | | 2 | 0 | | ns |
| Latch Hold Time (Note 5) | t_H | | | 5 | 2 | | ns |
| Latch Propagation Delay (Note 6) | t_{LPD} | | | | 7 | | ns |

Note 1: All specifications are 100% tested at $T_A = +25^\circ C$, unless otherwise noted. Specification limits over temperature ($T_A = T_{MIN}$ to T_{MAX}) are guaranteed by design.

Note 2: Input Offset Voltage (V_{OS}) is defined as the average of the two input offset voltages, measured by forcing first one output, then the other to 1.4V. Input Offset Current (I_{OS}) is defined the same way.

Note 3: Supply currents are measured with V_Q driven to both V_{OH} and V_{OL} (not 1.4V).

Note 4: Propagation Delay (t_{PD}) and Differential Propagation Delay (Δt_{PD}) cannot be measured in automatic handling equipment with low input overdrive values. Characterization and correlation tests have shown that t_{PD} and Δt_{PD} limits can be guaranteed by design. Electrical Characteristic DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to overdrive. Differential Propagation Delay is defined as $\Delta t_{PD} = t_{PD+} - t_{PD-}$.

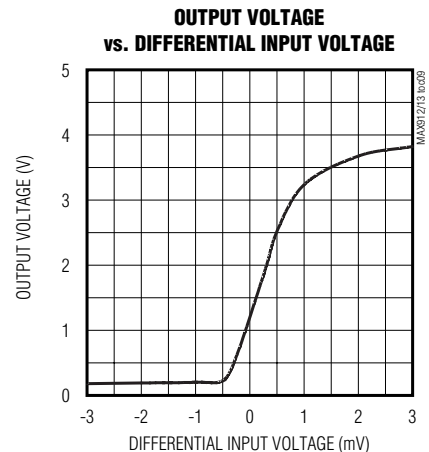
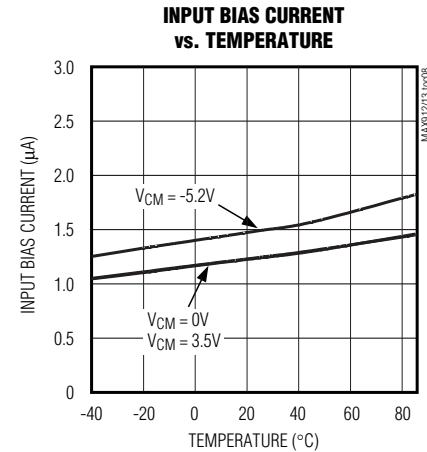
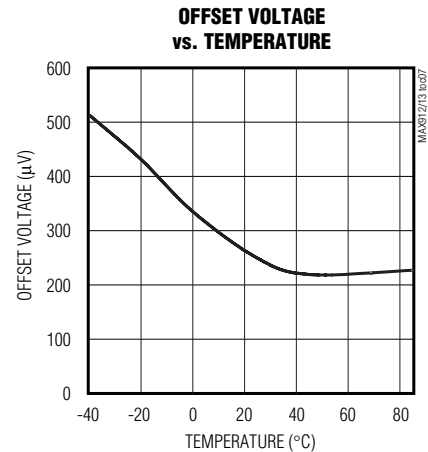
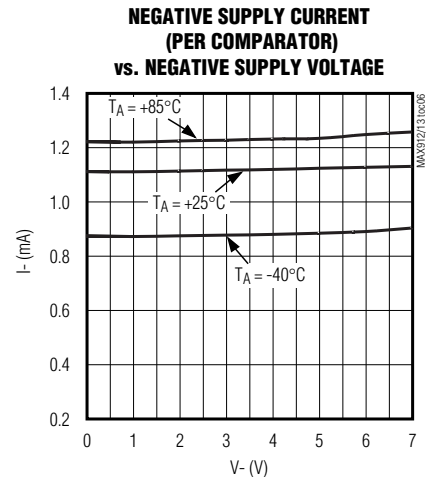
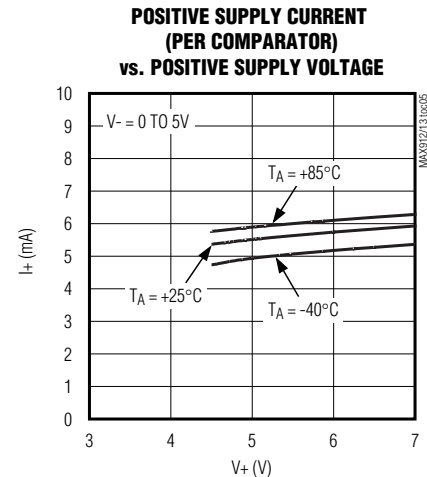
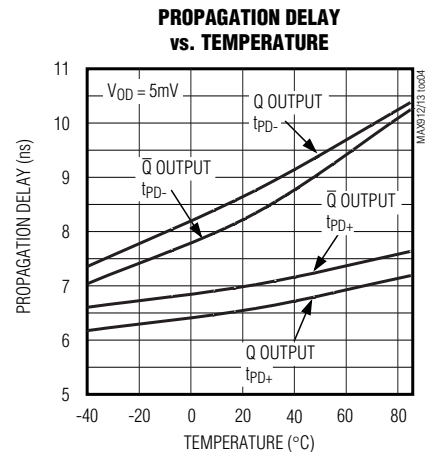
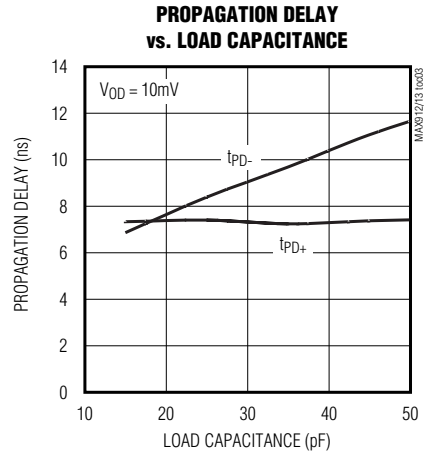
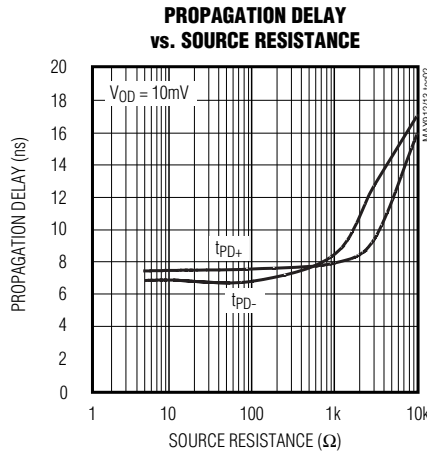
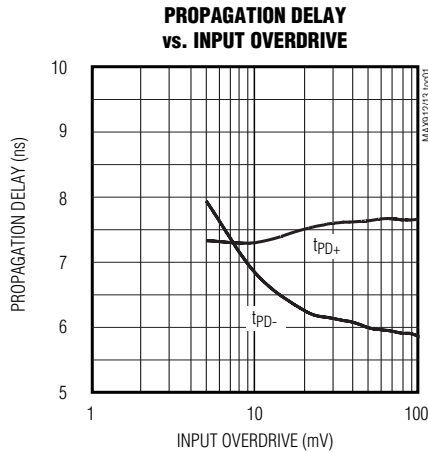
Note 5: Input latch setup time (t_{SU}) is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time (t_H) is the interval after the latch is asserted in which the input signal must be stable. These parameters are guaranteed by design.

Note 6: Latch Propagation Delay (t_{LPD}) is the delay time for the output to respond when the latch-enable pin is deasserted (see *Timing Diagram*).

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Typical Operating Characteristics

($V_+ = +5V$, $V_- = -5V$, $V_{LE} = 0V$, $C_L = 15pF$, $T_A = +25^\circ C$, unless otherwise noted.)



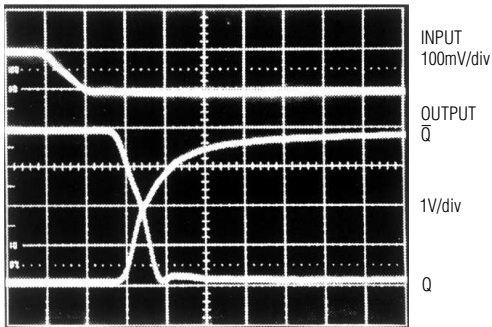
Single/Dual, Ultra-Fast, Low-Power Precision TTL Comparators

Typical Operating Characteristics (continued)

($V_+ = +5V$, $V_- = -5V$, $V_{LE} = 0V$, $C_L = 15pF$, $T_A = +25^\circ C$, unless otherwise noted.)

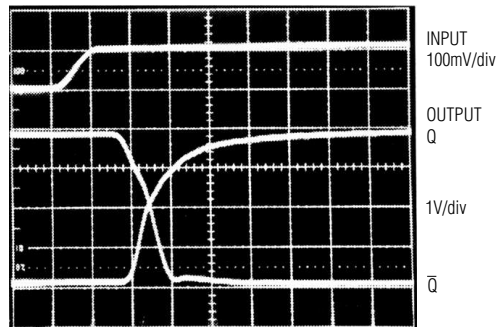
MAX912/MAX913

POSITIVE-TO-NEGATIVE PROPAGATION DELAY



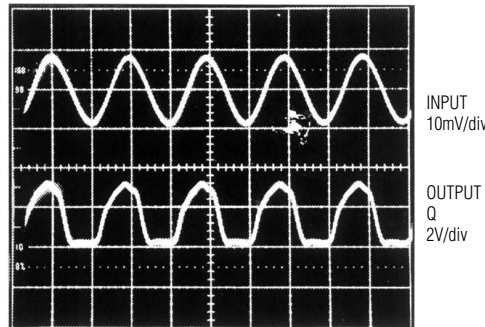
5ns/div

NEGATIVE-TO-POSITIVE PROPAGATION DELAY



5ns/div

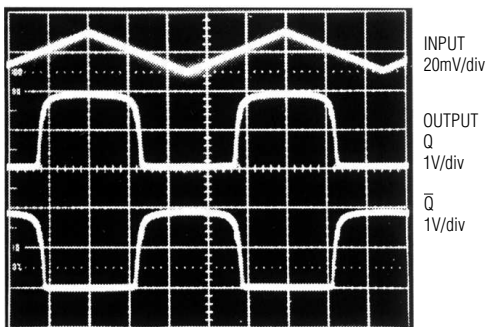
MAX912/MAX913 RESPONSE TO 50MHZ ($\pm 10mV_{p-p}$) SINE WAVE



10ns/div

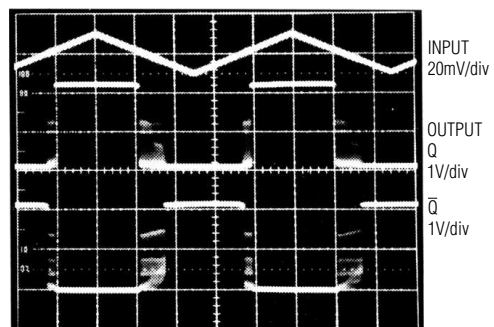
MAX912/MAX913 RESPONSE TO SLOW-MOVING TRIANGLE WAVE

MAX912/MAX913 RESPONSE



20 μ s/div

INDUSTRY-STANDARD 686 RESPONSE



20 μ s/div

Single/Dual, Ultra-Fast, Low-Power Precision TTL Comparators

MAX912 Pin Description

| PIN | NAME | FUNCTION |
|-------|-----------------|--|
| 1 | QA | Comparator A TTL Output |
| 2 | \overline{QA} | Comparator A Complementary TTL Output |
| 3, 14 | GND | Logic Ground. Connect both GND pins to ground. |
| 4 | LEA | Comparator A Latch Enable. QA and \overline{QA} are latched when LEA is TTL high or floating. Comparator A latch is transparent when LEA is low. |
| 5, 12 | N.C. | No Connection. Not internally connected. |
| 6 | V- | Negative Power Supply. -5V for dual supplies (bypass to GND with a 0.1 μ F capacitor) or GND for a single supply. |
| 7 | INA- | Comparator A Inverting Input |
| 8 | INA+ | Comparator A Noninverting Input |
| 9 | INB+ | Comparator B Noninverting Input |
| 10 | INB- | Comparator B Inverting Input |
| 11 | V+ | Positive Power Supply, +5V. Bypass to GND with a 0.1 μ F capacitor. |
| 13 | LEB | Comparator B Latch Enable. QB and \overline{QB} are latched when LEB is TTL high or floating. Comparator B latch is transparent when LEB is low. |
| 15 | \overline{QB} | Comparator B Complementary TTL Output |
| 16 | QB | Comparator B TTL Output |

MAX913 Pin Description

| PIN | NAME | FUNCTION |
|-----|----------------|---|
| 1 | V+ | Positive Power Supply. Bypass to GND with a 0.1 μ F capacitor. |
| 2 | IN+ | Noninverting Input |
| 3 | IN- | Inverting Input |
| 4 | V- | Negative Power Supply. -5V for dual supplies (bypass to GND with a 0.1 μ F capacitor) or GND for a single supply. |
| 5 | LE | Latch Enable. Q and \overline{Q} are latched when LE is TTL high or floating. The comparator latch is transparent when LE is low. |
| 6 | GND | Logic Ground |
| 7 | Q | TTL Output |
| 8 | \overline{Q} | Complementary TTL Output |

Single/Dual, Ultra-Fast, Low-Power Precision TTL Comparators

MAX912/MAX913

Detailed Description

The MAX912 (dual) and MAX913 (single) high-speed comparators have a unique design that prevents oscillation when the comparator is in its linear region. No minimum input slew rate is required.

Many high-speed comparators oscillate in the linear region, as shown in the *Typical Operating Characteristics*' industry-standard 686 response graph. One way to overcome this oscillation is to sample the output after it has passed through the unstable region. Another practical solution is to add hysteresis. Either solution results in a loss of resolution and bandwidth.

Because the MAX912/MAX913 do not need hysteresis, they offer high resolution to all signals—including low-frequency signals.

The MAX912/MAX913 provide a TTL-compatible latch function that holds the comparator output state (Figure 1). As long as Latch Enable (LE) is high or floating, the input signal has no effect on the output state. With LE low, the outputs are controlled by the input differential voltage and the latch is transparent.

Input Amplifier

A comparator can be thought of as having two sections; an input amplifier and a logic interface. The MAX912/MAX913's input amplifier is fully differential with input offset voltage trimmed to below 2.0mV at

+25°C. Input common-mode range extends from 200mV **below** the negative supply rail to 1.5V below the positive power supply. The total common-mode range is 8.7V when operating from ± 5 VDC supplies.

The MAX912/MAX913's amplifier has no built-in hysteresis. For highest accuracy, do not add hysteresis. Figure 2 shows how hysteresis degrades resolution.

Resolution

A comparator's ability to resolve small signal differences—its resolution—is affected by various factors. As with most amplifiers, the most significant factors are the input offset voltage (V_{OS}) and the common-mode and power-supply rejection ratios (CMRR, PSRR). If source impedance is high, input offset current can be significant. If source impedance is unbalanced, the input bias current can introduce another error.

For high-speed comparators, an additional factor in resolution is the comparator's stability in its linear region. Many high-speed comparators are useless in their linear region because they oscillate. This makes the differential input voltage region around 0V unusable, as does a high V_{OS} . Hysteresis does not cure the problem, but acts to keep the input away from its linear range (Figure 2).

The MAX912/MAX913 do not oscillate in the linear region, which greatly enhances the comparator's resolution.

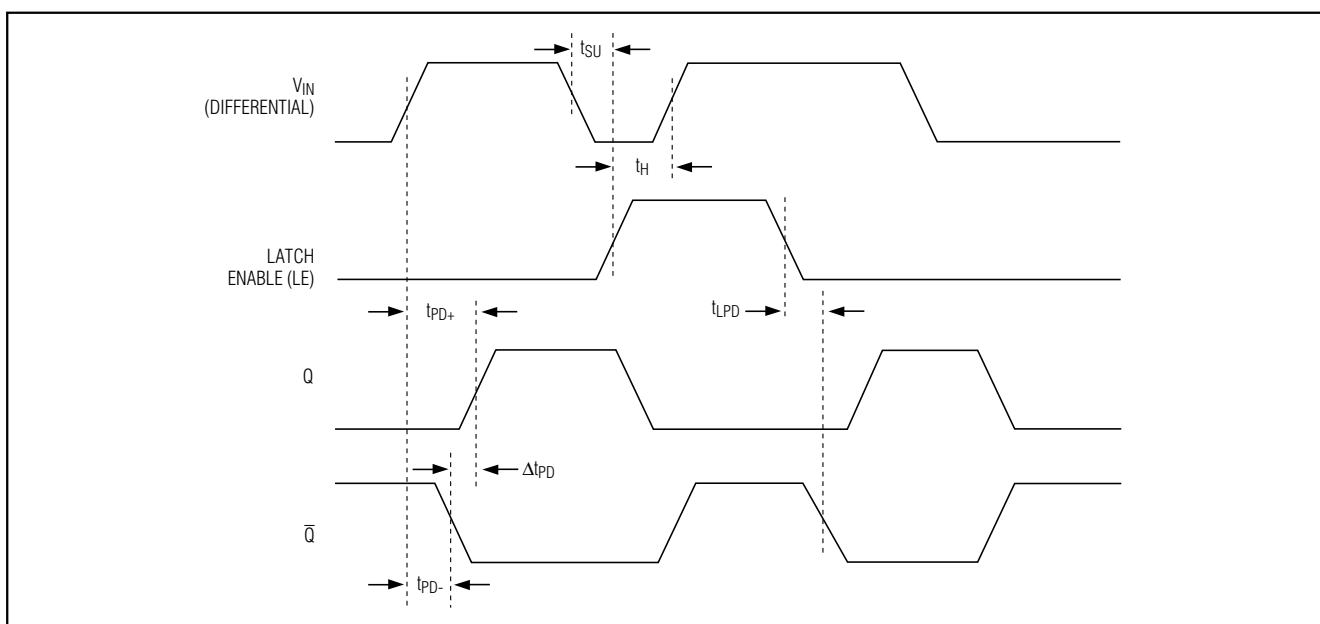


Figure 1. Timing Diagram

Single/Dual, Ultra-Fast, Low-Power Precision TTL Comparators

Applications Information

Power Supplies and Bypassing

The MAX912/MAX913 are tested with $\pm 5V$ power supplies that provide an input common-mode range (V_{CM}) of 8.7V (-5.2V to +3.5V). Operation from a single +5V supply provides a common-mode input range of 3.7V (-0.2V to +3.5). Connect V_- to GND for single-supply operation. The MAX912/MAX913 will operate from a minimum single-supply voltage of +4.5V.

The V_+ supply provides power to both the analog input stage and digital output circuits, whereas the V_- supply only powers the analog section. Bypass V_+ and V_- to ground with 0.1 μF to 1.0 μF ceramic capacitors in parallel with 10 μF or greater tantalum capacitors. Connect the ceramic capacitors very close to the MAX912/MAX913's supply pins, keeping leads short to minimize lead inductance. For particularly noisy applications, use ferrite beads on the power-supply lines.

Board Layout

As with all high-speed components, careful attention to layout is essential for best performance.

- 1) Use a printed circuit board with an unbroken ground plane.
- 2) Pay close attention to the bandwidth of bypass components and keep leads short.
- 3) Avoid sockets; solder the comparator and other components directly to the board to minimize unwanted parasitic inductance and capacitance.

Input Slew Rate

The MAX912/MAX913 design eliminates the input slew-rate requirement imposed on many standard comparators. As long as LE is high after the maximum propagation delay and the input is greater than the comparator's total DC error, the output will be valid without oscillations.

Maximum Clock (LE) and Signal Rate

The maximum clock and signal rate is 70MHz, based on the comparator's rise and fall time with a 5mV overdrive at +25°C (Figure 1). With a 20mV overdrive, the maximum propagation delay is 12ns and the clock signal rate is 85MHz.

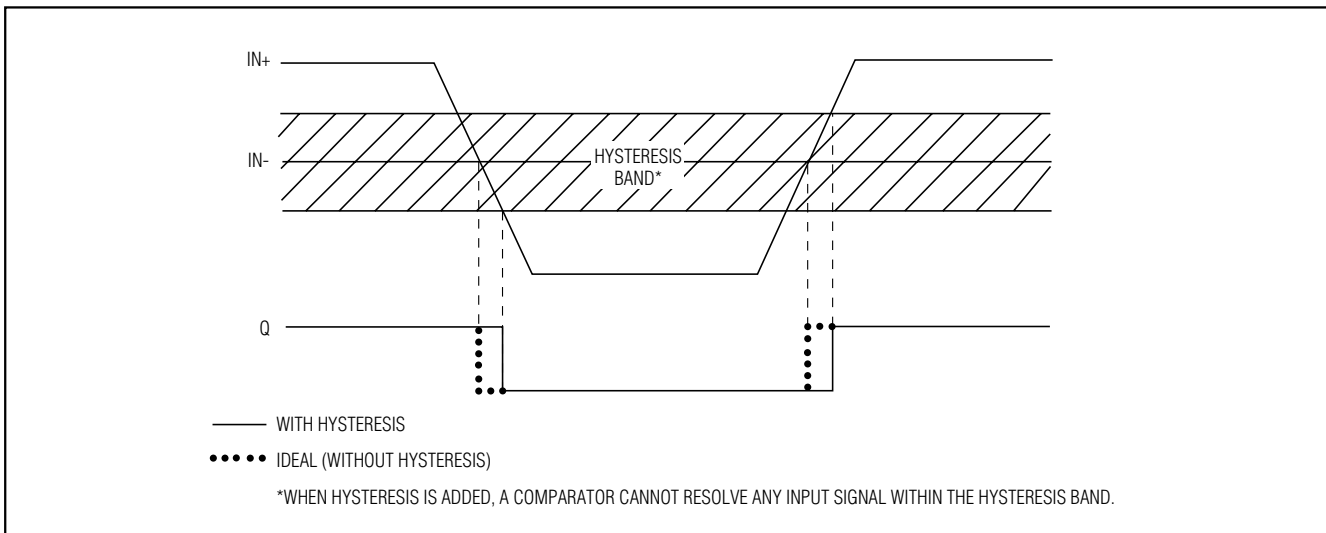


Figure 2. Effect of Hysteresis on Input Resolution

Chip Information

MAX912 TRANSISTOR COUNT: 285

MAX913 TRANSISTOR COUNT: 154

PROCESS: Bipolar

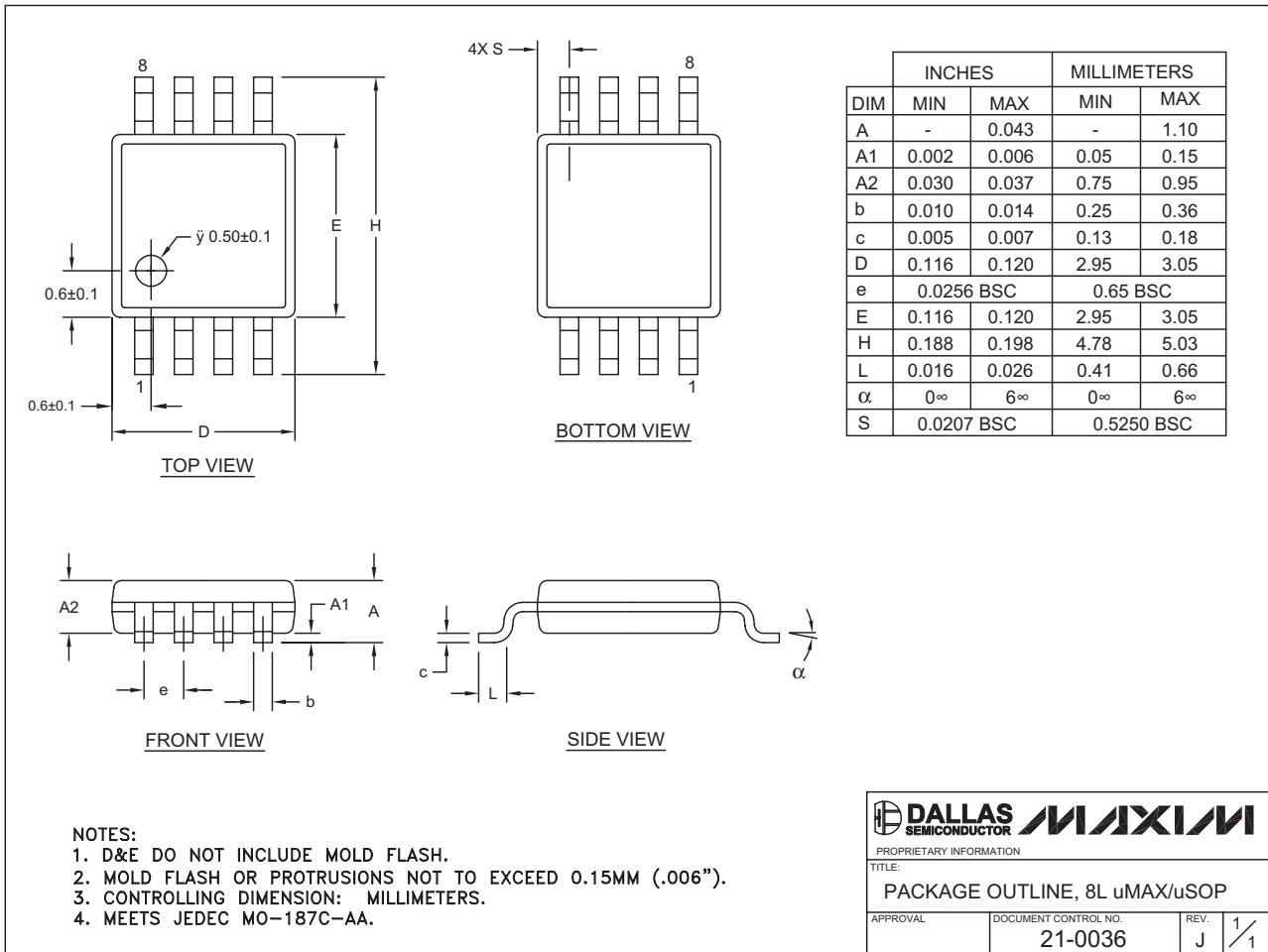
Single/Dual, Ultra-Fast, Low-Power Precision TTL Comparators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX912/MAX913

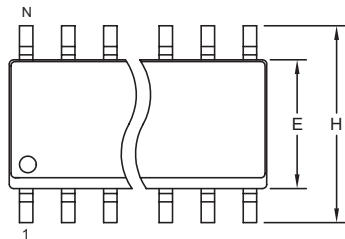
8LUMAXDEPS



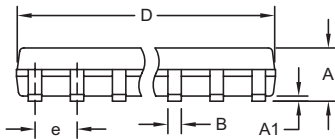
Single/Dual, Ultra-Fast, Low-Power Precision TTL Comparators

Package Information (continued)

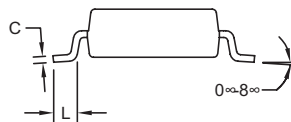
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

| DIM | INCHES | | MILLIMETERS | | N | MS012 |
|-----|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |

SOICN LEPS

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

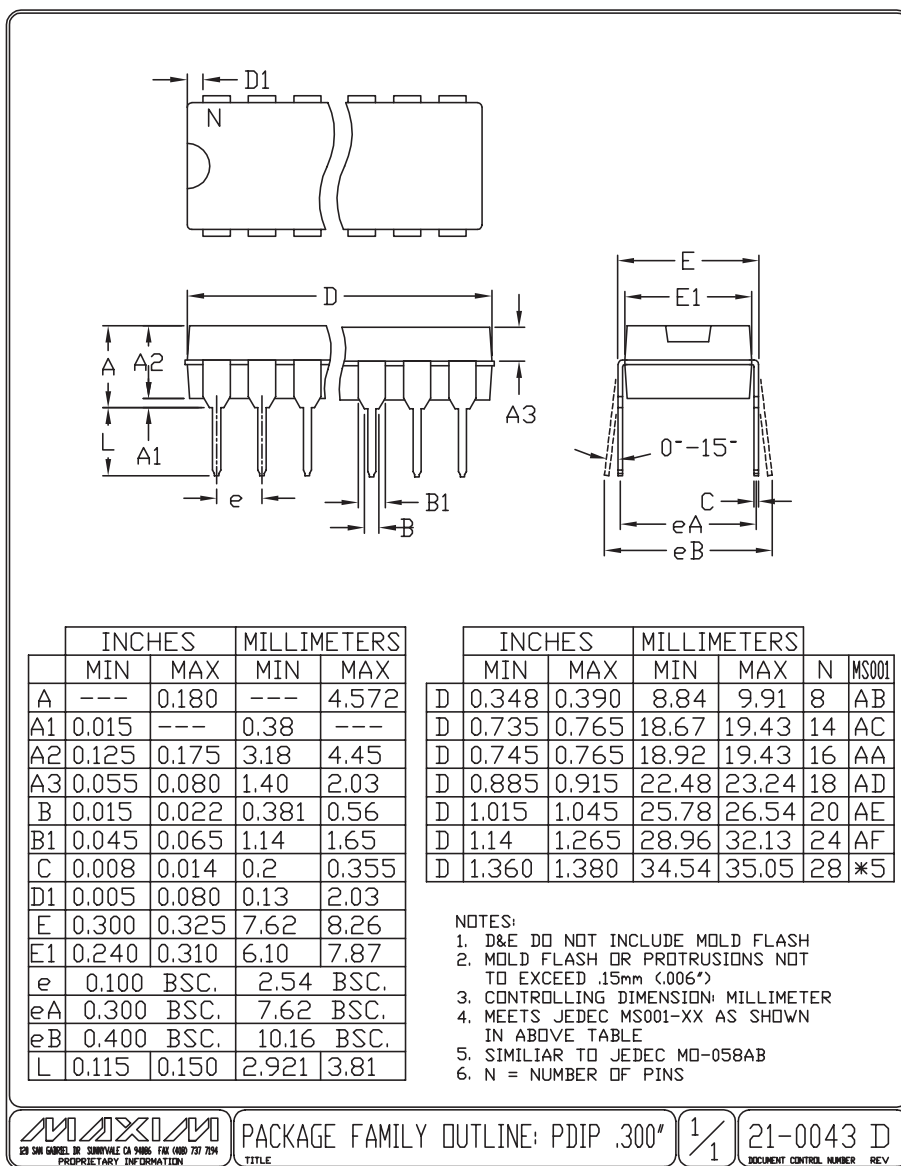
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MAX912/MAX913



PDIPN EPSS

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