19-1042; Rev 0; 10/07

EVALUATION KIT AVAILABLE

TFT-LCD Step-Up DC-DC Converter

General Description

The MAX17062 is a high-performance step-up DC-DC converter that provides a regulated supply voltage for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs). The MAX17062 incorporates current-mode, fixed-frequency, pulse-width modulation (PWM) circuitry with a built-in n-channel power MOSFET to achieve high efficiency and fast-transient response.

Users can select 640kHz or 1.2MHz operation using a logic input pin (FREQ). The high switching frequencies allow the use of ultra-small inductors and low-ESR ceramic capacitors. The current-mode architecture provides fast transient response to pulsed loads. A compensation pin (COMP) gives users flexibility in adjusting loop dynamics. The 22V internal MOSFET can generate output voltages up to 20V from an input voltage between 2.6V and 5.5V. Soft-start slowly ramps the input current and is programmed with an external capacitor.

The MAX17062 is available in a 10-pin TDFN package.

Applications

Notebook Computer Displays

LCD Monitor Panels

LCD TV Panels

Features

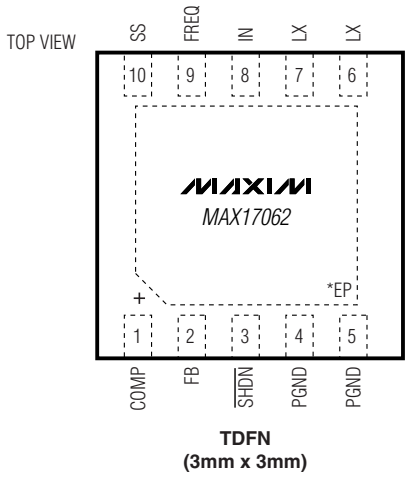
- **90% Efficiency**
- **Adjustable Output from V_{IN} to 20V**
- **2.6V to 5.5V Input Supply Range**
- **Input Supply Undervoltage Lockout**
- **Pin-Programmable 640kHz/1.2MHz Switching Frequency**
- **Programmable Soft-Start**
- **Improved EMI**
- **FB Regulation Voltage Tolerance < 1%**
- **Small 10-Pin TDFN Package**
- **Thermal-Overload Protection**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX17062ETB+T	-40°C to +85°C	10 TDFN-EP* (3mm x 3mm)	T1033-2

+Denotes a lead-free package.
**EP = Exposed pad.*
T = Tape and reel.

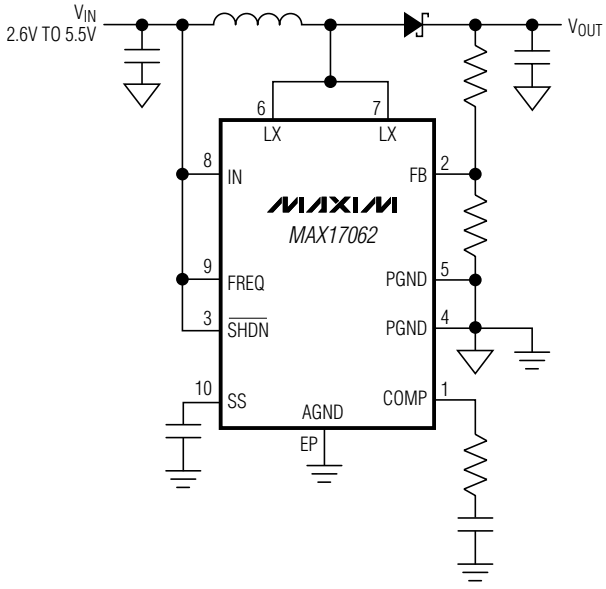
Pin Configuration



TDFN (3mm x 3mm)

**EP = EXPOSED PAD.*

Minimal Operating Circuit



TFT-LCD Step-Up DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

LX to AGND .....-0.3V to +22V
IN, $\overline{SHDN}$, FREQ, FB to AGND .....-0.3V to +7.5V
COMP, SS to AGND .....-0.3V to (V_{IN} + 0.3V)
PGND to AGND .....-0.3V to +0.3V
LX Switch Maximum Continuous RMS Current 3.2A

Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{\overline{SHDN}}$ = 3V, FREQ = 3V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{OUT} < 18V	2.6		5.5	V
	18V < V_{OUT} < 20V	4.0		5.5	
Output Voltage Range				20	V
IN Undervoltage-Lockout Threshold	V_{IN} rising, typical hysteresis is 50mV	2.30	2.45	2.57	V
IN Quiescent Current	V_{FB} = 1.3V, not switching		0.3	0.6	mA
	V_{FB} = 1.0V, switching		1.5	2.5	
IN Shutdown Current	$\overline{SHDN}$ = AGND, T_A = +25°C		0.01	10.0	µA
	$\overline{SHDN}$ = AGND, T_A = +85°C		0.01		
Thermal Shutdown	Temperature rising		160		°C
	Hysteresis		20		
ERROR AMPLIFIER					
FB Regulation Voltage	Level to produce V_{COMP} = 1.24V	1.23	1.24	1.25	V
FB Input Bias Current	V_{FB} = 1.24V	75	150	225	nA
FB Line Regulation	Level to produce V_{COMP} = 1.24V, V_{IN} = 2.6V to 5.5V		0.01	0.15	%/V
Transconductance		110	250	450	µS
Voltage Gain			2400		V/V
Shutdown FB Input Voltage	$\overline{SHDN}$ = AGND	0.05	0.10	0.15	V
OSCILLATOR					
Frequency	FREQ = AGND	500	640	780	kHz
	FREQ = IN	1000	1200	1400	
Maximum Duty Cycle		88	91	94	%
n-CHANNEL MOSFET					
Current Limit	V_{FB} = 1V, 75% duty cycle, IN = 5V	3.9	4.6	5.3	A
On-Resistance	IN = 5V		100	170	mΩ
	IN = 3V		125	210	
Leakage Current	V_{LX} = 20V		11	20	µA
Current-Sense Transresistance	IN = 5V	0.09	0.15	0.25	V/A
SOFT-START					
Reset Switch Resistance				100	Ω
Charge Current	V_{SS} = 1.2V	2	4	6	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = 3V, FREQ = 3V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS					
$\overline{SHDN}$, FREQ Input Low Voltage	V_{IN} = 2.6V to 5.5V			0.3 × V_{IN}	V
$\overline{SHDN}$, FREQ Input High Voltage	V_{IN} = 2.6V to 5.5V	0.7 × V_{IN}			V
$\overline{SHDN}$, FREQ Input Hysteresis	V_{IN} = 2.6V to 5.5V		0.1 × V_{IN}		V
FREQ Pulldown Current		3	6	9	µA
$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = AGND, T_A = +25°C	-1		+1	µA
	$\overline{SHDN}$ = AGND, T_A = +85°C		0		

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{\overline{SHDN}}$ = 3V, FREQ = 3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{OUT} < 18V	2.6		5.5	V
	18V < V_{OUT} < 20V	4.0		5.5	
Output Voltage Range				20	V
IN Undervoltage-Lockout Threshold	V_{IN} rising, typical hysteresis is 50mV	2.30		2.57	V
IN Quiescent Current	V_{FB} = 1.3V, not switching			0.6	mA
	V_{FB} = 1.0V, switching			2.5	
ERROR AMPLIFIER					
FB Regulation Voltage	Level to produce V_{COMP} = 1.24V	1.227		1.253	V
FB Input Bias Current	V_{FB} = 1.24V			225	nA
FB Line Regulation	Level to produce V_{COMP} = 1.24V, V_{IN} = 2.6V to 5.5V			0.15	%/V
Transconductance		110		450	µS
Shutdown FB Input Voltage	$\overline{SHDN}$ = AGND	0.05		0.15	V
OSCILLATOR					
Frequency	FREQ = AGND	450		830	kHz
	FREQ = IN	950		1500	
Maximum Duty Cycle		87		95	%
n-CHANNEL MOSFET					
Current Limit	V_{FB} = 1V, 75% duty cycle, IN = 5V	3.9		5.3	A
On-Resistance	IN = 5V			170	mΩ
	IN = 3V			210	
Current-Sense Transresistance	IN = 5V	0.09		0.25	V/A
SOFT-START					
Reset Switch Resistance				100	Ω
Charge Current	V_{SS} = 1.2V	2		6	µA

TFT-LCD Step-Up DC-DC Converter

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = 3V, FREQ = 3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

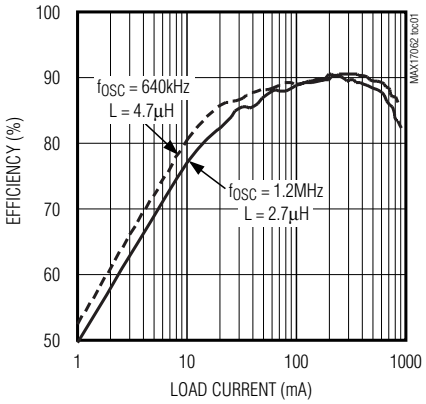
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS					
$\overline{SHDN}$, FREQ Input Low Voltage	V_{IN} = 2.6V to 5.5V			0.3 × V_{IN}	V
$\overline{SHDN}$, FREQ Input High Voltage	V_{IN} = 2.6V to 5.5V	0.7 × V_{IN}			V

Note 1: Limits are 100% tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design.

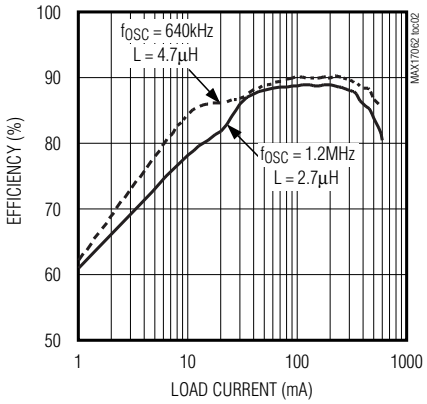
Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = 5V, V_{MAIN} = 15V, T_A = +25°C, unless otherwise noted.)

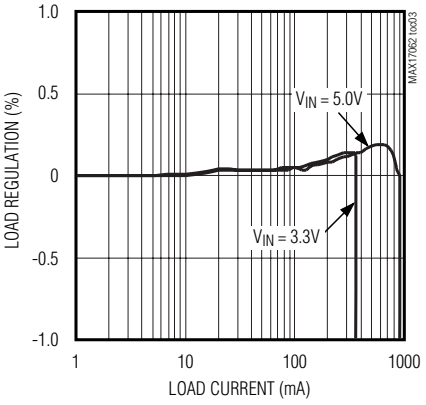
EFFICIENCY vs. LOAD CURRENT (V_{IN} = 5V, V_{OUT} = 15V)



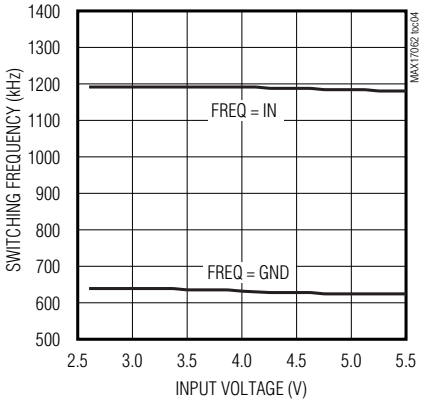
EFFICIENCY vs. LOAD CURRENT (V_{IN} = 3.3V, V_{OUT} = 9V)



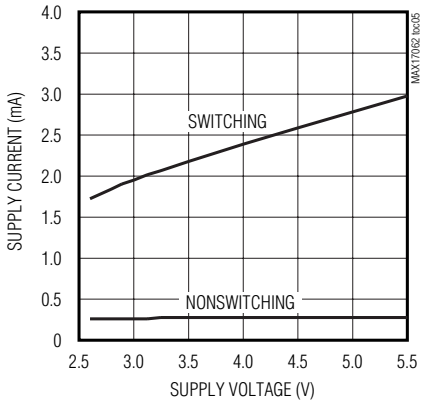
LOAD REGULATION (V_{OUT} = 15V)



SWITCHING FREQUENCY vs. INPUT VOLTAGE



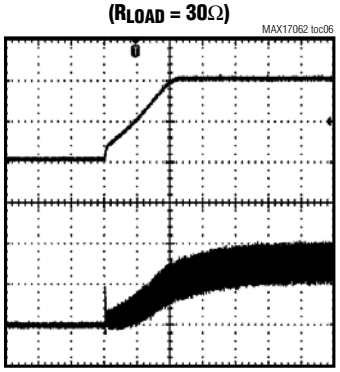
SUPPLY CURRENT vs. SUPPLY VOLTAGE



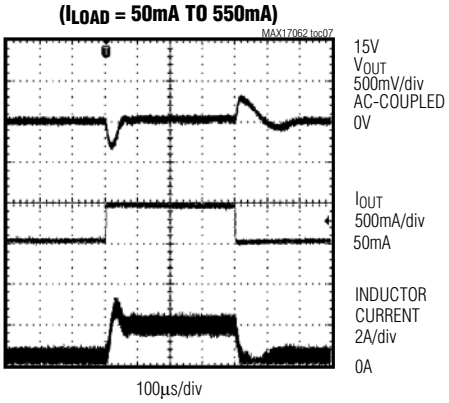
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 5V, V_{MAIN} = 15V, T_A = +25°C, unless otherwise noted.)

SOFT-START
(R_{LOAD} = 30Ω)

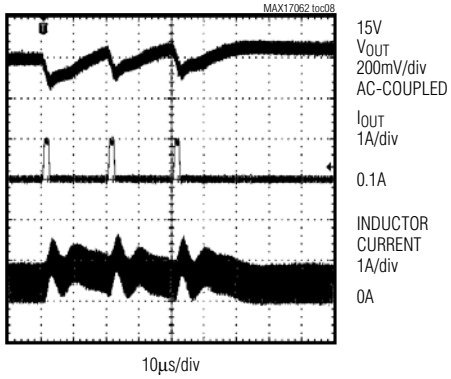


LOAD-TRANSIENT RESPONSE
(I_{LOAD} = 50mA TO 550mA)



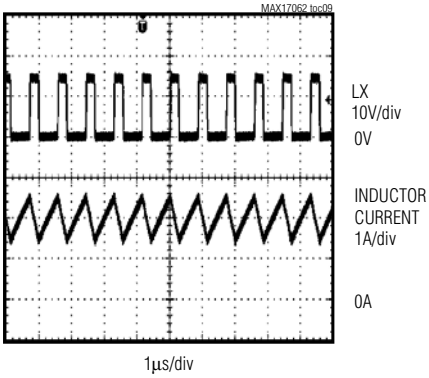
L = 2.7µH
R_{COMP} = 47kΩ
C_{COMP1} = 560pF

PULSED LOAD-TRANSIENT RESPONSE
(I_{LOAD} = 100mA TO 1.1A)



L = 2.7µH
R_{COMP} = 47kΩ
C_{COMP1} = 560pF

SWITCHING WAVEFORMS
(I_{LOAD} = 600mA)



Pin Description

PIN	NAME	FUNCTION
1	COMP	Compensation Pin for Error Amplifier. Connect a series RC from COMP to ground. See the *Loop Compensation* section for component selection guidelines.
2	FB	Feedback Pin. The FB regulation voltage is 1.24V nominal. Connect an external resistive voltage-divider between the step-up regulator's output (V_{OUT}) and AGND, with the center tap connected to FB. Place the divider close to the IC and minimize the trace area to reduce noise coupling. Set V_{OUT} according to the *Output Voltage Selection* section.
3	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to turn off the MAX17062.
4, 5	PGND	Power Ground. Connect pins 4 and 5 directly together.
6, 7	LX	Switch Pin. LX is the drain of the internal MOSFET. Connect the inductor/rectifier diode junction to LX and minimize the trace area for lower EMI. Connect pins 6 and 7 together.
8	IN	Supply Pin. Bypass IN with a minimum 1µF ceramic capacitor directly to AGND.
9	FREQ	Frequency-Select Input. When FREQ is low, the oscillator frequency is set to 640kHz. When FREQ is high, the frequency is 1.2MHz. This input has a 6µA pulldown current.
10	SS	Soft-Start Control Pin. Connect a soft-start capacitor (C_{SS}) to this pin. Leave open for no soft-start. The soft-start capacitor is charged with a constant current of 4µA. Full current limit is reached when the voltage of SS pin is charged to 1.5V, which is the current-limit time, $t = 2.4 \times 10^5 C_{SS}$. The soft-start capacitor is discharged to ground when $\overline{SHDN}$ is low. When $\overline{SHDN}$ goes high, the soft-start capacitor is charged to 0.4V, after which soft-start begins.
EP	AGND	Exposed Pad. Connect to AGND.

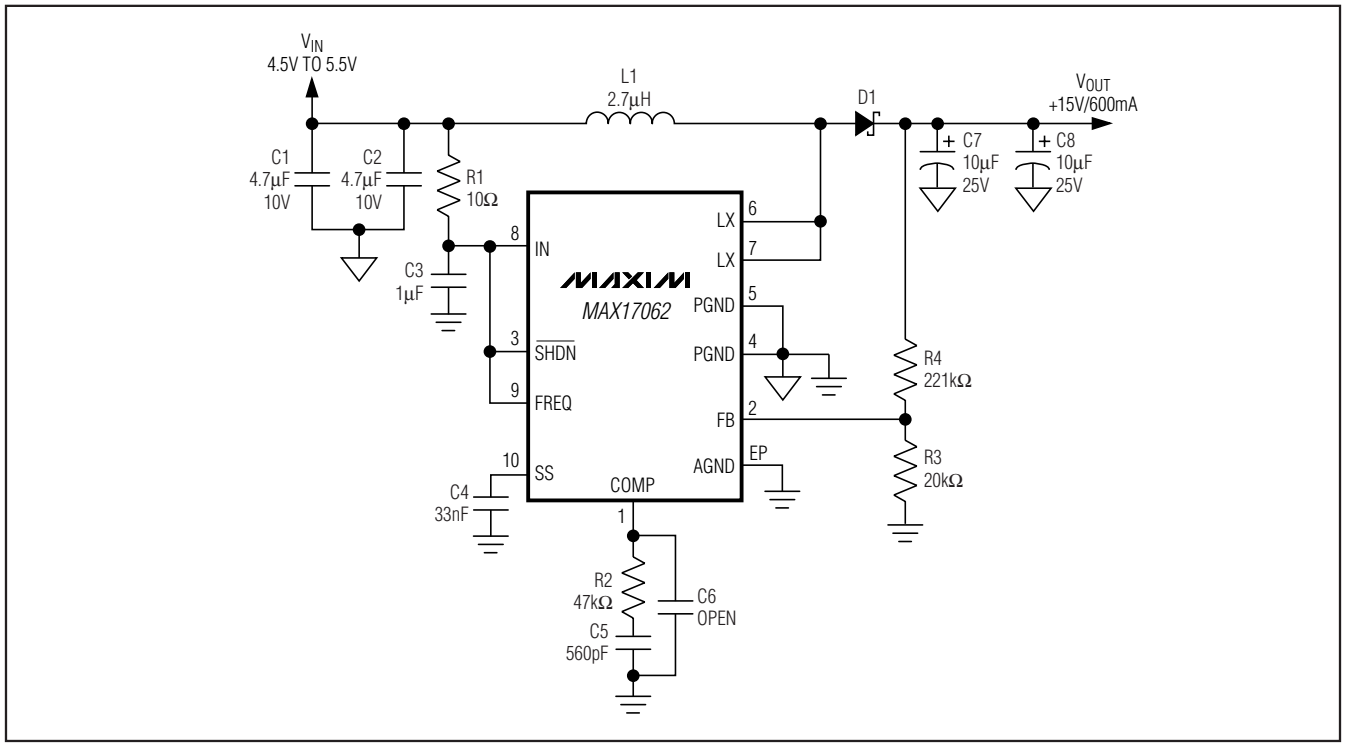


Figure 1. Typical Operating Circuit

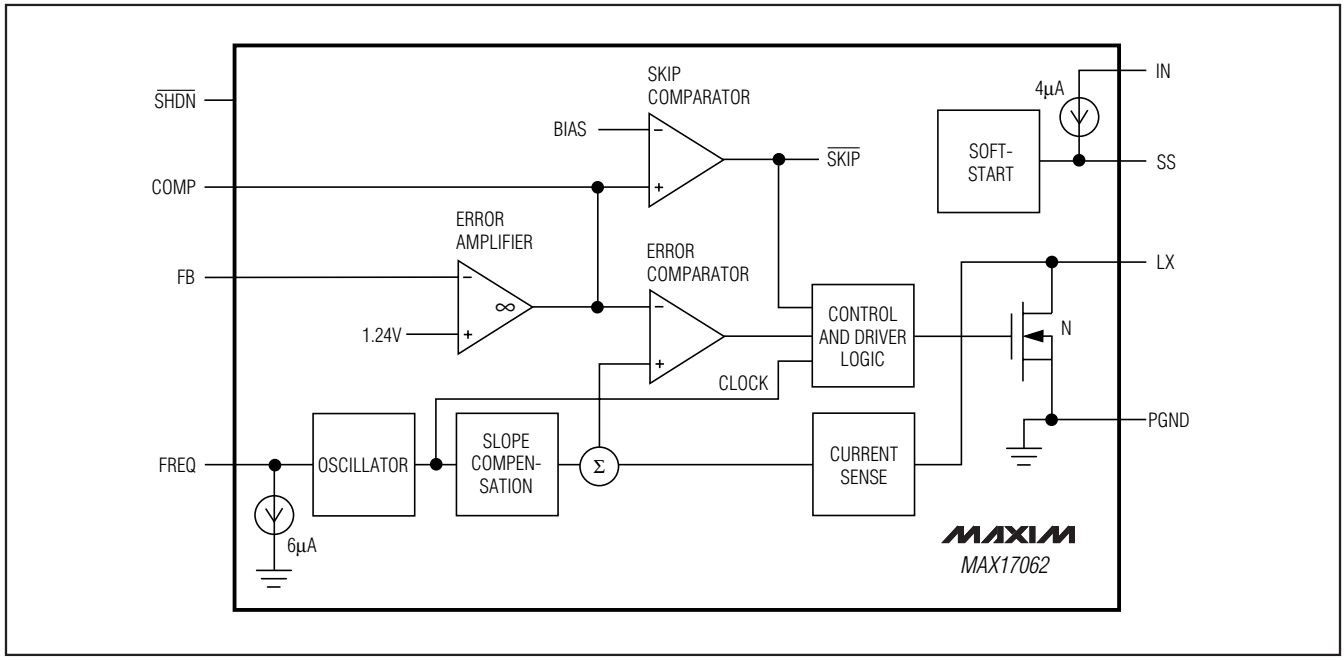


Figure 2. MAX17062 Functional Diagram

Detailed Description

The MAX17062 is a highly efficient power supply that employs a current-mode, fixed-frequency, PWM architecture for fast-transient response and low-noise operation. The device regulates the output voltage through a combination of an error amplifier, two comparators, and several signal generators (Figure 2). The error amplifier compares the signal at FB to 1.24V and varies the COMP output. The voltage at COMP determines the current trip point each time the internal MOSFET turns on. As the load changes, the error amplifier sources or sinks current to the COMP output to command the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal.

At light loads, this architecture allows the MAX17062 to "skip" cycles to prevent overcharging the output voltage.

In this region of operation, the inductor ramps up to a peak value of approximately 50mA, discharges to the output, and waits until another pulse is needed again.

Output Current Capability

The output current capability of the MAX17062 is a function of current limit, input voltage, operating frequency, and inductor value. Because of the slope compensation used to stabilize the feedback loop, the inductor current limit depends on the duty cycle. The current limit is determined by the following equation:

$$I_{LIM} = (1.26 - 0.35 \times D) \times I_{LIM\_EC}$$

where I_{LIM_EC} is the current limit specified at 75% duty cycle (see the *Electrical Characteristics* table) and D is the duty cycle.

The output current capability depends on the current-limit value and is governed by the following equation:

$$I_{OUT(MAX)} = \left[I_{LIM} - \frac{0.5 \times D \times V_{IN}}{f_{OSC} \times L} \right] \times \frac{V_{IN}}{V_{OUT}} \times \eta$$

where I_{LIM} is the current limit calculated above, η is the regulator efficiency (85% nominal), and D is the duty cycle. The duty cycle when operating at the current limit is:

$$D = \frac{V_{OUT} - V_{IN} + V_{DIODE}}{V_{OUT} - I_{LIM} \times R_{ON} + V_{DIODE}}$$

where V_{DIODE} is the rectifier diode forward voltage and R_{ON} is the on-resistance of the internal MOSFET.

Soft-Start

The MAX17062 can be programmed for soft-start upon power-up with an external capacitor. When the shutdown pin is taken high, the soft-start capacitor (C_{SS}) is immediately charged to 0.4V. Then the capacitor is charged at a constant current of 4µA (typ). During this time, the SS voltage directly controls the peak inductor current, allowing 0A at V_{SS} = 0.4V to the full current limit at V_{SS} = 1.5V. The maximum load current is available after the soft-start is completed. When the $\overline{SHDN}$ pin is taken low, the soft-start capacitor is discharged to ground.

Frequency Selection

The MAX17062's frequency can be user selected to operate at either 640kHz or 1.2MHz. Connect FREQ to AGND for 640kHz operation. For a 1.2MHz switching frequency, connect FREQ to IN. This allows the use of small, minimum-height external components while maintaining low output noise. FREQ has an internal pulldown, allowing the user the option of leaving FREQ unconnected for 640kHz operation.

Shutdown

The MAX17062 shuts down to reduce the supply current to 0.01µA when $\overline{SHDN}$ is low. In this mode, the internal reference, error amplifier, comparators, and biasing circuitry turn off, and the n-channel MOSFET is turned off. The step-up regulator's output is connected to IN by the external inductor and rectifier diode.

Thermal-Overload Protection

Thermal-overload protection prevents excessive power dissipation from overheating the MAX17062. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately activates the fault protection, which shuts down the MAX17062, allowing the device to cool down. Once the device cools down by approximately 20°C, the MAX17062 starts up automatically.

Applications Information

Step-up regulators using the MAX17062 can be designed by performing simple calculations for a first iteration. All designs should be prototyped and tested prior to production. Table 1 provides a list of power components for the typical applications circuit (Figure 1). Table 2 lists component suppliers.

External-component-value choice is primarily dictated by the output voltage and the maximum load current, as well as maximum and minimum input voltages. Begin by selecting an inductor value. Once L is known, choose the diode and capacitors.

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient-response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C2	4.7µF ±10%, 10V X5R ceramic capacitors (0603) TDK C1608X5RIA475K
C7, C8	10µF±10%, 25V X5R ceramic capacitors (1210) TDK C3225X5RIE106K
D1	3A, 30V Schottky diode (M-Flat) Toshiba CMS03
L1	2.7µH ±20% power inductor TOKO FDV0630-2R7M

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
TDK	847-803-6100	847-390-4405	www.component.tdk.com
TOKO	847-297-0070	847-699-7864	www.tokoam.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec

AC characteristics of the inductor core material and the ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(MAX)} \times f_{OSC}}\right) \left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(MAX)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times (V_{MAIN} - V_{IN(MIN)})}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17062's LX current limit (I_{LIM}) should exceed I_{PEAK}, and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit (Figure 1), the maximum load current ($I_{MAIN(MAX)}$) is 600mA with a 15V output and a typical input voltage of 5V. Choosing an LIR of 0.5 and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{5V}{15V}\right)^2 \left(\frac{15V - 5V}{0.6A \times 1.2MHz}\right) \left(\frac{0.85}{0.50}\right) \approx 2.7\mu H$$

Using the circuit's minimum input voltage (4.5V) and estimating efficiency of 85% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.6A \times 15V}{4.5V \times 0.85} \approx 2.35A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{4.5V \times (15V - 4.5V)}{2.7\mu H \times 15V \times 1.2MHz} \approx 0.97A$$

$$I_{PEAK} = 2.35A + \frac{0.97A}{2} \approx 2.84A$$

Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}} \left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

TFT-LCD Step-Up DC-DC Converter

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 4.7µF ceramic capacitors are used in the *Typical Operating Circuit* (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in the typical operating circuit. Ensure a low-noise supply at IN by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter (see R1 and C3 in Figure 1).

Rectifier Diode Selection

The MAX17062's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. The diode should be rated to handle the output voltage and the peak switch current. Make sure that the diode's peak current rating is at least I_{PEAK} calculated in the *Inductor Selection* section and that its breakdown voltage exceeds the output voltage.

Output Voltage Selection

The MAX17062 operates with an adjustable output from V_{IN} to 20V. Connect a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to FB (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{FB}} - 1 \right)$$

where V_{FB}, the step-up regulator's feedback set point, is 1.24V (typ). Place R1 and R2 close to the IC.

Loop Compensation

The voltage feedback loop needs proper compensation to prevent excessive output ripple and poor efficiency caused by instability. This is done by connecting a resistor (R_{COMP}) and capacitor (C_{COMP}) in series from COMP to AGND, and another capacitor (C_{COMP2}) from COMP to AGND. R_{COMP} is chosen to set the high-frequency integrator gain for fast transient response, while C_{COMP} is chosen to set the integrator zero to maintain loop stability. The second capacitor, C_{COMP2}, is chosen to cancel the zero introduced by output-capacitance ESR. For optimal performance, choose the components using the following equations:

$$R_{COMP} \approx \frac{315 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{V_{OUT} \times C_{OUT}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

$$C_{COMP2} \approx \frac{0.0036 \times R_{ESR} \times L \times I_{MAIN(MAX)}}{V_{IN} \times V_{OUT}}$$

For the ceramic output capacitor, where ESR is small, C_{COMP2} is optional. The best gauge of correct loop compensation is by inspecting the transient response of the MAX17062. Adjust R_{COMP} and C_{COMP} as necessary to obtain optimal transient performance.

Soft-Start Capacitor

The soft-start capacitor should be large enough that it does not reach final value before the output has reached regulation. Calculate C_{SS} to be:

$$C_{SS} > 21 \times 10^{-6} \times C_{OUT} \times \left(\frac{V_{OUT}^{2} - V_{IN} \times V_{OUT}}{V_{IN} \times I_{INRUSH} - I_{OUT} \times V_{OUT}} \right)$$

where C_{OUT} is the total output capacitance including any bypass capacitor on the output bus, V_{OUT} is the maximum output voltage, I_{INRUSH} is the peak inrush current allowed, I_{OUT} is the maximum output current during power-up, and V_{IN} is the minimum input voltage.

The load must wait for the soft-start cycle to finish before drawing a significant amount of load current. The duration after which the load can begin to draw maximum load current is:

$$t_{MAX} = 2.4 \times 10^{5} \times C_{SS}$$

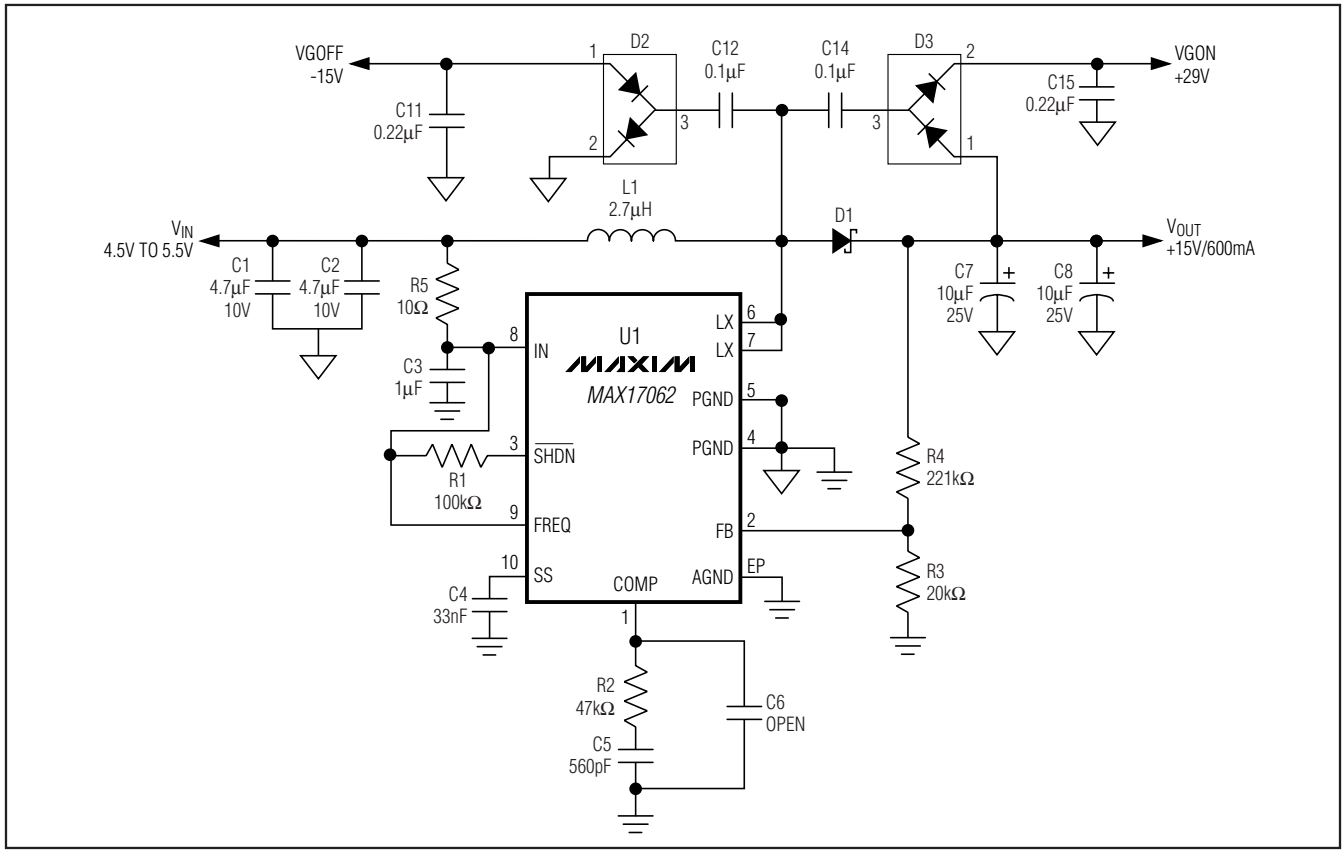


Figure 3. Multiple-Output TFT-LCD Power Supply

Multiple-Output Power Supply for TFT-LCD

Figure 3 shows a power supply for active-matrix TFT-LCD flat-panel displays. Output-voltage transient performance is a function of the load characteristic. Add or remove output capacitance (and recalculate compensation-network component values) as necessary to meet the required transient performance. Regulation performance for secondary outputs (VGON and VGOFF) depends on the load characteristics of all three outputs.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Minimize the area of high-current loops by placing the inductor, rectifier diode, and output capacitors near the input capacitors and near the LX and PGND pins. The high-current output loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from LX switch node to the rectifier diode (D1) to the output capacitors, and reconnecting negative terminals of output capacitors to PGND of the IC. This loop has very high di/dt, and it is critical to minimize the area of this loop. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.

2) Create a power ground island (PGND) consisting of the input and output capacitor grounds and PGND pins. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the feedback-divider ground connection, the COMP and SS capacitor ground connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pins directly to the exposed backside pad. Make no other connections between these separate ground planes.

3) Place the feedback voltage-divider-resistors as close to the FB pin as possible. The divider's center trace should be kept short. Placing the resistors far away causes the FB trace to become an antenna that can pick up switching noise. Avoid running the feedback trace near LX.
4) Place the IN pin bypass capacitor as close to the device as possible. The ground connection of the IN bypass capacitor should be connected directly to AGND pins with a wide trace.
5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and analog ground. Use DC traces as a shield if necessary.

Refer to the MAX17062 Evaluation Kit for an example of proper board layout.

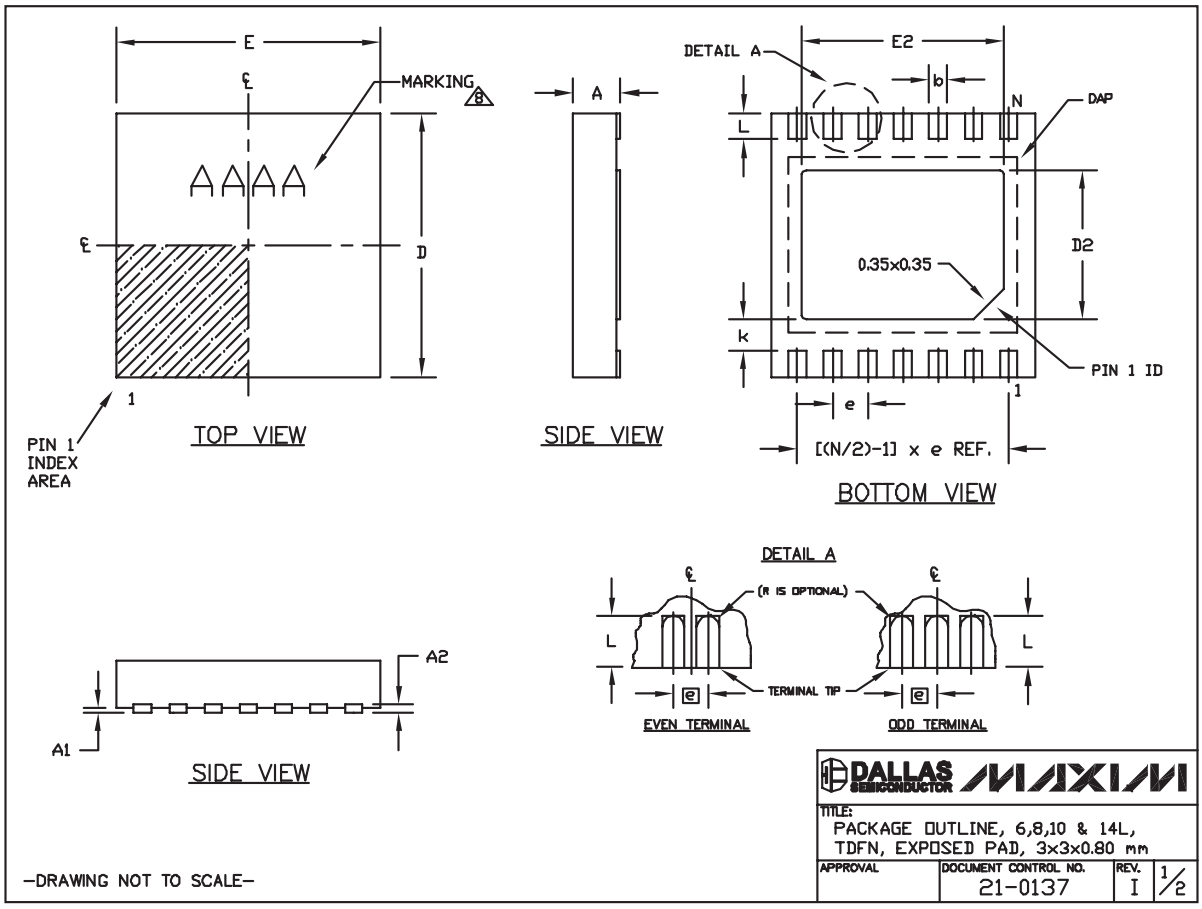
Chip Information

TRANSISTOR COUNT: 3612

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



TFT-LCD Step-Up DC-DC Converter

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

-DRAWING NOT TO SCALE-