SCOPE: CMOS TTL COMPATIBLE ANALOG SWITCHES

Device Type	Generic Number	Circuit Function
01	IH5040M(x)/883B	SPST
02	IH5041M(x)/883B	Dual SPST
03	IH5042M(x)/883B	SPDT
04	IH5043M(x)/883B	Dual SPDT
05	IH5044M(x)/883B	DPST
06	IH5045M(x)/883B	Dual DPST
07	IH5047M(x)/883B	4 PST

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JE	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
FD	CDFP3-F14	14 LEAD FLATPACK	F14

Absolute Maximum Ratings:

V^+ to V^- 44V
V^+ to V_D 30V
V_D to V^- 30V
V_D to V_S ..... ±22V
V_L to V^- 33V
V_L to V_{IN} 30V
V_L to GND 20V
V_{IN} to GND 20V
Digital Input Overvoltage Range ..... (V^+ +0.3V) to (V^+ -38V)
V_S or V_D 1/.....(V^-) -0.3V to (V^+)+0.3V
Continuous Current, Any terminal 30mA
Peak Current, S or D (Pulsed at 1ms, 10% duty cycle max) 100mA
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 lead CERDIP (derate 10.0mW/°C above +70°C) 800mW
14 lead Flatpack (derate 5.7mW/°C above +70°C) 457mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 16 lead CERDIP..... 50°C/W
Case Outline 14 lead Flatpack ..... 70°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 16 lead CERDIP..... 100°C/W
Case Outline 14 lead Flatpack ..... 175°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V^+) ..... +15V
Negative Supply Voltage (V^-) ..... -15V
V_{AL} (max) 0.8V
V_{AH} (min) 2.4V

NOTE 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{AH}=2.4V, V_{AL}=0.8V, V_L=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
INPUT							
Input Logic Current	$I_{IN(ON)}$	V_{IN}=2.4V, 5V	1,3 2	All		±1 ±10	µA
Input Logic Current	$I_{IN(OFF)}$	V_{IN}=0.8V	1,3 2	All		±1 ±10	µA
Input Logic Low	V_{IL}		1,2,3	All		0.8	V
Input Loigic High	V_{IH}		1,2,3	All	2.4		V
SWITCH							
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S =±10mA, V_{ANALOG}=±10V,	1,3 2	All		75 150	Ω
On-Resistance Match Between Channels	$\Delta r_{DS(ON)}$	I_S =10mA, V_D=±10V, NOTE 2	1	All		10	Ω
Analog Signal Handling Capability	V_{ANALOG}		1	All	±15		V
Switch- OFF Leakage Current	$I_{S(OFF)}$	V_{ANALOG}=±10V	1 2	All		±1 ±100	nA
Drain- OFF Leakage Current	$I_{D(OFF)}$	V_{ANALOG}=±10V	1 2	All		±1 ±100	nA
Switch-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D=V_S=±10V	1 2	All		±2 ±200	nA
SUPPLY							
Positive Supply Current	I+	V_A=0V, 5V	1,3 2	All		10 100	µA
Negative Supply Current	I-	V_A=0V, 5V	1,3 2	All		10 100	µA
Logic Supply Current	I_L	V_A=0V, 5V	1,3 2	All		10 100	µA
Ground Current	I_{GND}	V_A=0V, 5V	1,3 2	All		10 100	µA
DYNAMIC							
Turn-On Time	t_{ON}	Figure 1	9,11 10	All		450 550	ns
Turn-Off Time	t_{OFF}	Figure 1	9,11 10	All		250 400	ns

NOTE 2: Guaranteed but not production tested.

Figure 1. Switching Time: See Commercial Data Sheet.

TERMINAL CONNECTIONS

TERMINAL NUMBER	01 IH5040	02 IH5041	03 IH5042	04 IH5043	05 IH5044	06 IH5045	06 IH5045	07 IH5047	07 IH5047
0	J16	J16	J16	J16	J16	F14	J16	F14	J16
1	D	D1	D1	D1	D1	D1	D1	D2	D1
2						S3		S1	
3			D2	D3	D2	D3	D3	D1	D3
4			S2	S3	S2	D4	S3	D4	S3
5				S4		S4	S4	S4	S4
6				D4		D2	D4	D3	D4
7						S2		S3	
8		D2		D2		IN2	D2		D2
9		S2		S2		V+	S2	V+	S2
10		IN2		IN2		VL	IN2	VL	IN2
11	V+	V+	V+	V+	V+	VR	V+	VR	V+
12	VL	VL	VL	VL	VL	V-	VL	V-	VL
13	VR	VR	VR	VR	VR	IN1	VR	IN	VR
14	V-	V-	V-	V-	V-	S1	V-	S2	V-
15	IN	IN1	IN	IN1	IN		IN1		IN1
16	S	S1	S1	S1	S1		S1		S1

ORDERING INFORMATION:			
IH5040MJE/883B	16 CDIP	IH5045MFD/883B	14 CFlatpack
IH5041MJE/883B	16 CDIP	IH5045MJE/883B	16 CDIP
IH5042MJE/883B	16 CDIP	IH5047MFD/883B	14 CFlatpack
IH5043MJE/883B	16 CDIP	IH5047MJE/883B	16 CDIP
IH5044MJE/883B	16 CDIP		

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.