SCOPE: CMOS, 12-BIT, SERIAL-INPUT MULTIPLYING DAC

Device Type	Generic Number
01	MAX543AM(x)/883B
02	MAX543BM(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
MAXIN	SMD			
JA	P	GDIP1-T8 or CDIP2-T8	8 LEAD CERDIP	J8
LP	2	CQCC1-N20	20 LEADLESS CHIP CARRIER	L20

Absolute Maximum Ratings:

V_{DD} to GND ..... +17V
VREF to GND ..... ±25V
VRFB to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, (V_{DD}+0.3V)
V_{IOUT} to GND ..... -0.3V, (V_{DD}+0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
8 pin CERDIP(derate 8.0mW/°C above +70°C) 640mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
8 pin CERDIP..... 55°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
8 pin CERDIP..... 125°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤+125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
STATIC PERFORMANCE		2/					
Resolution	N		1,2,3	All	12.0		Bits
Integral nonlinearity	INL		1,2,3	01 02	-0.5 -1.0	+0.5 +1.0	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	01 02	-0.5 -1.0	+0.5 +1.0	LSB
Gain Error	FSE	Use internal R_{FB}	1 1 2,3	01 02 All		±1.0 ±2.0 ±2.0	LSB
Gain Tempco NOTE 2	TCFS	Use internal R_{FB}		All		±5.0	ppm/°C
DC Supply Rejection	PSR	ΔV_{DD}=±5%	1,2,3	All		±0.001	%/%
DYNAMIC PERFORMANCE							
Current Settling Time	t_S	NOTE 2, NOTE 3	9	All		1	µs
Digital-to-Analog Glitch	Q	NOTE 2, NOTE 4	4	All		20	nV-s
AC Feedthrough at I_{OUT}	FTE	NOTE 5	4	All		1	mVp-p
Output Noise-Voltage Density	en	NOTE 6	4	All		15	nV/√Hz
REFERENCE INPUT							
Input Resistance	RREF		1,2,3	All	7	15	kΩ
ANALOG INPUT							
I_{OUT} Leakage Current	I_{LKG}	DAC register all 0s	1 2,3	All		±5 ±100	nA
Output Capacitance	C_{OUT}	DAC register all 0s DAC register all 1s	4	All		80 110	pF
DIGITAL INPUTS							
Input High Voltage	V_{IH}	V_{DD}=5V V_{DD}=15V	1,2,3	All	2.4 13.5		V
Input Low Voltage	V_{IL}	V_{DD}=5V V_{DD}=15V	1,2,3	All		0.8 1.5	V
Input Leakage Current	I_{IN}	Digital inputs=0V or V_{DD}	1,2,3	All		±1.0	µA
Input Capacitance	C_{IN}	Digital inputs=0V or V_{DD}	4	All		8.0	pF
POWER REQUIREMENTS							
Positive Supply Range	V_{DD}	V_{DD}=5V V_{DD}=15V	1,2,3	All	4.75 14.25	5.25 15.75	V
Negative Supply Range	I_{DD}	All digital inputs=V_{IL} or V_{IH} All digital inputs=0V or V_{DD}	1,2,3	All		500 100	µA

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
SWITCHING CHARACTERISTICS		NOTES 5, 6					
CLK Pulse Width High	t_{CH}		9	All	90		ns
CLK Pulse Width Low	t_{CL}		9	All	120		ns
SRI Data to CLK Setup	t_{DS}		9	All	40		ns
SRI Data to CLK Hold	t_{DH}		9	All	80		ns
$\overline{\text{LOAD}}$ Pulse Width	t_{LD}		9	All	120		ns
LSB CLK to $\overline{\text{LOAD}}$	t_{SL}		9	All	0		ns
$\overline{\text{LOAD}}$ High to CLK	t_{LC}		9	All	0		ns

NOTE 1: V_{DD}=+5V or +15V, VREF=+10V, I_{OUT}=GND=0V, unless otherwise noted.
NOTE 2: Characteristics supplied for use as a guaranteed design limit, but not production tested.
NOTE 3: Settling time to 1/2 LSB. I_{OUT} load is 100Ω⏐⏐13pF. DAC register alternately loaded with all 1s and all 0s.
NOTE 4: VREF=0V. I_{OUT} load is 100Ω⏐⏐13pF. DAC register alternately loaded with all 1s and all 0s.
NOTE 5: VREF=±10Vp-p at 10kHz. DAC register loaded with all 0s.
NOTE 6: 10Hz to 100kHz. Measured between R_{FB} and I_{OUT}
NOTE 7: Guaranteed by PSR testing.

	Package	ORDERING INFORMATION:	SMD NUMBER
01	8 pin CERDIP	MAX543AMJA/883B	5962-9234501MPA
01	20 pin LCC	MAX543AMLP/883B	5962-9234501M2C
02	8 pin CERDIP	MAX543BMJA/883B	5962-9234502MPA
02	20 pin LCC	MAX543BMLP/883B	5962-9234502M2C

TERMINAL CONNECTIONS:

PIN	J8	L20	PIN	L20
1	VREF	NC	11	NC
2	RFB	NC	12	NC
3	I_{OUT}	VREF	13	NC
4	GND	RFB	14	$\overline{\text{LOAD}}$
5	$\overline{\text{LOAD}}$	I_{OUT}	15	SRI
6	SRI	GND	16	CLK
7	CLK	NC	17	V_{DD}
8	V_{DD}	NC	18	NC
9		GND	19	NC
10		NC	20	NC

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4**, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4 is guaranteed by design where noted. Capacitance tests are tested only at initial qualification and at redesign. Sample size will be 116 units.