SCOPE: MICROPROCESSOR SUPERVISORY CIRCUITS

Device Type	Generic Number
01	MAX690A(x)/883B
02	MAX692A(x)/883B
03	MAX805L(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JA	GDIP1-T08 or CDIP2-T08	8 LEAD CERDIP	J08

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- V_{BATT} ..... -0.3V to 6.0V
- All other Inputs 1/ ..... -0.3V to (V_{CC}+0.3V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short-circuit protected for up to 10 sec.
- All other outputs 20mA

Rate of Rise, V_{CC}, V_{BATT} 100V/µs

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Continuous Power Dissipation ..... T_A=+70°C
8 lead CERDIP(derate 8.0mW/°C above +70°C) 640mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 8 lead CERDIP..... 55°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 8 lead CERDIP..... 125°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C

1/ The input voltage limits on PFI and WDI may be exceeded if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤+125°C V_{CC} =4.75V to 5.5V for 01,03. V_{CC}=4.5V to 5.5V for 02. V_{BATT}=2.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Operating Voltage Range V_{CC}, V_{BATT}.		NOTE 2	1,2,3	All	1.2	5.5	V
Supply Current (Excluding I_{OUT})	I_{SUPPLY}		1,2,3	All		500	µA
I_{SUPPLY} in Battery Mode (Excluding I_{OUT})		V_{CC}=0V, V_{BATT}=2.8V	1 2,3	All		1.0 5.0	µA
V_{BATT} Standby Current NOTE 3		5.5V>V_{CC}>V_{BATT}+0.2V	1 2,3	All	-0.1 -1.0	0.02 0.02	µA
V_{OUT} Output		I_{OUT}=5mA I_{OUT}=50mA	1,2,3	All	V_{CC} -0.05 V_{CC}-0.5		V
V_{OUT} in Battery-Backup Mode		I_{OUT}=250µA, V_{CC}<V_{BATT}-0.2V	1,2,3	All	V_{BATT}- 0.1		V
Battery Switch Threshold, V_{CC} to V_{BATT}		V_{CC}<V_{RT}, Power Up V_{CC}<V_{RT}, Power Down	1,2,3	All	 -200	+200	mV
Reset Threshold	V_{RT}		1,2,3	01,03 02	4.50 4.25	4.75 4.50	V
Reset Threshold Hysteresis			1,2,3	All		250	mV
Reset Pulse Width	t_{RS}		9,10,11	All	140	280	ms
$\overline{RESET}$ Output Voltage		I_{SOUCE}=800µA I_{SINK}=3.2mA	1,2,3	All	V_{CC}-1.5	0.4	V
		V_{CC}=1.0V, I_{SINK}=50µA V_{CC}=1.2V, I_{SINK}=100µA	1 1,2,3	01,02		0.3 0.3	
Reset Output Voltage		I_{SOURCE}=4µA, V_{CC}=1.2V I_{SOURCE}=800µA I_{SINK}=3.2mA	1,2,3	03	0.9 V_{CC}-1.5	 0.4	V
Watchdog Timeout	t_{WD}		9,10,11	All	1.00	2.25	sec
WDI Pulse Width	t_{WP}	V_{IL}=0.4V, V_{IH}=(0.8)(V_{CC})	9,10,11	All	50		ns
WDI Input Threshold NOTE 4		V_{CC}=5V, Logic low V_{CC}=5V, Logic high	1,2,3	All	 3.5	0.8	V
WDI Input Current		WDI=V_{CC} WDI=0V	1,2,3	All	 -150	150	µA
PFI Input Threshold		V_{CC}=5V	1,2,3	All	1.20	1.30	V
PFI Input Current			1,2,3	All	-25	25	nA
PFO Output Voltage		I_{SOURCE}=800µA I_{SINK}=3.2mA	1,2,3	All	V_{CC}-1.5	 0.4	V

NOTE 2: Either V_{CC} or V_{BATT} can go to 0V, if the other is greater than 2.0V.
NOTE 3: "-"= battery-charging, "+" = battery-discharging current.
NOTE 4: WDI is guaranteed to be in an intermediate, non-logic state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased 35% of V_{CC} with an input impedance of 50kΩ.

	Package	**ORDERING INFORMATION:**
01	8 pin CERDIP	MAX690AMJA/883B
02	8 pin CERDIP	MAX692AMJA/883B
03	8 pin CERDIP	MAX805LMJA/883B

TERMINAL CONNECTIONS:

	MAX690A/692A	MAX805L
	J8	J8
1	V_{OUT}	V_{OUT}
2	V_{CC}	V_{CC}
3	GND	GND
4	PFI	PFI
5	$\overline{PFO}$	$\overline{PFO}$
6	WDI	WDI
7	$\overline{RESET}$	RESET
8	V_{BATT}	V_{BATT}

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.