SCOPE: CMOS, BUFFERED, MULTIPLYING 8-BIT D/A CONVERTER

Device Type	Generic Number	Circuit Function
01	MX7524S(x)/883B	DAC with .5 LSB
02	MX7524T(x)/883B	DAC with .25 LSB
03	MX7524U(x)/883B	DAC with .125 LSB

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
E	CQCC1-N20	20 LCC	L20

Absolute Maximum Ratings:

V_{DD} to GND ..... -.3V, + 17V
V_{RFB} to GND ..... ±25V
V_{REF} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V to V_{DD}
V_{OUT1}, V_{OUT2}, 0 to GND ..... -0.3V to V_{DD}

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 pin CERDIP(derate 10mW/°C above +70°C) 800mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
16 pin CERDIP..... 50°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
16 pin CERDIP..... 100°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Supply Voltage Range ..... +5V to +15V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY							
Resolution NOTE 4	RES	V_{DD}=+5V and V_{DD}=+15V	1,2,3	All	8.0		Bits
Relative Accuracy	RA	V_{DD}=+5V	1,2,3	ALL		±0.5	LSB
Relative Accuracy	RA	V_{DD}=+15V	1,2,3	01 02 03		±0.5 ±0.25 ±0.125	LSB
Gain Error NOTE 2	AE	V_{DD}=+5V	1 2,3	All		±1.0 ±1.4	%/FSR
Gain Error NOTE 2	AE	V_{DD}=+15V	1 2,3	All		±0.5 ±0.6	%/FSR
Power Supply Rejection	PSRR	V_{DD}=+5V, ΔV_{DD}=±10%	1 2,3	All		±0.08 ±0.16	%/%
Power Supply Rejection	PSRR	V_{DD}=+15V, ΔV_{DD}=±10%	1 2,3	All		±0.02 ±0.04	%/%
Output Leakage Current	I_{OUT1}	V_{DD}=+5V DB0-DB7=0V, $\overline{WR}$=$\overline{CS}$=0V	1 2,3	All		±50 ±400	nA
Output Leakage Current	I_{OUT1}	V_{DD}=+15V DB0-DB7=0V, $\overline{WR}$=$\overline{CS}$=0V	1 2,3	All		±50 ±200	nA
Output Leakage Current	I_{OUT2}	V_{DD}=+5V DB0-DB7=V_{DD}, $\overline{WR}$=$\overline{CS}$=0V	1 2,3	All		±50 ±400	nA
Output Leakage Current	I_{OUT2}	V_{DD}=+15V DB0-DB7=V_{DD}, $\overline{WR}$=$\overline{CS}$=0V	1 2,3	All		±50 ±200	nA
Input Resistance	R_{IN}	V_{DD}=+5V and +15V	1,2,3	All	5	20	kΩ
Digital Input High Voltage	V_{IH}	V_{DD}=+5V V_{DD}=+15V	1,2,3	All	2.4 13.5		V
Digital Input Low Voltage	V_{IL}	V_{DD}=+5V V_{DD}=+15V	1,2,3	All		0.8 1.5	V
Digital Input Leakage Current	I_{IN}	V_{DD}=+5V V_{IN}=0V or V_{DD}	1 2,3	All		±1.0 ±10	µA
Digital Input Leakage Current	I_{IN}	V_{DD}=+15V V_{IN}=0V or V_{DD}	1 2,3	All		±1.0 ±10	µA
Supply Current	I_{DD}	V_{DD}=+5V | All digital inputs V_{DD}=+15V | V_{IL} or V_{IH}	1,2,3	All		2.0 2.0	mA
Supply Current	I_{DD}	V_{DD}=+5V & +15V. All digital inputs 0V or V_{DD}	1 2,3	All		100 500	µA
Gain Temperature Coefficient NOTE 3	TC_{AE}	V_{DD}=+5V V_{DD}=+15V	1,2,3	All		±40 ±10	ppm/°C
Feedthrough Error NOTE 3, NOTE 7	FT	V_{DD}=+5V or V_{DD}=+15V, V_{REF}=+10V, 100kHz sinewave, DB0-DB7=0V, $\overline{WR}$=$\overline{CS}$=0V	4,5,6	All		50	mVp-p
Digital Input Capacitance NOTE 3	C_{IN}	V_{DD}=+5V V_{IN}=0V, DB0-DB7 V_{DD}=+15V	4	All		5 20	pF

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Digital Input Capacitance NOTE 3	C_{IN}	V_{DD}=+5V V_{DD}=+15V V_{IN}=0V, $\overline{WR}$, $\overline{CS}$	4	All		5 20	pF
ANALOG INPUTS							
Digital Output Capacitance NOTE 3	C_{OUT1} C_{OUT2}	V_{DD}=+5V and 15, $\overline{WR}$ $\overline{CS}$=0V DB0-DB7=V_{DD}, WR=CS=0V	4	All		120 30	pF
Digital Output Capacitance NOTE 3	C_{OUT1} C_{OUT2}	V_{DD}=+5V and 15V, $\overline{WR}$ $\overline{CS}$=0V DB0-DB7=0V, WR=CS=0V	4	All		30 120	pF
TIMING							
Chip select to write setup time NOTE 3, 7	t_{CS}	V_{DD}=+5V V_{DD}=+15V	9,10,11	All	240 150		ns
Chip select to write hold time NOTE 3, 7	t_{CH}	V_{DD}=+5V V_{DD}=+15V	9,10,11	All	0		ns
Write pulse width NOTE 3, 7	t_{WR}	V_{DD}=+5V, $t_{CS}\geq t_{WR}$, $t_{CH}\geq 0$ V_{DD}=+15V, $t_{CS}\geq t_{WR}$, $t_{CH}\geq 0$	9,10,11	All	240 150		ns
Data setup time NOTE 3, 7	t_{DS}	V_{DD}=+5V V_{DD}=+15V	9,10,11	All	170 100		ns
Data hold time NOTE 3, 7	t_{DH}	V_{DD}=+5V V_{DD}=+15V	9,10,11	All	10 10		ns
Output Current Settling Time NOTE 3, 8	t_{SL}	V_{DD}=+5V V_{DD}=+15V	9,10,11	All		500 350	ns

NOTE 1: $V_{OUT}1=V_{OUT}2=0V$; VREF=+10V, unless otherwise specified.
NOTE 2: Measured using internal RFB and includes effect of leakage current and gain TC.
NOTE 3: Characteristics supplied for use as a typical design limit, but not production tested.
NOTE 4: Guaranteed, if not tested.
NOTE 5: Feedthrough error can be reduced by connecting the metal lid to ground.
NOTE 6: Subgroup 4 (CIN and COUT measurements) shall be measured only for the inital test and after process or design changes which may affect capacitance.
NOTE 7: Timing in accordance with Write Cycle Timing Diagram in Commercial Data Sheet. $\overline{WR}$ $\overline{CS}$
NOTE 8: R_{OUT1} load=100Ω, C_{EXT}=13pF. DB0-DB7=0V to V_{DD} or V_{DD} to 0V, WR, CS=0V. Extrapolated: $t_S(\pm 1/2LSB)=tpD+6.2T$, where T=the measured first time constant of the final RC delay.

MODE SELECTION TABLE:

$\overline{CS}$	$\overline{WR}$	MODE	DAC Response
L	L	Write	DAC responds to data bus (DB0-BD7) inputs
H	X	Hold	Data bus (DB0-DB7) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed High state.
X	H	Hold	

L = Low state, H = High state, X = Don't care

ORDERING INFORMATION:

	Package	**Pkg. Code**	
01	16 pin CERDIP	J16	MX7524SQ/883B
01	20 pin LCC	L20	MX7524SE/883B
02	16 pin CERDIP	J16	MX7524TQ/883B
02	20 pin LCC	L20	MX7524TE/883B
03	16 pin CERDIP	J16	MX7524UQ/883B
03	20 pin LCC	L20	MX7524UE/883B

TERMINAL CONNECTIONS:

	J16	L20
Pin		
1	OUT1	NC
2	OUT2	OUT1
3	GND	OUT2
4	DB7(MSB)	GND
5	DB6	DB7(MSB)
6	DB5	NC
7	DB4	DB6
8	DB3	DB5
9	DB2	DB4
10	DB1	DB3
11	DB0(LSB)	NC
12	$\overline{CS}$	DB2
13	$\overline{WR}$	DB1
14	V_{DD}	DB0(LSB)
15	VREF	$\overline{CS}$
16	RFB	NC
17		$\overline{WR}$
18		V_{DD}
19		VREF
20		RFB

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3, 4, 5, 6, 9**, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroups 9, 10 and 11, if not tested shall be guaranteed to the limits specified in Table 1.