SCOPE: CMOS, PARALLEL-LOADING, DUAL, MULTIPLYING 12-BIT D/A CONVERTER

Device Type	Generic Number
01	MX7537U(x)/883B
02	MX7537T(x)/883B
03	MX7537S(x)/883B
04	MX7547U(x)/883B
05	MX7547T(x)/883B
06	MX7547S(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
MAXIM	SMD			
Q	L	GDIP1-T24 or CDIP2-T24	24 LEAD CERDIP	J24
E	3	CQCC1-N28	28 LEADLESS CHIP	L28

Absolute Maximum Ratings:

V_{DD} to DGND ..... -0.3V, + 17V
V_{RFBA}, V_{RFBB} to AGND ..... ±25V
V_{REFA}, V_{REFB} to AGND ..... ±25V
Digital Input Voltage to DGND ..... -0.3V, (V_{DD}+0.3V)
IOUTA, IOUTB Voltage to DGND ..... -0.3V, (V_{DD}+0.3V)
AGND to DGND ..... -0.3V, (V_{DD}+0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
24 pin CERDIP(derate 12.5mW/°C above +70°C) 1000mW
28 pin LCC(derate 10.2mW/°C above +70°C) 816mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
24 pin CERDIP..... 40°C/W
28 pin LCC ..... 15°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
24 pin CERDIP..... 80°C/W
28 pin LCC ..... 98°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Logic Supply Voltage (V_{LOGIC}) ..... +4.5V to +5.5V
Positive Supply Voltage (V_{DD})..... +11.4V to +16.5V
Negative Supply Voltage (V_{EE})..... -11.4V to -16.5V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY							
Resolution	RES		1,2,3	All	12.0		Bits
Relative Accuracy	RA	V_{DD}=+10.8V and V_{DD}=+16.5V V_{DD}=10.8V (MX7547 only)	1,2,3	1,2,4,5 3,6		±0.5 ±1.0	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	All		±1.0	LSB
Gain Error	AE	Measured using R_{FBA}, R_{FBB}; DAC registers loaded with all 1's, V_{DD}=10.8V	1,2,3	1,4 2,5 3,6		±2.0 ±3.0 ±6.0	LSB
Gain Tempco ΔGain/ΔTemperature NOTE 2	TCFS		4	All		±5.0	ppm/°C
Output Leakage Current IOUTA, IOUTB	ILKG	V_{DD}=+16.5V, DAC registers loaded with all 0s	1,3 2	All		±10 ±250	nA
VREFA, VREFB Input Leakage	RREF	V_{DD}=+10.8V	1,2,3	All	9	20	kΩ
VREFA, VREFB Input Resistance Match	ΔRREF	V_{DD}=+10.8V	1,2,3	1,4 2,3,5,6		±1.0 ±3.0	%
Digital Input High Voltage	V_{IH}	V_{DD}=+10.8V and V_{DD}=+16.5V	1,2,3	All	2.4		V
Digital Input Low Voltage	V_{IL}	V_{DD}=+10.8V and V_{DD}=+16.5V	1,2,3	All		0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN}=+0V or 16.5V	1,3 2	All		±1.0 ±10	µA
Digital Input Capacitance	C_{IN}		4	All		10	pF
Supply Voltage	V_{DD}	Operating range, V_{DD}=16.5V	1,2,3	All	10.8	16.5	V
Supply Current	I_{DD}		1,2,3	All		2.0	mA
Current Settling Time	t_{SL}	To 0.5 LSB, IOUT load =100Ω, CEXT=13pF, DAC output measured from falling edge of $\overline{WR}$	9,10,11	4,5,6		1.5	µs
Current Settling Time	t_{SL}	To 0.5 LSB, IOUT load =100Ω, CEXT=13pF, DAC output measured from rising edge of $\overline{WR}$	4	1,2,3		1.5	µs
Feedthrough Error VREFA to IOUTA VREFB to IOUTB NOTE 2	FTE	DAC registers loaded with all 0s	VREFA=20Vp-p 10kHz sine wave, VREFB=0V VREFB=20Vp-p 10kHz sine wave, VREFA=0V	4,5,6 (SMD)	4,5,6	-70	-65 (SMD)	dB
Feedthrough Error VREFA to IOUTA VREFB to IOUTB NOTE 2	FTE	DAC registers loaded with all 0s	VREFA=20Vp-p 10kHz sine wave, VREFB=0V VREFB=20Vp-p 10kHz sine wave, VREFA=0V	4 (SMD)	1,2,3	-70	-65 (SMD)	dB

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Power-Supply Rejection Ratio	PSRR	V_{DD}=10.8V, ΔV_{DD}=12V±5%	1 2,3	01,02,03		±0.01 ±0.02	%/%
		V_{DD}=10.8V, ΔV_{DD}=V_{DD} MAX - V_{DD} MIN	1 2,3	All		±0.01 ±0.02	
Output Capacitance (IOUTA, IOUTB)	C_{OUT}	DAC A, DAC B loaded with 0s DAC A, DAC B loaded with 1s	4	All		-70 140	dB
Channel-to-Channel Isolation	VREFA to IOUTA VREFB to IOUTB	VREFA=20Vp-p, 10kHz sine wave, VREFB=0V VREFB=20Vp-p, 10kHz sine wave, VREFA=0V	4	All	-84		dB
TIMING							
Address Valid to Write-setup Time	t_1		9 10,11	01,02,03	20 30		ns
Address Valid to Write-hold Time	t_2		9 10,11	01,02,03	15 25		ns
Data-setup Time	t_3		9 10,11	All	60 80		ns
Data-hold Time	t_4		9,10,11	All	25		ns
Chip Select or Update to Write-setup Time	t_5		9,10,11 9 10,11	01,02,03 04,05,06	0 80 100		ns
Chip Select orUpdate to Write Hold Time	t_6		9,10,11	All	0		ns
Write Pulse Width	t_7		9 10,11	All	80 100		ns
Clear Pulse Width	t_8		9 10,11	All	80 100		ns

NOTE 1: Conditions unless otherwise specified, 4.5V≤V_{DD}≤5.5V. VDD=10.8V to 16.5V, AGND=DGND=0V, use maximum possible reference voltage.

NOTE 2: Typical number, for design aid only.

MODE SELECTION TABLE:

						MX7537
$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	Function
1	1	1	X	X	X	No data transfer
1	1	X	1	X	X	No data transfer
0	X	X	X	X	X	All registers cleared
1	1	0	0	0	0	DAC A LS input register loaded with D7-D0
1	1	0	0	0	1	DAC A MS input register loaded with D3-D0
1	1	0	0	1	0	DAC B LS input register loaded with D7-D0
1	1	0	0	1	1	DAC B MS input register loaded with D3-D0
1	0	1	0	X	X	DAC A, DAC B registers updated simultaneously from input registers. Input registers not changed.
1	0	0	0	X	X	DAC A, DAC B registers are transparent. Input registers loaded.

X = Don't care

MODE SELECTION TABLE:

			MX7547
$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No data transfer
1	1	X	No data transfer
↑	↑	0	A rising edge on $\overline{CSA}$ or $\overline{CSB}$ transfer data to the respective DAC.
0	1	↑	DAC A register loaded from data bus.
1	0	↑	DAC B register loaded from data bus.
0	0	↑	DAC A and DAC B registers loaded from data bus.

X= don't care WR input is edge-triggered.

ORDERING INFORMATION:

	Package	Pkg. Code	Device ID	SMD Number
01	24 pin CERDIP	J24	MX7537UQ/883B	5962-8776303LA
02	24 pin CERDIP	J24	MX7537TQ/883B	5962-8776302LA
03	24 pin CERDIP	J24	MX7537SQ/883B	5962-8776301LA
01	28 pin LCC	L28	MX7537UE/883B	5962-87763033C
02	28 pin LCC	L28	MX7537TE/883B	5962-87763023C
03	28 pin LCC	L28	MX7537SE/883B	5962-87763013C
04	24 pin CERDIP	J24	MX7547UQ/883B	5962-8965703LA
05	24 pin CERDIP	J24	MX7547TQ/883B	5962-8965702LA
06	24 pin CERDIP	J24	MX7547SQ/883B	5962-8965701LA
04	28 pin LCC	L28	MX7547UE/883B	5962-89657033C
05	28 pin LCC	L28	MX7547TE/883B	5962-89657023C
06	28 pin LCC	L28	MX7547SE/883B	5962-89657013C

TERMINAL CONNECTIONS:

	MX7537 J24	MX7537 L28	MX7547 J24	MX7547 L28		MX7537 J24	MX7537 L28	MX7547 J24	MX7547 L28
1	AGNDA	NC	AGNDA	NC	15	A0	NC	D8	NC
2	I_{OUTA}	AGNDA	I_{OUTA}	AGNDA	16	A1	D6	D9	D6
3	RFBA	I_{OUTA}	RFBA	I_{OUTA}	17	$\overline{CLR}$	D7	D10	D7
4	VREFA	RFBA	VREFA	RFBA	18	$\overline{WR}$	A0	D11 (MSB)	D8
5	$\overline{CS}$	VREFA	$\overline{CSA}$	VREFA	19	$\overline{UPD}$	A1	$\overline{WR}$	D9
6	D0	$\overline{CS}$	(LSB)D0	$\overline{CSA}$	20	V_{DD}	$\overline{CLR}$	$\overline{CSB}$	D10
7	D1	D0	D1	(LSB)D0	21	VREFB	$\overline{WR}$	V_{DD}	D11
8	D2	NC	D2	NC	22	RFBB	NC	VREFB	NC
9	D3	D1	D3	D1	23	I_{OUTB}	$\overline{UPD}$	RFBB	$\overline{WR}$
10	D4	D2	D4	D2	24	AGNDB	V_{DD}	I_{OUTB}	$\overline{CSB}$
11	D5	D3	D5	D3	25		VREFB		V_{DD}
12	DGND	D4	DGND	D4	26		RFBB		VREFB
13	D6	D5	D6	D5	27		I_{OUTB}		RFBB
14	D7	DGND	D7	DGND	28		AGNDB		I_{OUTB}

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 4**, 5**, 6**, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** If not tested shall be guaranteed to the limits specified in Table 1.