SCOPE: CMOS, 12-BIT MONOLITHIC, MULTIPLYING D/A CONVERTER

Device Type	Generic Number
01	MX7541AS(x)/883B
02	MX7541AT(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP1-T18 or CDIP2-T18	18 LEAD CERDIP	J18
E	CQCC1-N20	20 LCC	L20

Absolute Maximum Ratings:

V_{DD} to GND .....+ 17V
V_{RFB} to GND ..... ±25V
V_{REF} to GND ..... ±25V
Digital Input Voltage Range ..... -0.3V to V_{DD}
V_{OUT1}, V_{OUT2}, to GND ..... -0.3V to V_{DD}

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
18 pin CERDIP(derate 10.5mW/°C above +70°C) 842mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
18 pin CERDIP..... 45°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
18 pin CERDIP..... 95°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Logic Supply Voltage (VLOGIC) ..... +4.5D to +5.5V
Positive Supply Voltage ..... +15V
Negative Supply Voltage ..... -15V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY							
Resolution NOTE 2	RES			All	12		Bits
Relative Accuracy	RA		1,2,3	01 02		±1.0 ±0.5	LSB
Differential Nonlinearity	DNL	All grades guaranteed monotonic over temperature	1,2,3	01 02		±1.0 ±0.5	LSB
Gain Error NOTE 3	AE		1 2,3	01		±6 ±8	LSB
			1 2,3	02		±3 ±5	
Gain Temperature Coefficient NOTE 2	TC_{AE}			All		±5	ppm/°C
Power Supply Rejection	PSRR	ΔV_{DD}=±5%	1 2,3	All		±0.01 ±0.02	%/%
Output Leakage Current	I_{OUT1}	Digital inputs = 0V	1 2,3	All		±5.0 ±200	nA
	I_{OUT2}	Digital inputs = V_{DD}	1 2,3	All		±5.0 ±200	
Output Current Settling Time NOTE 2		To ±0.5%LSB. OUT 1 load is 100Ω|| 13pF, digital inputs =V_{IH} to V_{IL} or V_{IL} to V_{IH}	4	All		0.6	µs
Feedthrough Error NOTE 2, NOTE 4	FTE	VREF=20Vp-p at 10kHz sine wave	4	All		1.0	mVp-p
Input Resistance	R_{IN}		1,2,3	All	7	18	kΩ
Digital Input High Voltage	V_{IH}		1,2,3	All	2.4		V
Digital Input Low Voltage	V_{IL}		1,2,3	All		0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN}=0V or V_{DD}	1 2,3	All		±1.0	µA
Supply Current	I_{DD}	All digital inputs V_{IL} or V_{IH}	1,2,3	All		2.0	mA
		All digital inputs 0V or V_{DD}	1 2,3	All		100 500	
Digital Input Capacitance NOTE 2	C_{IN}		4	All		8	pF
Output Capacitance NOTE 2	C_{OUT1}	Digital inputs at V_{IH} Digital inputs at V_{IL}	4	All		200 70	pF
	C_{OUT2}	Digital inputs at V_{IH} Digital inputs at V_{IL}				70 200	

NOTE 1: V_{DD}=+15V, V_{OUT1}=V_{OUT2}=0V; VREF=+10V, unless otherwise specified.
NOTE 2: Characteristics supplied for use as a typical design limit, but not production tested.
NOTE 3: Measured using internal feedback resistor and includes effect of leakage current and gain TC.
NOTE 4: Feedthrough error can be reduced by connecting the metal lid on the package to ground.

ORDERING INFORMATION:

	Package	**Pkg. Code**	**MAXIM PART #**	**SMD NUMBER**
01	18 pin CERDIP	J18	MX7541ASQ/883B	5962-8948101VA
01	20 pin LCC	L20	MX7541ASE/883B	5962-89481012C
02	18 pin CERDIP	J18	MX7541ATQ/883B	5962-8948102VA
02	20 pin LCC	L20	MX7541ATE/883B	5962-89481022C

TERMINAL CONNECTIONS:

	J18	L20
Pin		
1	OUT1	NC
2	OUT2	OUT1
3	GND	OUT2
4	D1(MSB)	GND
5	D2	D1(MSB)
6	D3	D2
7	D4	D3
8	D5	D4
9	D6	D5
10	D7	D6
11	D8	NC
12	D9	D7
13	D10	D8
14	D11	D9
15	D12(LSB)	D10
16	V_{DD}	D11
17	VREF	D12(LSB)
18	R_{FB}	V_{DD}
19		VREF
20		R_{FB}

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3, 4**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 116 units.