SCOPE: CMOS, µP-Compatible, 12-Bit D/A Converter

Device Type:	**Generic Number:**
-01	**MX7542S(x)/883B**
-02	**MX7542T(x)/883B**
-03	**MX7542GT(x)/883B**

Case Outline(s).

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP1-T16 or CDIP2-T16	16 Lead CERDIP	J16
E	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maxi mum Ratings: (T_A=+25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +7V
V_{DD} to DGND ..... 0V, +7V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{OUT1}, V_{OUT2} to AGND ..... -0.3V, V_{DD}
VREF to AGND ..... -25V to +25V
V_{RFB} to AGND ..... -25V to +25V

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 pin CERDIP(derate 10mW/°C above +70°C) 800mW
20 pin LCC(derate 9.09mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
16 pin CERDIP..... 50°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
16 pin CERDIP..... 100°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS $-55°C \le T_A \le +125°C$ 1/ Unless otherwise specified	GROUP A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution	RES	NOTE 2		All	12		Bits
Relative Accuracy	RA		1,2,3	01 02,03	-1 -0.5	1 0.5	LSB
Differential Nonlinearity	DNL	Monotonic to 11 bits Monotonic to 12 bits	1,2,3	01 02,03	-2 -1	2 1	LSB
Gain Error NOTE 3	AE		1 2,3	01,02	-12.3 -14.5	12.3 14.5	LSB
Gain Error NOTE 3	AE		1 2,3	03	-1 -2	1 2	LSB
Gain Tempco	TC_{AE}	NOTE 2		All	-5	5	ppm/°C
Power-Supply Rejection	PSRR	V_{DD}=4.75V to 5.25V ($\Delta Gain/\Delta V_{DD}$)	1 2,3	All	-0.005 -0.01	0.005 0.01	$\%/\%V_{DD}$
OUT1 Leakage Current	I_{OUT1}	DAC register loaded with all 0s	1 2,3	All	-1 -200	1 200	nA
OUT2 Leakage Current	I_{OUT2}	DAC register loaded with all 1s	1 2,3	All	-1 -200	1 200	nA
Output Current Settling Time NOTE 2	t_{SL}	To ±0.5LSB, OUT1 load is 100 Ω || 13pF, output measured ___ from trailing edge of WR	4	All		2	µs
Feedthrough Error NOTE 2	FT	VREF=10V, 10kHz sine wave	4	All		2.5	mVp-p
Reference Input Resistance	R_{IN}		1,2,3	All	8	25	kΩ
Digital Input High Voltage	V_{IH}		1,2,3	All	3.0		V
Digital Input Low Voltage	V_{IL}		1,2,3	All		0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN}=0V or V_{DD}	1,2,3	All	-1	1	µA
Digital Input Capacitance NOTE 2	C_{IN}		4	All		8	pF
Output Capacitance NOTE 2	C_{OUT1}	Digital inputs at V_{IH}, DAC register loaded with all 1s Digital inputs at V_{IL}, DAC register loaded with all 0s	4	All		260 75	pF
Output Capacitance NOTE 2	C_{OUT2}	Digital inputs at V_{IH}, DAC register loaded with all 1s Digital inputs at V_{IL}, DAC register loaded with all 0s	4	All		75 260	pF

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS $-55°C \le T_A \le +125°C$ 1/ Unless otherwise specified	GROUP A Subgroup	Device type	Limits Min	Limits Max	Units
Write Pulse Width	t_{WR}	NOTE 4	9	All	220		ns
Address to Write-Hold Time	t_{AWH}	NOTE 4	9	All	80		ns
Chip Select to Write-Hold Time	t_{CWH}	NOTE 4	9	All	100		ns
Minimum Clear Pulse Width	t_{CLR}	NOTE 4	9	All	300		ns
Chip Select to Write-Setup Time	t_{CWS}	Byte loading, NOTE 4	9	All	130		ns
Address Valid to Write-Setup Time	t_{AWS}	Byte loading, NOTE 4	9	All	180		ns
Data-Setup Time	t_{DS}	NOTE 4	9	All	350		ns
Data-Hold Time	t_{DH}	NOTE 4	9	All	65		ns
Chip Select to Write-Setup Time	t_{CWS}	DAC loading, NOTE 4	9	All	150		ns
Address Valid to Write-Setup Time	t_{AWS}	DAC loading, NOTE 4	9	All	240		ns
Supply Current	I_{DD}	Digital inputs = V_{IH} or V_{IL}	1,2,3	All		2.5	mA

NOTE 1: V_{DD}=+5V, V_{OUT1}=V_{OUT2}=0V, VREF=+10V, unless otherwise noted.
NOTE 2: Characteristics supplied for use as a typical design limit but not production tested.
NOTE 3: Measured using internal feedback resistor; includes effects of leakage current and gain TC.
NOTE 4: Timing shown in commercial datasheet.

TERMINAL CONNECTIONS:

	MX7542				
	J16	L20		J16	L20
1	OUT1	NC	11	A1	NC
2	OUT2	OUT1	12	DGND	$\overline{WR}$
3	AGND	OUT2	13	$\overline{CLR}$	A0
4	D3	AGND	14	V_{DD}	A1
5	D2	D3	15	VREF	DGND
6	D1	NC	16	R_{FB}	NC
7	D0	D2	17		$\overline{CLR}$
8	$\overline{CS}$	D1	18		V_{DD}
9	$\overline{WR}$	D0	19		VREF
10	A0	$\overline{CS}$	20		R_{FB}

ORDERING INFORMATION:

01	J16	MX7542SQ/883B
01	L20	MX7542SE/883B
02	J16	MX7542TQ/883B
02	L20	MX7542TE/883B
03	J16	MX7542GTQ/883B
03	L20	MX7542GTE/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with Mil-Prf-38535, Appendix A as Specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. T_A = +125°C, minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, Including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883.
   1. Test condition A, B, C, D.
   2. T_A = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups Per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3, 4** 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 116 units.